NCP5359

Gate Driver for Notebook Power Systems

The NCP5359 is a high performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. Each of the drivers can drive up to 3 nF load with a 25 ns propagation delay and 20 ns transition time.

Adaptive nonoverlap and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook and desktop systems.

A high floating top driver design can accommodate VBST voltage as high as 35 V, with transient voltages as high as 35 V. Bidirectional EN pin can provide a fault signal to controller when the gate driver fault detect under OVP, UVLO occur. Also, an undervoltage lockout function guarantees the outputs are low when supply voltage is low, and a thermal shutdown function provides the IC with overtemperature protection.

Features

- Faster Rise and Fall Times
- Thermal Shutdown Protection
- Adaptive Nonoverlap Circuit
- Floating Top Driver Accommodates Boost Voltages of up to 35 V
- Output Disable Control Turns Off Both MOSFETs
- Complies with VRM 11.1 Specifications
- Undervoltage Lockout
- Power Saving Operation Under Light Load Conditions
- Thermally Enhanced Package
- These are Pb−Free Devices

Typical Applications

- Power Solutions for Desktop and Notebook Systems

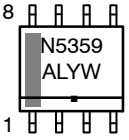
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MARKING DIAGRAMS



SOIC−8
D SUFFIX
CASE 751



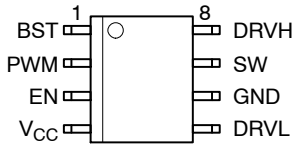


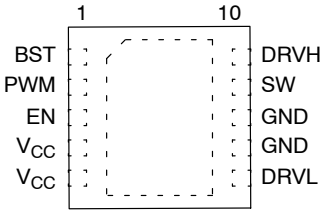
DFN−10
MN SUFFIX
CASE 485C



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS





(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5359DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
NCP5359MNR2G	DFN−10 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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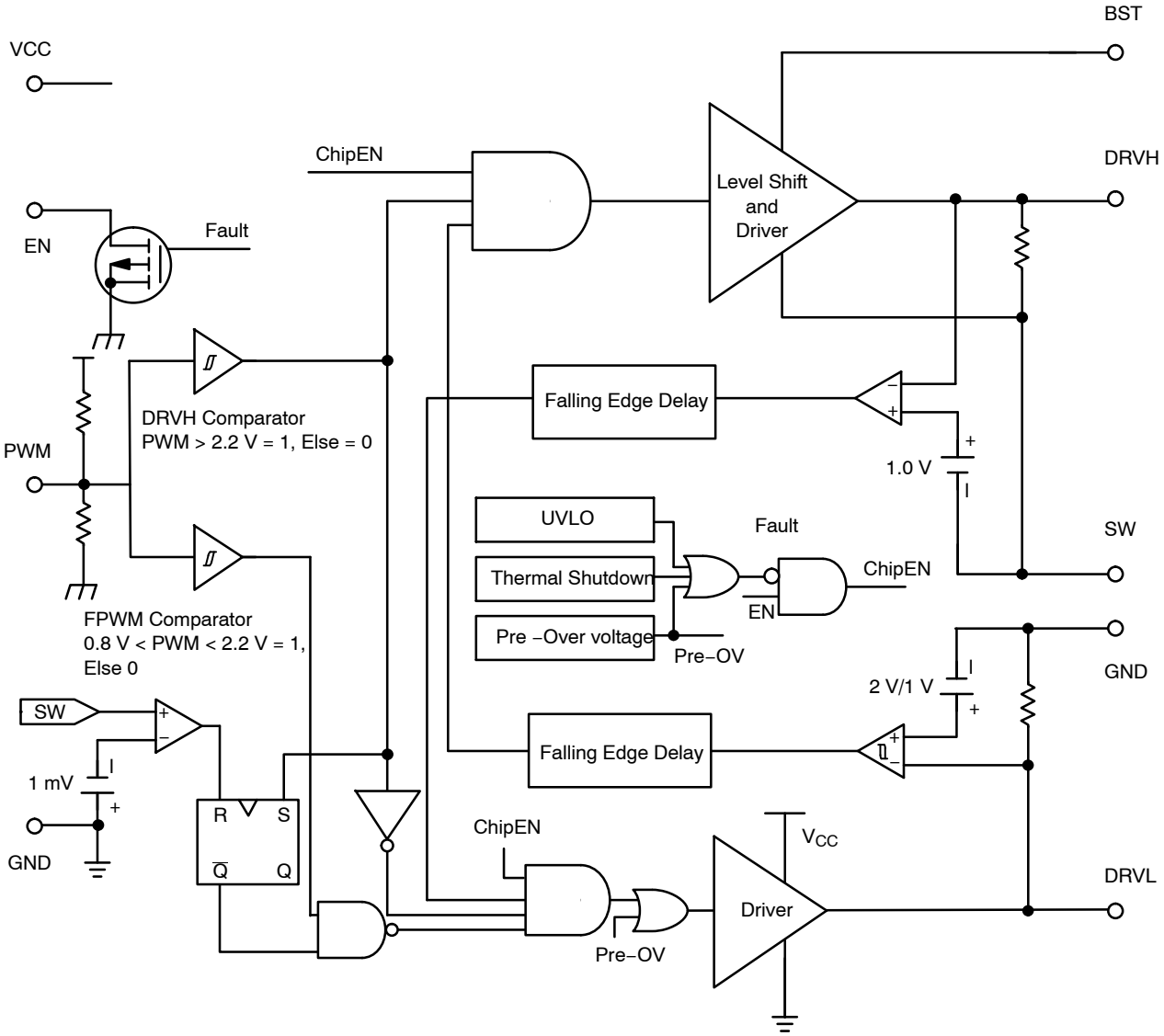


Figure 1. Internal Block Diagram

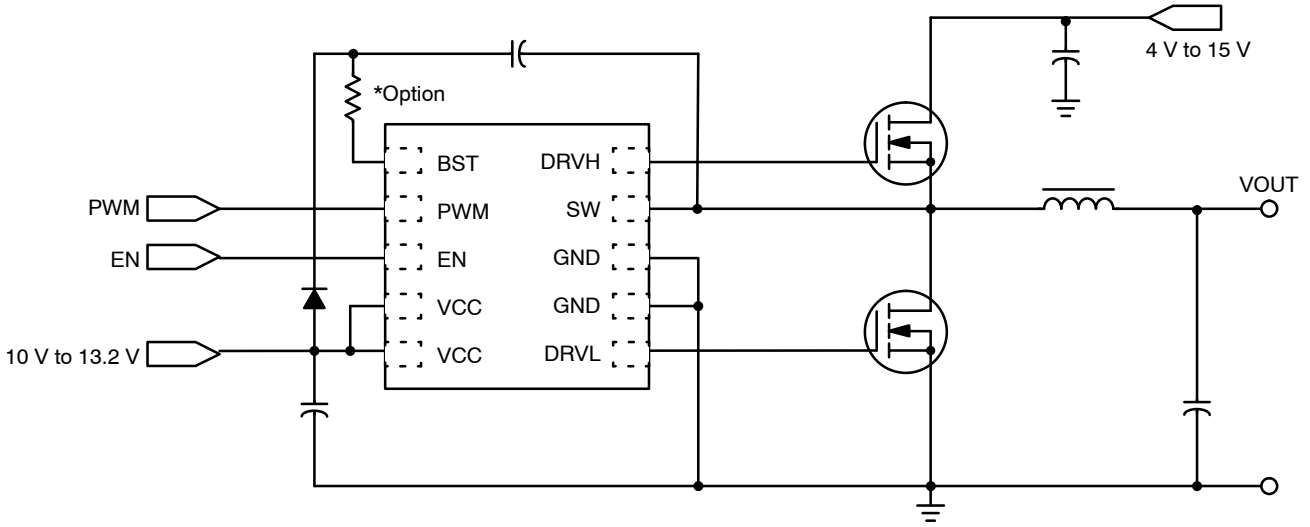


Figure 2. Typical Application

PIN DESCRIPTION

SOIC−8	DFN10	Symbol	Description
1	1	BST	Upper MOSFET Floating Bootstrap Supply Pin
2	2	PWM	PWM Input Pin When PWM voltage is higher than 2.2 V, DRVH will set to 1 and DRVL set to 0 When PWM voltage is lower than 0.8 V, DRVL will set to 1 and DRVH set to 0 When 0.8 V < PWM < 2.2 V and SW < 0, DRVL will set to 1 When 0.8 V < PWM < 2.2 V and SW > 0, DRVL will set to 0
3	3	EN	Enable Pin When OVP, TSD or UVLO has happened, the gate driver will pull the pin to low
4	4, 5	VCC	Connect to Input Power Supply 10 V to 13.2 V
5	6	DRVL	Low Side Gate Drive Output
6	7, 8	GND	Ground Pin
7	9	SW	Switch Node Pin
8	10	DRVH	High Side Gate Drive Output

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Thermal Characteristics, Plastic Package Thermal Resistance Junction−to−Air	 SOIC−8 DFN10	$R_{\theta JA}$	 178 45	°C/W
Operating Junction Temperature Range		T_J	0 to +150	°C
Operating Ambient Temperature Range		T_A	0 to +85	°C
Storage Temperature Range		T_{stg}	− 55 to +150	°C
Moisture Sensitivity Level	SOIC−8 DFN10	MSL	3 1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
Vcc	Main Supply Voltage Input	15 V	−0.3 V
BST	Bootstrap Supply voltage	35 V wrt / GND 40 V ≤ 50 ns wrt / GND 15V wrt / SW	−0.3 V
SW	Switching Node (Bootstrap Supply Return)	35 V wrt / GND 40 V ≤ 50 ns wrt / GND	−1 VDC −10 V (200 ns) (Note 4)
DRVH	High Side Driver Output	BST + 0.3 V 35 V ≤ 50 ns wrt / GND 15V wrt / SW	−0.3 V −2 V (200 ns)
DRVL	Low Side Driver Output	Vcc + 0.3 V	−0.3 V −5 V (200 ns)
PWM	DRVH and DRVL Control Input	6 V	−0.3 V
EN	Enable Pin	6 V	−0.3 V
GND	Ground	0 V	0 V

1. Latchup Current Maximum Rating: 100 mA per JEDEC standard: JESD78.
2. Moisture Sensitivity Level (MSL): 1&3 per IPC/JEDEC standard: J−STD−020A.
3. The maximum package power dissipation limit must not be exceeded.

$$PD = \frac{TJ(max) - TA}{R\theta JA}$$

4. Switching node negative voltage is −5 V (200 ns) at PSI mode.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_A = 0°C to +85°C, V_{EN} = 5 V unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage						
V_{CC} Operating Voltage	V_{CC}		10		13.2	V
Power ON Reset threshold	V_{POR}			2.8		V
Supply Current						
V_{CC} Quiescent Supply Current in Normal Operation	I_{VCC_NORM}	EN = 5 V, PWM = OSC, F_{SW} = 100 k C_{LOAD} = 0 p		2.0	5.0	mA
V_{CC} Standby Current	I_{VCC_SBC}	EN = GND; No switching		0.5	1.0	mA
BST Quiescent Supply Current in Normal Operation	I_{BST1_normal}	PWM = +5 V, SW = 0 V		1.0	1.8	mA
	I_{BST2_normal}	PWM = GND, SW = 0 V		1.0	1.8	
BST Standby Current	I_{BST1_SD}	PWM = +5 V		0.25		mA
	I_{BST2_SD}	PWM = GND		0.25		
Undervoltage Lockout						
V_{CC} Start Threshold	VCC_{TH}		8.2	8.7	9.5	V
V_{CC} UVLO Hysteresis	VCC_{HYS}			1.0		V
Output Overvoltage Trip Threshold at Startup	OVPSU	Power Startup time, V_{CC} > 9 V. (Without trimming)	1.8		2.0	V
EN Input						
Input Voltage High	V_{EN_HI}		2.0			V
Input Voltage Low	V_{EN_LOW}				1.0	V
Hysteresis (Note 5)	V_{EN_HYS}			500		mV
Enable Pin Sink Current	I_{EN_SINK}	V_{CC} = 5.5 V	5.0			mA
Propagation Delay Time (Note 5)	tpd_{hEN}			20	60	ns
	tpd_{lEN}			20	60	ns
PWM Input						
DRVH Comparator Drop Threshold	VTH_DRVH		2.2			V
PWM Input Self Bias Voltage	V_{PWM}		1.4	1.5	1.6	V
DRVL Comparator Rise Threshold	VTH_DRVL				0.8	V
Input Current	I_{PWM}	PWM = 0 V, EN = GND		30		μA
High Side Driver						
Output Resistance, Sourcing	R_{H_TG}	$V_{BST} - V_{SW}$ = 12 V		2.0	3.5	Ω
Output Resistance, Sinking	R_{L_TG}	$V_{BST} - V_{SW}$ = 12 V		1.0	2.5	Ω
Transition Time (Note 7)	tr_{DRVH}	C_{LOAD} = 3 nF, $V_{BST} - V_{SW}$ = 12 V		16	25	ns
	tf_{DRVH}	C_{LOAD} = 3 nF, $V_{BST} - V_{SW}$ = 12 V		11	15	
Propagation Delay (Notes 5 & 6)	$tpdh_{DRVH}$	Driving High, C_{LOAD} = 3 nF	10		35	ns
	$tpdl_{DRVH}$	Driving Low, C_{LOAD} = 3 nF	8.0		30	
Low Side Driver						
Output Resistance, Sourcing	R_{H_BG}	SW = GND		2.0	3.5	Ω
Output Resistance, Sinking	R_{L_BG}	SW = V_{CC}		1.0	2.5	Ω
Transition Time (Note 7)	tr_{DRVL}	C_{LOAD} = 3 nF		16	25	ns
	tf_{DRVL}	C_{LOAD} = 3 nF		11	15	
Propagation Delay (Notes 5 & 6)	$tpdh_{DRVL}$	Driving High, C_{LOAD} = 3 nF	10		35	ns
	$tpdl_{DRVL}$	Driving Low, C_{LOAD} = 3 nF	8.0		30	
Negative Current Detector Threshold	V_{NCDT}	(Note 7)		−1.0		mV
Thermal Shutdown						
Thermal Shutdown	Tsd	(Note 7)	150	170		°C
Thermal Shutdown Hysteresis	Tsd_{hys}	(Note 7)		20		°C

5. Guaranteed by design; not tested in production .
6. For propagation delays, "t_{pdh}" refers to the specified signal going high "t_{pdl}" refers to it going low.
7. Design guaranteed.

Table 1. DECODER TRUTH TABLE

PWM Input	ZCD	DRVL	DRVH
Greater than 2.2 V	X	Low	High
Greater than 0.8 V, but less than 2.2 V	High (current through MOSFET is greater than 0)	High	Low
Greater than 0.8 V, but less than 2.2 V	Low (current through MOSFET is less than 0)	Low	Low
Less than 0.8 V	X	High	Low

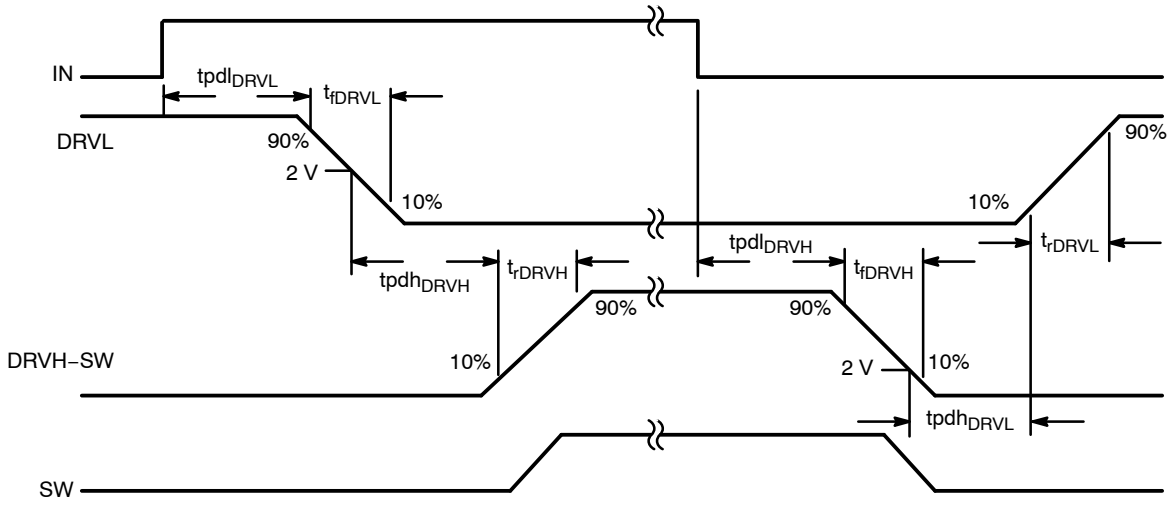


Figure 3.

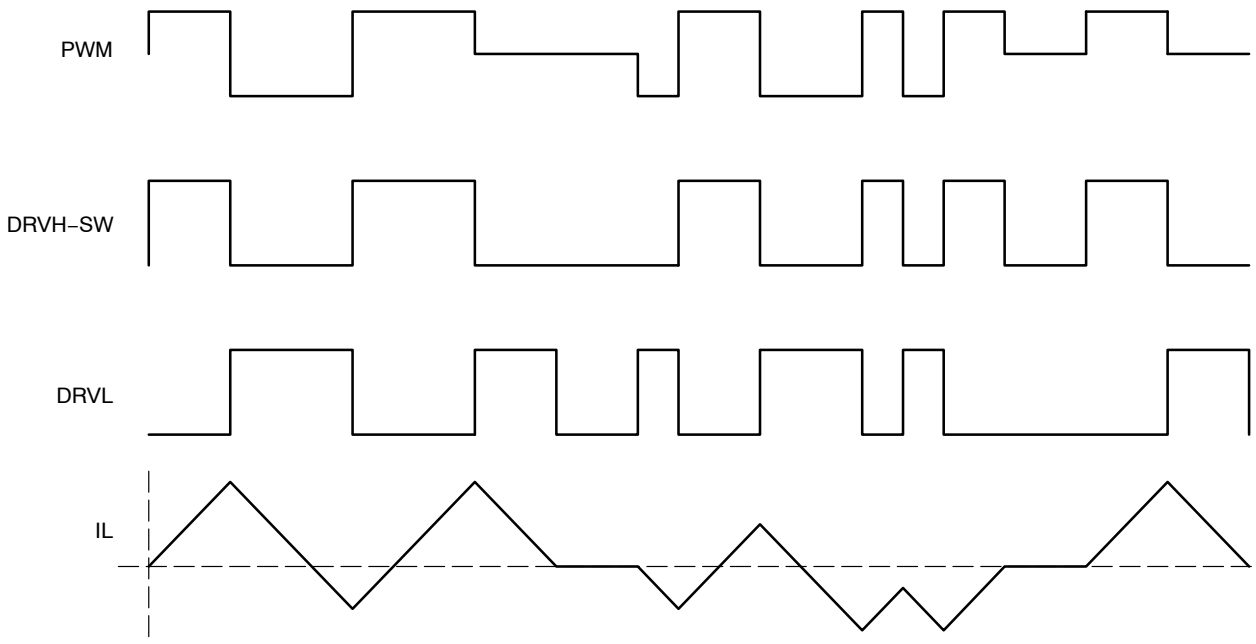


Figure 4. Timing Diagram

APPLICATION INFORMATION

The NCP5359 gate driver is a single phase MOSFET driver designed for driving two N−channel MOSFETs in a synchronous buck converter topology. This driver is compatible with the NCP3418B gate drive. This gate drives operation is similar with the NCP3418B, but has two additional new features: Bidirection fault detection and multilevel PWM input. When the gate driver works with ON Semiconductor's NCP5392 controller, it can provide a difference output logic status through multi−level PWM input. For this new feature, higher efficiency can be provided. For the bidirection fault detection function, it is used to provide a driver state information to other gate drivers and controller in a multiphase buck converter. e.g overvoltage protection (OVP) function at startup, thermal shutdown and undervoltage lockout (UVLO). This feature can provide an additional protection function for the multi−phase system when the fault condition occurs in one channel. With this additional feature, converter overall system will be more reliable and safe.

Enable Pin

The bidirection enable pin is connected with an open drain MOSFET. This pin is controlled by internal or external signal. There are three conditions will be triggered:

1. The voltage at SWN pin is higher than preset voltage at power startup.
2. The controller hits the UVLO at V_{CC} pin.
3. The controller hits the thermal shutdown.

When the internal fault has been detected, EN pin will be pull low. In this case, the drive output DRVH and DRVL will be forced low, until the fault mode remove then restart automatic.

Undervoltage Lockout

The DRVH and DRVL are held low until V_{CC} reaches 9 V during startup. The PWM signals will control the gate status when V_{CC} threshold is exceeded. If V_{CC} decreases to 3.2 V below the threshold, the output gate will be forced low until input voltage V_{CC} rises above the startup threshold.

Power ON reset

Power on reset feature is used to protect a gate driver avoid abnormal status driving the startup condition. When the initial soft−start voltage is higher than 3.2 V, the gate driver will monitor the switching node SW pin. If SW pin high than 1.9 V, bottom gate will be force to high for discharge the output capacitor. The fault mode will be latch and EN pin will force to be low, unless the driver is recycle. When input voltage is higher than 9 V, the gate driver will normal operation, top gate driver DRVH and bottom gate driver will follow the PWM signal decode to a status.

Adaptive Nonoverlap

The nonoverlap dead time control is used to avoid the shoot through damage the power MOSFETs. When the PWM signal pull high, DRVL will go low after a propagation delay, the controller will monitors the switching node (SWN) pin voltage and the gate voltage of the MOSFET to know the status of the MOSFET. When the low side MOSFET status is off an internal timer will delay turn on of the high–side MOSFET. When the PWM pull low, gate DRVH will go low after the propagation delay (tpd DRVH). The time to turn off the high side MOSFET is depending on the total gate charge of the high−side MOSFET. A timer will be triggered once the high side MOSFET is turn off to delay the turn on the low−side MOSFET.

Layout Guidelines

Layout is very important thing for design a DC−DC converter. Bootstrap capacitor and V_{CC} capacitor are most critical items, it should be placed as close as to the driver IC. Another item is using a GND plane. Ground plane can provide a good return path for gate drives for reducing the ground noise. Therefore GND pin should be directly connected to the ground plane and close to the low−side MOSFET source pin. Also, the gate drive trace should be considered. The gate drives has a high di/dt when switching, therefore a minimized gate drives trace can reduce the di/dv, raise and fall time for reduce the switching loss.

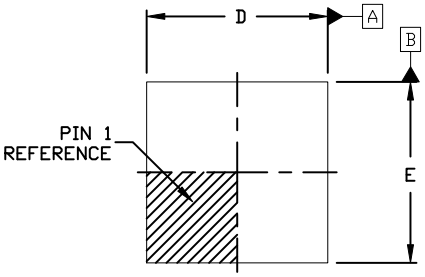
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

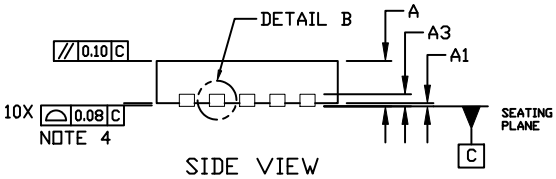
DATE 16 DEC 2021



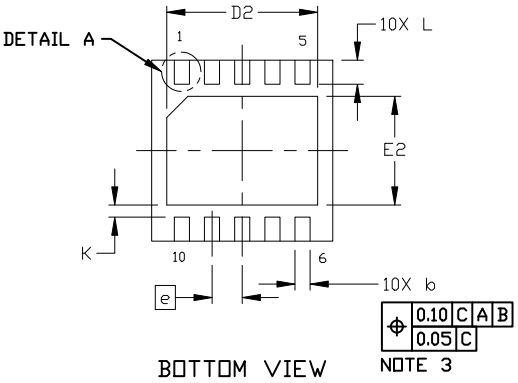
SCALE 2:1



TOP VIEW

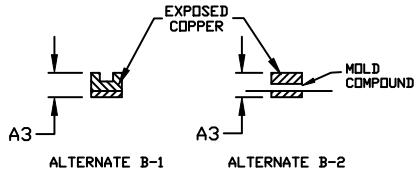


SIDE VIEW

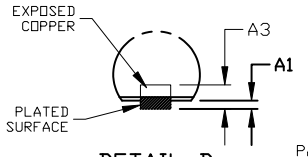


BOTTOM VIEW

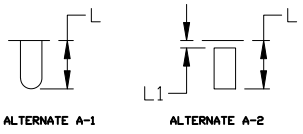
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

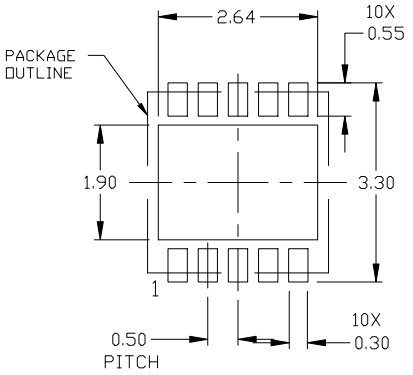


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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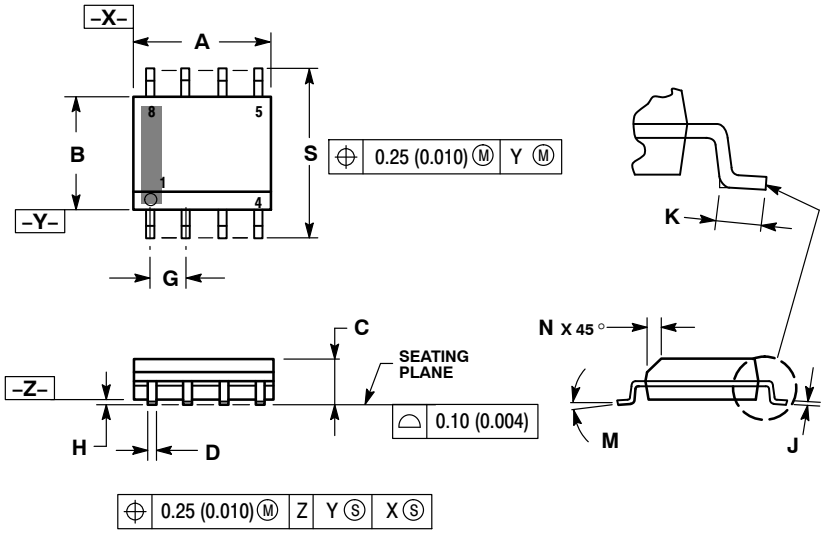
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

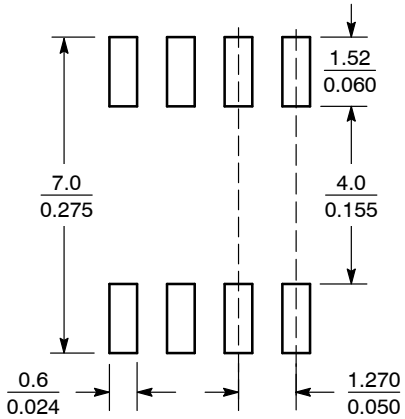
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

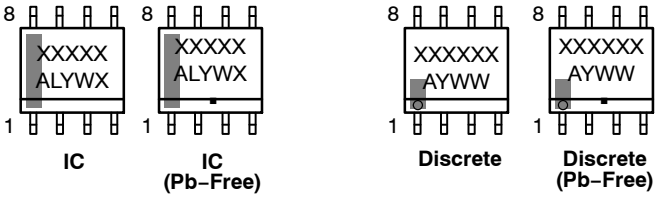
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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