NCP81151

MOSFET Driver, VR12.5 Compatible Synchronous Buck

The NCP81151 is a high performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. It can drive up to 3 nF load with a 25 ns propagation delay and 20 ns transition time.

Adaptive anti−cross−conduction and power saving operation circuit can provide a low switching loss and high efficiency solution for notebook systems.

The UVLO function guarantees the outputs are low when the supply voltage is low.

Features

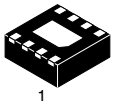
- Faster Rise and Fall Times
- Adaptive Anti−Cross−Conduction Circuit
- Zero Cross Detection function
- Output Disable Control Turns Off Both MOSFETs
- Undervoltage Lockout
- Power Saving Operation Under Light Load Conditions
- Direct Interface to NCP6131 and Other Compatible PWM Controllers
- Thermally Enhanced Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Management Solutions for Notebook Systems

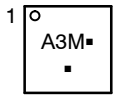
ON Semiconductor®

www.onsemi.com



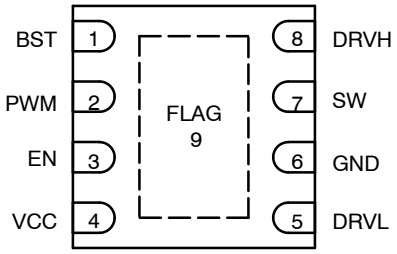
DFN8
CASE 506AA

MARKING DIAGRAM



A3 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCP81151MNTAG	DFN8 (Pb−Free)	3000 / Tape & Reel
NCP81151MNTBG	DFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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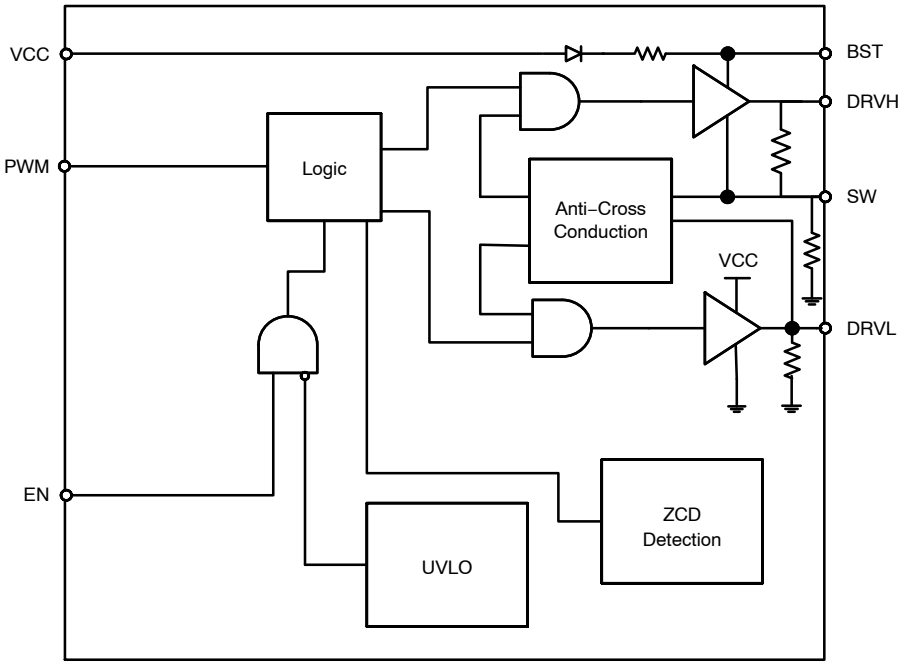


Figure 1. Block Diagram

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2	PWM	Control input. The PWM signal has three distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled.
3	EN	Logic input. A logic high to enable the part and a logic low to disable the part. Three states logic input: EN = High to enable the gate driver; EN = Low to disable the driver; EN = Mid to go into diode mode (both high and low side gate drive signals are low)
4	VCC	Power supply input. Connect a bypass capacitor (0.1 μF) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node.
7	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
8	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.

APPLICATION CIRCUIT

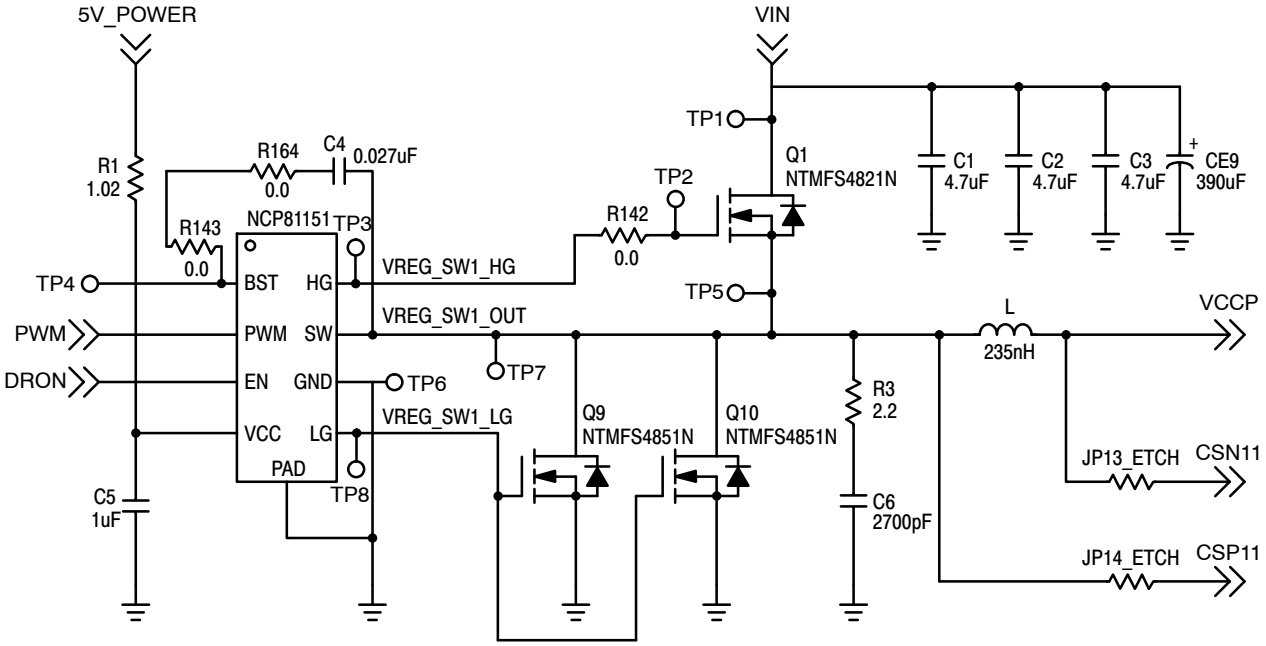


Figure 2. Application Circuit

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION

Symbol	Pin Name	V_{MAX}	V_{MIN}
V_{CC}	Main Supply Voltage Input	6.5 V	−0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 6.5 V wrt/ SW 7.7 V < 50 ns wrt/ SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	−5 V −10 V (200 ns)
DRVH	High Side Driver Output	BST + 0.3 V	−0.3 V wrt/SW −2 V (< 200 ns) wrt/SW
DRVL	Low Side Driver Output	V_{CC} + 0.3 V	−0.3 V DC −5 V (< 200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN	Enable Pin	6.5 V	−0.3 V
GND	Ground	0 V	0 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to AGND unless noted otherwise.

THERMAL INFORMATION

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Characteristic QFN Package (Note 1)	119	°C/W
T_J	Operating Junction Temperature Range (Note 2)	−40 to 150	°C
T_A	Operating Ambient Temperature Range	−40 to +100	°C
T_{STG}	Maximum Storage Temperature Range	−55 to +150	°C
MSL	Moisture Sensitivity Level − QFN Package	1	

*The maximum package power dissipation must be observed.
1. 1 in^2 Cu, 1 oz. thickness.
2. JESD 51−7 (1S2P Direct−Attach Method) with 1 LFM.

NCP81151 ELECTRICAL CHARACTERISTICS (−40°C < T_A < +100°C; 4.5 V < V_{CC} < 5.5 V, 4.5 V < BST−SWN < 5.5 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V, unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
VCC Operation Voltage		4.5		5.5	V
UNDERVOLTAGE LOCKOUT					
VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV
SUPPLY CURRENT					
Shutdown Mode	I_{CC} + I_{BST}, EN = GND		11	20	μA
Normal Mode	I_{CC} + I_{BST}, EN = 5 V, PWM = OSC		4.7		mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		0.9		mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		1.1		mA
BOOTSTRAP DIODE					
Forward Voltage	V_{CC} = 5 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT					
PWM Input High		3.4			V
PWM Mid−State		1.3		2.7	V
PWM Input Low				0.7	V
ZCD Blanking Timer			350		ns
HIGH SIDE DRIVER					
Output Impedance, Sourcing Current	V_{BST}−V_{SW} = 5 V		0.9	1.7	Ω
Output Impedance, Sinking Current	V_{BST}−V_{SW} = 5 V		0.7	1.7	Ω
DRVH Rise Time tr_{DRVH}	V_{CC} = 5 V, 3 nF load, V_{BST}−V_{SW} = 5 V		16	25	ns
DRVH Fall Time tf_{DRVH}	V_{CC} = 5 V, 3 nF load, V_{BST}−V_{SW} =5 V		11	18	ns
DRVH Turn−Off Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF	10		30	ns
DRVH Turn−On Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF	10		40	ns
SW Pulldown Resistance	SW to PGND		45		kΩ
DRVH Pulldown Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
LOW SIDE DRIVER					
Output Impedance, Sourcing Current			0.9	1.7	Ω
Output Impedance, Sinking Current			0.4	0.8	Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		16	25	ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		11	15	ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF	10		30	ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF	5.0		25	ns
DRVL Pulldown Resistance	DRVL to PGND, V_{CC} = PGND		45		kΩ

NCP81151 ELECTRICAL CHARACTERISTICS (−40°C < T_A < +100°C; 4.5 V < V_{CC} < 5.5 V, 4.5 V < BST−SWN < 5.5 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V, unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
EN INPUT					
Input Voltage High		3.3			V
Input Voltage Mid		1.35		1.8	V
Input Voltage Low				0.6	V
Input bias current		−1.0		1.0	μA
Propagation Delay Time			20	40	ns
SW NODE					
SW Node Leakage Current				20	μA
Zero Cross Detection Threshold Voltage			−6.0		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 1. DECODER TRUTH TABLE

Input	ZCD	DRVL	DRVH
PWM High (Enable High)	ZCD Reset	Low	High
PWM Mid (Enable High)	Positive Current Through the Inductor	High	Low
PWM Mid (Enable High)	Zero Current Through the Inductor	Low	Low
PWM Low (Enable High)	ZCD Reset	High	Low
Enable at Mid	X	Low	Low

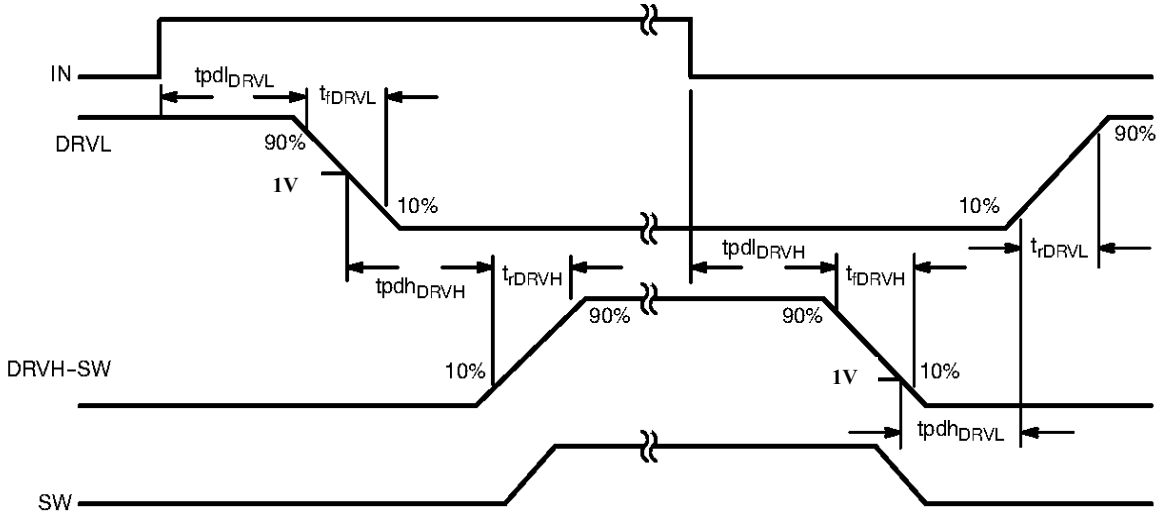


Figure 3.

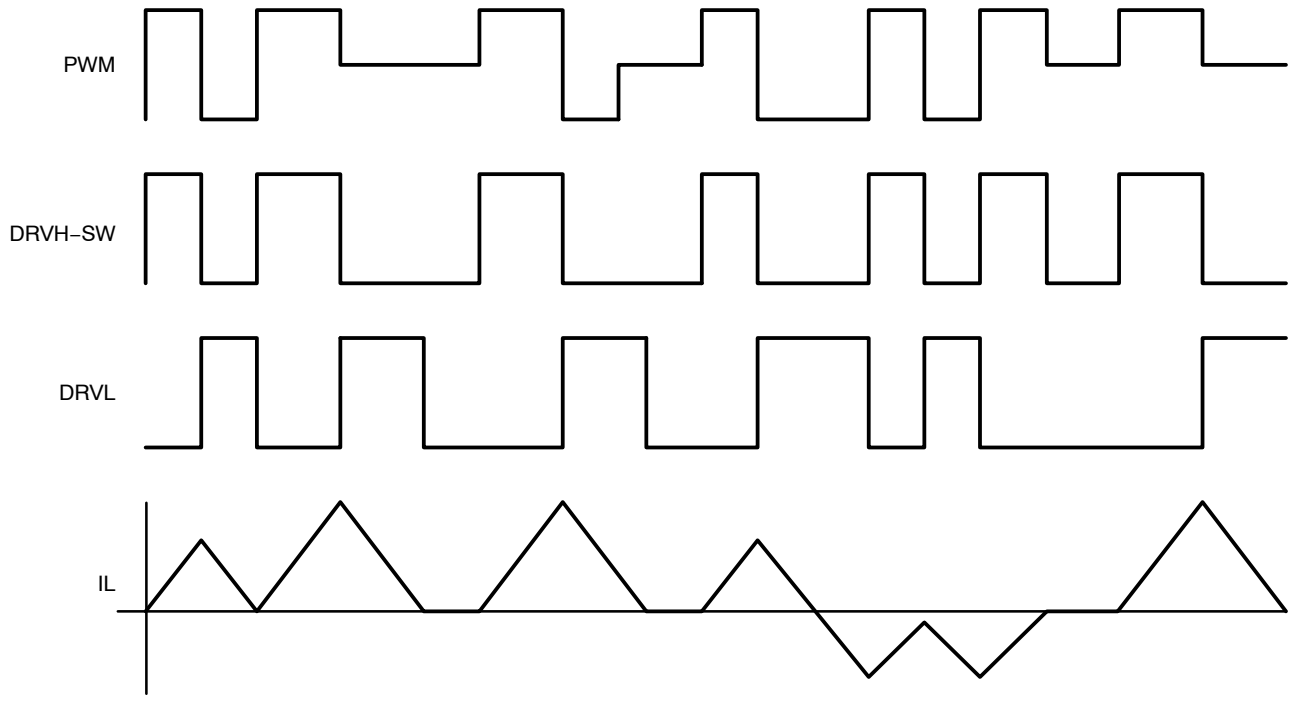


Figure 4. Timing Diagram

APPLICATION INFORMATION

The NCP81151 gate driver is a single phase MOSFET driver designed for driving N−channel MOSFETs in a synchronous buck converter topology. The NCP81151 is designed to work with ON Semiconductor's NCP6131 multi−phase controller. This gate driver is optimized for notebook applications.

Undervoltage Lockout

DRVH and DRVL are held low until V_{CC} reaches 4.5 V during startup. The PWM signal will control the gate status when V_{CC} threshold is exceeded.

Three−State EN Signal

When EN is set to the mid state, both DRVH and DRVL are set low, to force diode mode operation.

PWM Input and Zero Cross Detect (ZCD)

The PWM input, along with EN and ZCD, control the state of DRVH and DRVL.

When PWM is set high, DRVH will be set high after the adaptive non−overlap delay. When PWM is set low, DRVL will be set high after the adaptive non−overlap delay.

When PWM is set to the mid state, DRVH will be set low, and after the adaptive non−overlap delay, DRVL will be set high. DRVL remains high during the ZCD blanking time. When the timer has expired, the SW pin will be monitored for zero cross detection. After the detection, DRVL will be set low.

Adaptive Non−overlap

Adaptive dead time control is used to avoid shoot−through damage of the power MOSFETs. When the PWM signal pulls high, DRVL will be set low and the driver will monitor the gate voltage of the low side MOSFET. When the DRVL voltage falls below the gate threshold, DRVH will be set to high after the $tpdh_{DRVH}$ delay. When PWM is set low, the driver will monitor the gate voltage of the high side MOSFET. When the DRVH−SWN voltage falls below the top gate drive threshold, DRVL will be set to high after the $tpdh_{DRVL}$ delay.

Layout Guidelines

The layout for a DC−DC converter is very important. The bootstrap and V_{CC} bypass capacitors should be placed close to the driver IC.

Connect the GND pin to a local ground plane. The ground plane can provide a good return path for gate drives and reduce the ground noise. The thermal slug should be tied to the ground plane for good heat dissipation. To minimize the ground loop for the low side MOSFET, the driver GND pin should be close to the low−side MOSFET source pin. The gate drive trace should be routed to minimize its length. The minimum width is 20 mils.

Gate Driver Power Loss Calculation

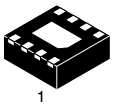
The gate driver power loss consists of the gate drive loss and quiescent power loss.

The equation below can be used to calculate the power dissipation of the gate driver. Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET.

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}\right) + I_{CC}\right] \times V_{CC} \quad \text{(eq. 1)}$$

Also shown is the standby dissipation factor (I_{CC} x V_{CC}) of the driver.

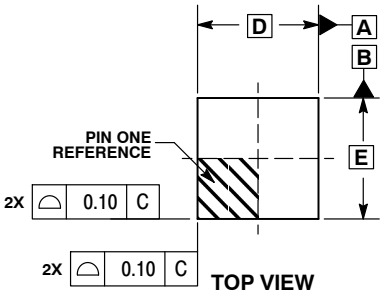
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

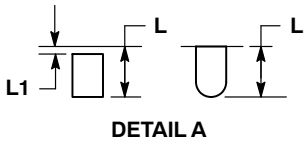


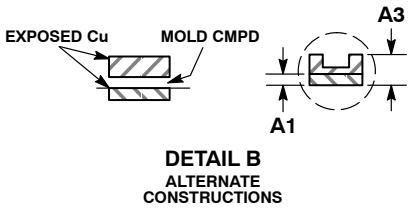
SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016

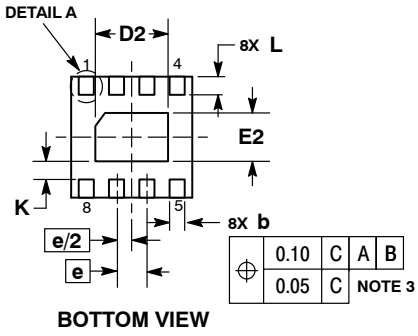




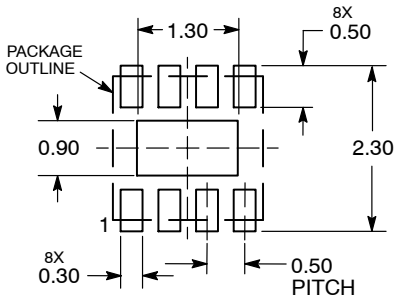


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3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10



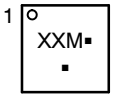
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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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