NCP81152

Synchronous Buck Dual MOSFET Driver

The NCP81152 is a high−performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. Two drivers are co−packaged into a 2.5 mm x 3.5 mm QFN16 package that greatly reduces the footprint compared to two discrete drivers. Adaptive anti−cross−conduction circuitry and power saving operation provides a low−switching−loss and high−efficiency solution for notebook systems. The under−voltage lockout function guarantees the outputs are low when the supply voltage is low.

Features

- Adaptive Anti−Cross−Conduction Circuit
- Integrated Bootstrap Diode
- Zero Cross Detection
- Floating Top Driver Accommodates Boost Voltages up to 35 V
- Output Disable Control Turns Off Both MOSFETs
- Under−voltage Lockout
- Power Saving Operation Under Light Load Conditions
- Thermally Enhanced Package
- These are Pb−Free Devices

Typical Applications

- Vcore Power for Notebook Systems
- Power Systems for DDR and Graphics

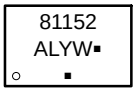
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QFN16
MN SUFFIX
CASE 485AW

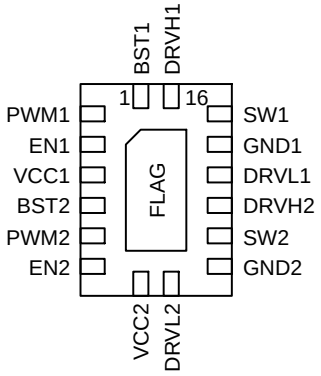
MARKING DIAGRAM



81152	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81152MNTWG	QFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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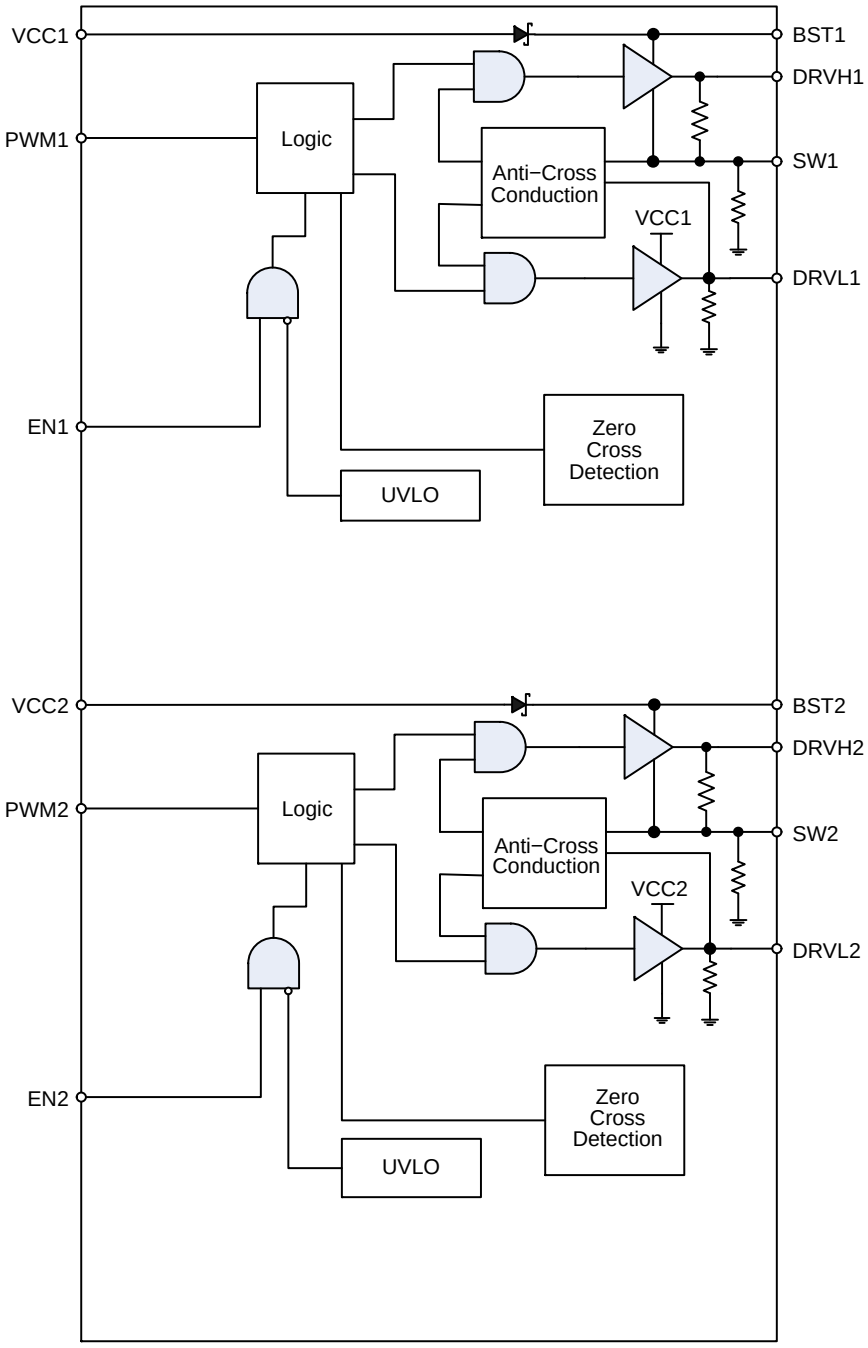


Figure 1. Block Diagram

Table 1. PIN DESCRIPTIONS

Pin No.	Symbol	Description
1, 5	BST1, BST2	Floating bootstrap supply pin for high−side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2, 6	PWM1, PWM2	Control input. The PWM signal has three states: PWM = High enables the high−side FET; PWM = Mid enables zero cross detection; PWM = Low enables the low−side FET.
3, 7	EN1, EN2	Logic input. Three−state logic input: EN = High enables the driver; EN = Mid goes into diode braking mode (both high−side and low−side gate drive signals are low); EN = Low disables the driver.
4, 8	VCC1, VCC2	Power supply input. Connect a bypass capacitor (0.1 μF) from this pin to ground.
9, 13	DRVL1, DRVL2	Low−side gate drive output. Connect to the gate of the low−side MOSFET.
10, 14	GND1, GND2	Bias and reference ground. All signals are referenced to this node.
11, 15	SW1, SW2	Switch node. Connect this pin to the source of the high−side MOSFET and drain of the low−side MOSFET.
12, 16	DRVH1, DRVH2	High−side gate drive output. Connect to the gate of the high−side MOSFET.
17	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
VCC1, VCC2	Main Supply Voltage Input	6.5 V	−0.3 V
BST1, BST2	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 6.5 V wrt/ SW	−0.3 V wrt/SW
SW1, SW2	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	−5 V −10 V (200 ns)
DRVH1, DRVH2	High Side Driver Output	BST+0.3 V	−0.3 V wrt/SW −2 V (<200 ns) wrt/SW
DRVL1, DRVL2	Low Side Driver Output	VCC+0.3 V	−0.3 V DC −5 V (<200 ns)
PWM1, PWM2	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN1, EN2	Enable Pin	6.5 V	−0.3 V
GND1, GND2	Ground	0 V	0 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to AGND unless noted otherwise.

Table 3. THERMAL INFORMATION

Parameter	Symbol	Value	Unit
Thermal Characteristic (Note 1)	$R_{\theta JA}$	29	°C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +100	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level − QFN Package	MSL	1	

*The maximum package power dissipation must be observed.
1. 1 in^2 Cu., 1 oz. thickness.

Table 4. NCP81152 DRIVER ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < +100°C; VCC = 4.5 V ~ 5.5 V; BST−SW = 4.5 V ~ 5.5 V; BST = 4.5 V ~ 30 V; SWN = 0 V ~ 21 V.

Parameter	Test Conditions	Min	Typ	Max	Units
SUPPLY VOLTAGE					
VCC1, VCC2 Operation Voltage		4.5		5.5	V
UNDERVOLTAGE LOCKOUT (VCC1, VCC2)					
Start Threshold		3.8	4.35	4.5	V
Hysteresis		150	200	250	mV
SUPPLY CURRENT					
Normal Mode	$I_{CC1} + I_{CC2} + I_{BST1} + I_{BST2}$ EN1, EN2 = 5 V, PWM1 & PWM2 oscillating at 100 kHz, C_{LOAD} = 3 nF		9.4		mA
Shutdown Mode	$I_{CC1} + I_{CC2} + I_{BST1} + I_{BST2}$ EN1, EN2 = Gnd		22	40	μA
Standby Current 1	$I_{CC1} + I_{CC2} + I_{BST1} + I_{BST2}$ EN1, EN2 = Logic High, PWM1, PWM2 = Logic Low, No loading on DRVH1/2 & DRVL1/2		1.8		mA
Standby Current 2	$I_{CC1} + I_{CC2} + I_{BST1} + I_{BST2}$ EN1, EN2 = Logic High, PWM1, PWM2 = Logic High, No loading on DRVH1/2 & DRVL1/2		2.2		mA
BOOTSTRAP DIODE					
Forward Voltage	VCC = 5 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT					
Input High		3.4			V
Mid−State		1.3		2.45	V
Input Low				0.7	V
ZCD blanking timer			350		ns
HIGH SIDE DRIVER (DRVH1, DRVH2)					
Output Resistance, Sourcing Current	BST − SW = 5 V		0.9	1.7	Ω
Output Resistance, Sinking Current	BST − SW = 5 V		0.7	1.7	Ω
Rise Time, tr_{DRVH}	VCC = 5 V, 3 nF load, BST − SW = 5 V		16	25	ns
Fall Time, tf_{DRVH}	VCC = 5 V, 3 nF load, BST − SW = 5 V		11	18	ns
Turn−Off Propagation Delay, $tpdl_{DRVH}$	C_{LOAD} = 3 nF	10		30	ns
Turn−On Propagation Delay, $tpdh_{DRVH}$	C_{LOAD} = 3 nF	10		40	ns
SW Pull−Down Resistance	SW to PGND		45		kΩ
DRVH Pull−Down Resistance	DRVH to SW, V_{BST}−V_{SW} = 0 V		45		kΩ
LOW SIDE DRIVER (DRVL1, DRVL2)					
Output Resistance, Sourcing Current			0.9	1.7	Ω
Output Resistance, Sinking Current			0.4	0.8	Ω
Rise Time, tr_{DRVH}	C_{LOAD} = 3 nF		16	25	ns
Fall Time, tf_{DRVH}	C_{LOAD} = 3 nF		11	15	ns
Turn−Off Propagation Delay, $tpdl_{DRVH}$	C_{LOAD} = 3 nF	10		30	ns
Turn−On Propagation Delay, $tpdh_{DRVH}$	C_{LOAD} = 3 nF	5		25	ns
DRVL Pull−Down Resistance	DRVL to PGND, VCC = PGND		45		kΩ

Table 4. NCP81152 DRIVER ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < +100°C; VCC = 4.5 V ~ 5.5 V; BST−SW = 4.5 V ~ 5.5 V; BST = 4.5 V ~ 30 V; SWN = 0 V ~ 21 V.

Parameter	Test Conditions	Min	Typ	Max	Units
ENABLE INPUT (EN1, EN2)					
Input High		3.3			V
Mid−State		1.35		1.8	V
Input Low				0.6	V
Normal Mode Bias Current		−1		1	μA
Propagation Delay Time			20	40	ns
SWITCH NODE (SW1, SW2)					
SW Leakage Current				20	μA
Zero Cross Detection Threshold Voltage	SW to −20 mV, ramp slowly until BG goes off		−6		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. PWM/EN TRUTH TABLE

PWM INPUT	ZCD	DRVL	DRVH
PWM High	ZCD Reset	Low	High
PWM Mid	Positive current through the inductor	High	Low
PWM Mid	Zero or negative current through the inductor	Low	Low
PWM Low	ZCD Reset	High	Low
Enable at Mid	X	Low	Low

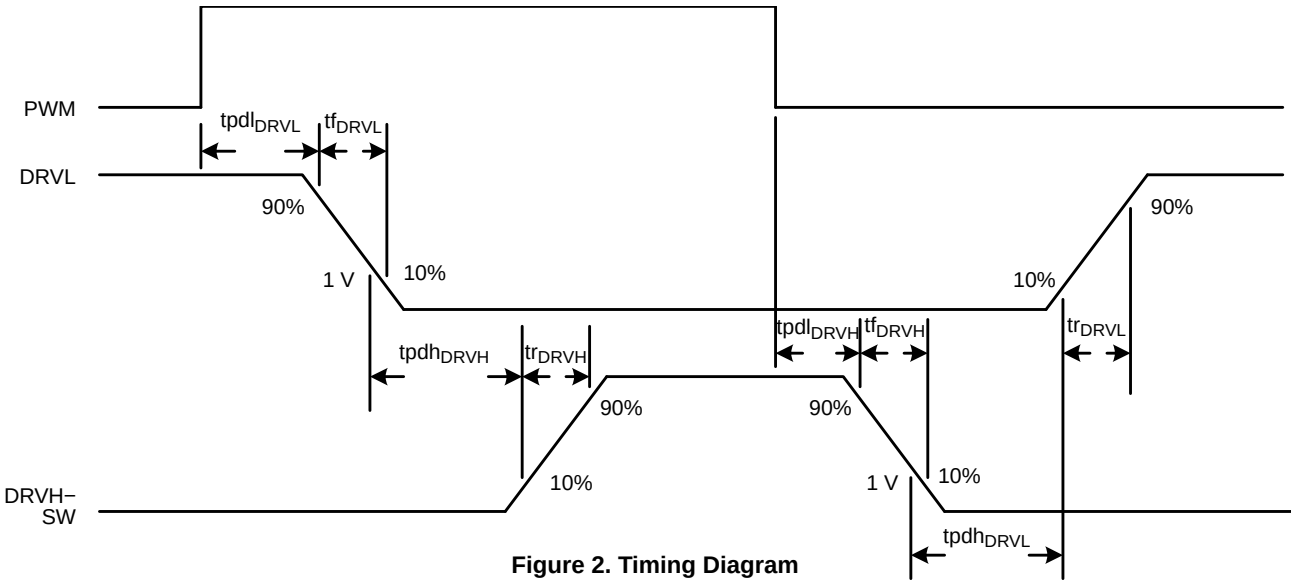


Figure 2. Timing Diagram

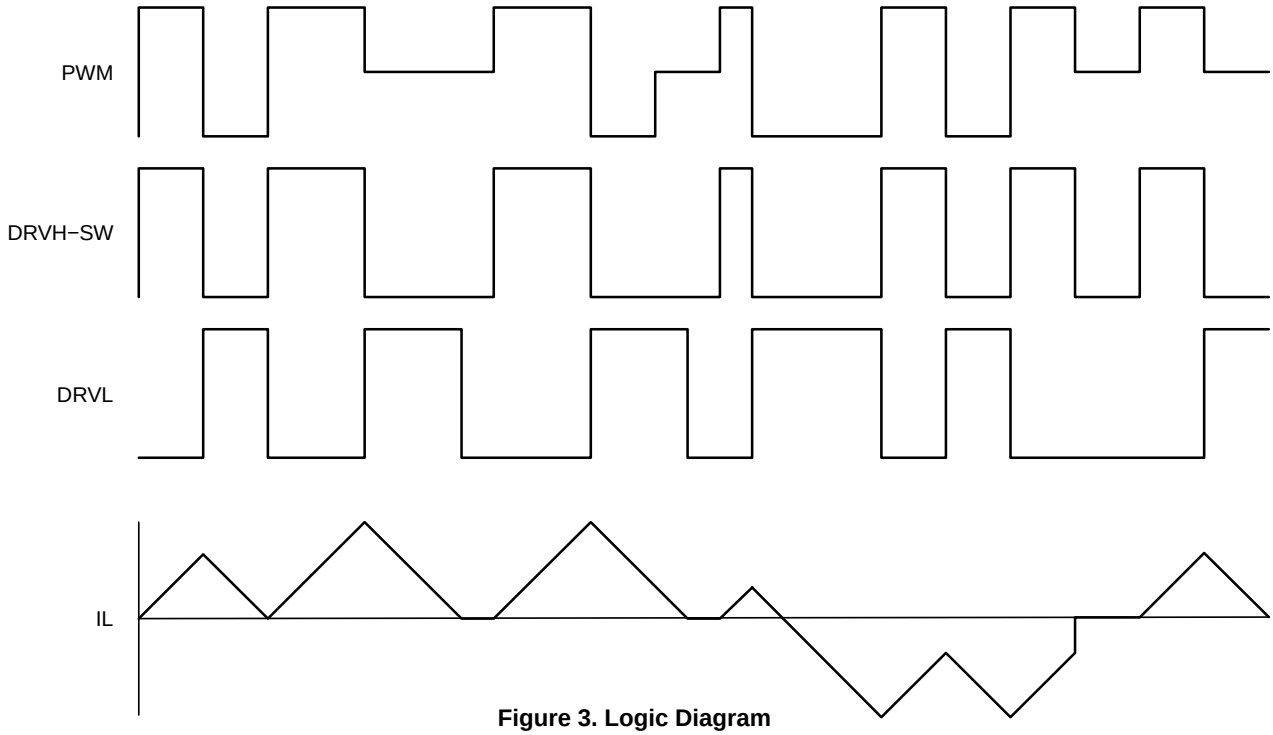


Figure 3. Logic Diagram

Application Information

The NCP81152 is a high−performance dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. Two drivers are co−packaged into a 2.5 mm x 3.5 mm QFN16 package that greatly reduces the footprint compared to two discrete drivers.

Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. When VCC reaches this threshold, the PWM signal controls the states of DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull−down resistors on DRVH, DRVL and SW that prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

Three−State EN Signal

Placing EN into a logic−high or logic−low turns the driver on and off, respectively, as long as VCC is greater than the UVLO threshold. The EN threshold limits are specified in the electrical characteristics table in this datasheet. Setting the EN voltage to a mid−state level pulls both DRVH and DRVL low.

Setting EN to the mid−state level can be used for body diode braking to quickly reduce the inductor current. By turning the LS FET off and having the current conduct through the LS FET body diode, the voltage at the switch node is at a greater negative potential compared to having the LS FET on. This greater negative potential on switch node allows there to be a greater voltage across the output inductor, since the opposite terminal of the inductor is connected to the converter output voltage. The larger voltage across the inductor causes there to be a greater inductor current slew rate, allowing the current to decrease at a faster rate.

PWM Input and Zero Cross Detect (ZCD)

The PWM input, along with EN and ZCD, controls the state of DRVH and DRVL. When PWM is set high, DRVH is set high after the adaptive non−overlap delay. When PWM is set low, DRVL is set high after the adaptive non−overlap delay.

When PWM is set to the mid−state, DRVH is set low, and after the adaptive non−overlap delay, DRVL is set high. DRVL remains high until the ZCD blanking time expires. When the timer expires, the voltage on the SW pin is monitored for zero cross detection (whether it has crossed the ZCD threshold voltage). After zero cross is detected, DRVL is set low.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low−$R_{DS(on)}$ N−channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCC and GND pins.

High−Side Driver

The high−side driver is designed to drive a floating low−$R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81152 is starting up, the SW pin is held at ground, allowing the bootstrap capacitor to charge up to VCC through the bootstrap diode. When the PWM input is driven high, the high−side driver turns on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin rises. When the high−side MOSFET fully turns on, SW settles to VIN and BST settles to VIN + VCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used for C_{BST}.

Thermal Considerations

As power in the NCP81152 increases, it may be necessary to provide thermal relief. The maximum power dissipation supported by the device depends upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81152 has good thermal conductivity through the PCB, the junction temperature is relatively low with high power applications. The maximum dissipation the NCP81152 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, the NCP81152, soldered on to a 645 mm^2 copper area, using 1 oz. copper and FR4, can dissipate up to 4.3 W when the ambient temperature (T_A) is 25°C. The power dissipated by the NCP81152 can be calculated from the following equation:

$$P_D \approx VCC \cdot \left[(n_{HS} \cdot Qg_{HS} + n_{LS} \cdot Qg_{LS}) \cdot f + I_{standby}\right] \qquad \text{(eq. 2)}$$

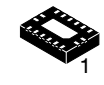
Where n_{HS} and n_{LS} are the number of high−side and low−side FETs, respectively, Qg_{HS} and Qg_{LS} are the gate charges of the high−side and low−side FETs, respectively and *f* is the switching frequency of the converter.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

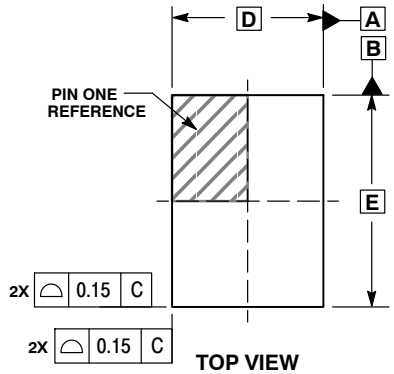
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CASE 485AW−01
ISSUE O

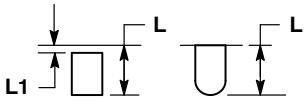
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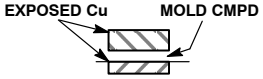
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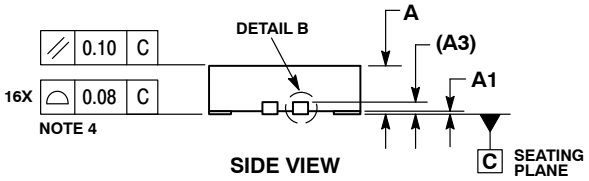
TOP VIEW



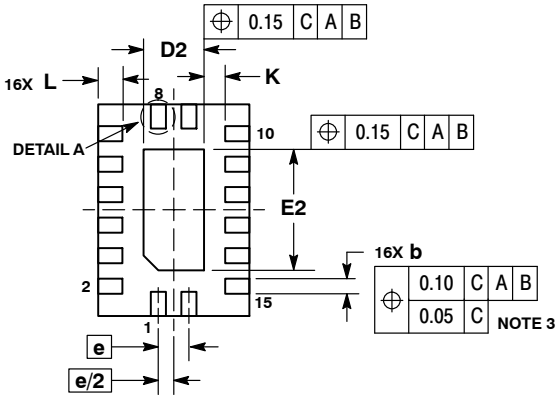
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERAL MARKING DIAGRAM*

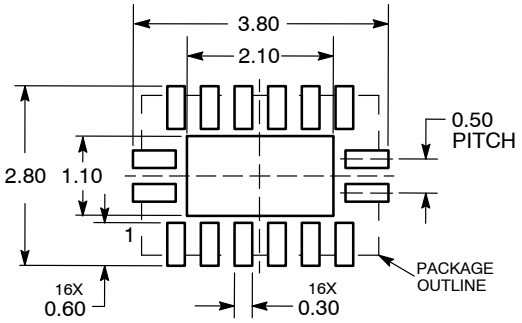


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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