NCP81158

Synchronous Buck MOSFET Driver

The NCP81158 is a high−performance dual MOSFET gate driver in a small 3 mm x 3 mm package, optimized to drive the gates of both high−side and low−side power MOSFETs in a synchronous buck converter. The driver outputs can be placed into a high−impedance state via the tri−state PWM and EN inputs. The NCP81158 comes packaged with an integrated boost diode to minimize external components. A VCC UVLO function guarantees the outputs are low when the supply voltage is low.

Features

- Space−efficient 3 mm x 3 mm DFN8 thermally−enhanced Package
- VCC Range of 4.5 V to 5.5 V
- Internal Bootstrap Diode
- 5 V 3−stage PWM Input
- Diode Braking Capability via EN Mid−state
- Adaptive Anti−cross Conduction Circuit Protects Against Cross−conduction during FET Turn−on and Turn−off
- Output Disable Control Turns Off Both MOSFETs via Enable Pin
- VCC Undervoltage Lockout
- These Devices are Pb−free, Halogen−free/BFR−free and are RoHS Compliant

Typical Applications

- Power Solutions for Notebook and Desktop Systems

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DFN8
CASE 506BJ

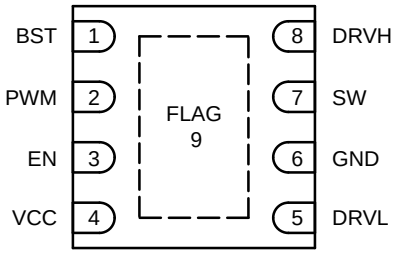
MARKING DIAGRAM



81158	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCP81158MNTXG	DFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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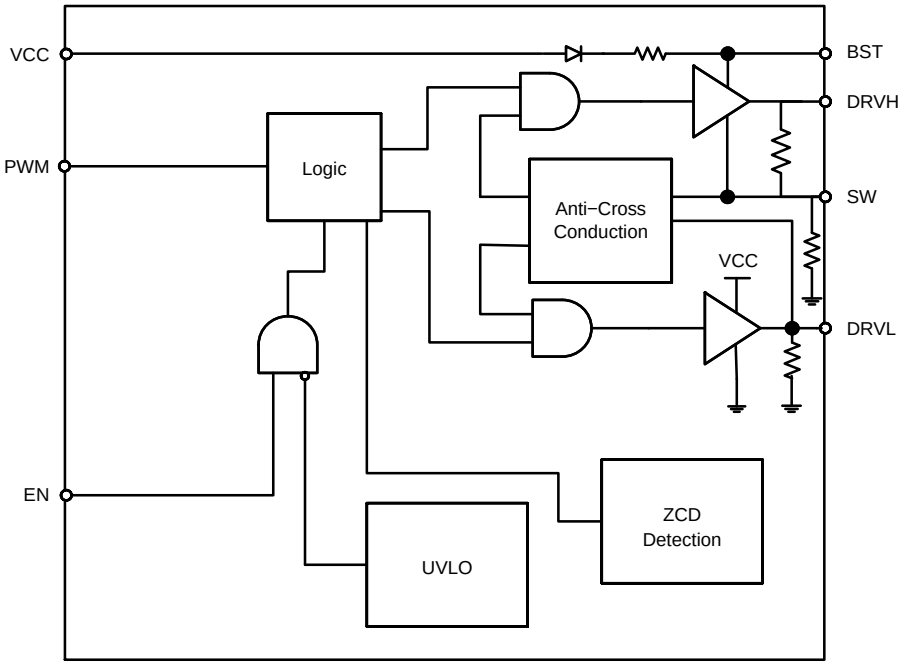


Figure 1. Block Diagram

PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2	PWM	Control input. The PWM signal has three distinctive states: Low = Low Side FET Enabled, Mid = Diode Emulation Enabled, High = High Side FET Enabled.
3	EN	Logic input. A logic high to enable the part and a logic low to disable the part. Three states logic input: EN = High to enable the gate driver; EN = Low to disable the driver; EN = Mid to go into diode mode (both high and low side gate drive signals are low)
4	VCC	Power supply input. Connect a bypass capacitor (0.1 μF) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node.
7	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
8	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.

APPLICATION CIRCUIT

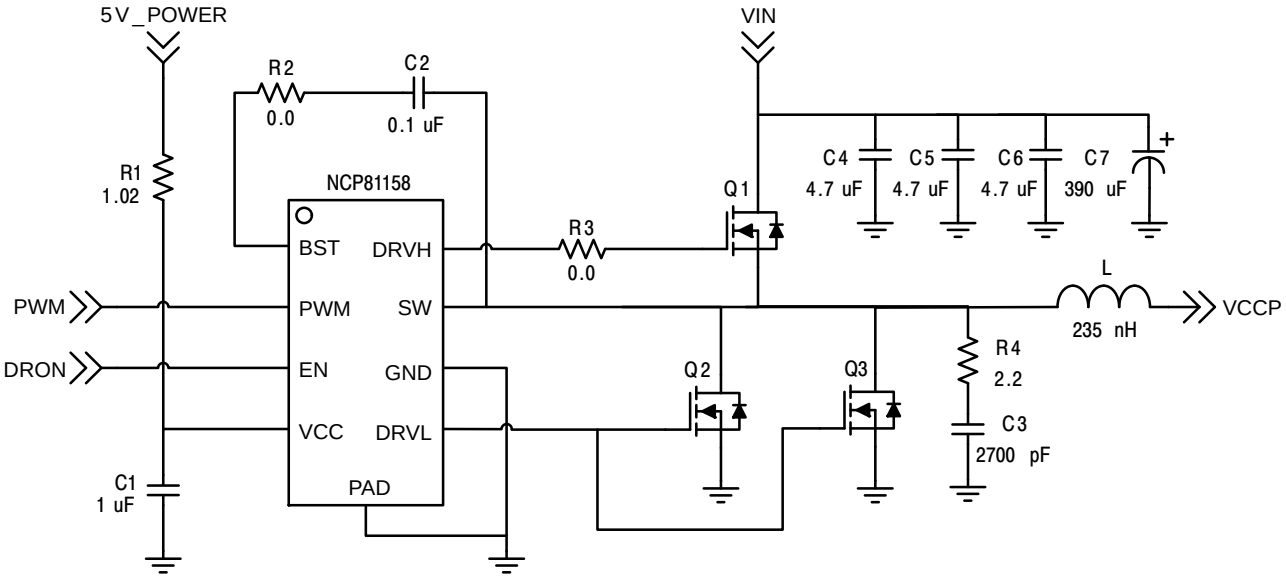


Figure 2. Application Circuit

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL INFORMATION

Symbol	Pin Name	V_{MAX}	V_{MIN}
V_{CC}	Main Supply Voltage Input	6.5 V 7.5 V < 80 ns	−0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 6.5 V wrt/ SW 7.7 V < 50 ns wrt/ SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 80 ns	−5 V −10 V (200 ns)
DRVH	High Side Driver Output	BST + 0.3 V SW + 7 V (< 80 ns)	−0.3 V wrt/SW −2 V (< 200 ns) wrt/SW
DRVL	Low Side Driver Output	V_{CC} + 0.3 V 7 V (< 80 ns)	−0.3 V DC −5 V (< 200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN	Enable Pin	6.5 V	−0.3 V
GND	Ground	0 V	0 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to AGND unless noted otherwise.

THERMAL INFORMATION

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Characteristic QFN Package (Note 1)	119	°C/W
T_J	Operating Junction Temperature Range (Note 2)	−40 to 150	°C
T_A	Operating Ambient Temperature Range	−40 to +100	°C
T_{STG}	Maximum Storage Temperature Range	−55 to +150	°C
MSL	Moisture Sensitivity Level − QFN Package	1	

*The maximum package power dissipation must be observed.
1. 1 in^2 Cu, 1 oz. thickness.
2. JESD 51−7 (1S2P Direct−Attach Method) with 1 LFM.

NCP81158 ELECTRICAL CHARACTERISTICS ($-40°C < T_A < +100°C$; $4.5\ V < V_{CC} < 5.5\ V$, $4.5\ V < BST-SWN < 5.5\ V$, $4.5\ V < BST < 30\ V$, $0\ V < SWN < 21\ V$, unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
VCC Operation Voltage		4.5		5.5	V
UNDERVOLTAGE LOCKOUT					
VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV
SUPPLY CURRENT					
Shutdown Mode	$I_{CC} + I_{BST}$, EN = GND		1.0	2.0	μA
Normal Mode	$I_{CC} + I_{BST}$, EN = 5 V, PWM = OSC		4.7		mA
Standby Current	$I_{CC} + I_{BST}$, EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		0.9		mA
Standby Current	$I_{CC} + I_{BST}$, EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		1.1		mA
BOOTSTRAP DIODE					
Forward Voltage	V_{CC} = 5 V, forward bias current = 2 mA	0.1	0.4	0.6	V

NCP81158 ELECTRICAL CHARACTERISTICS (−40°C < T_A < +100°C; 4.5 V < V_{CC} < 5.5 V, 4.5 V < BST−SWN < 5.5 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V, unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
PWM INPUT					
PWM Input High		3.4			V
PWM Mid−State		1.3		2.7	V
PWM Input Low				0.7	V
ZCD Blanking Timer			350		ns
HIGH SIDE DRIVER					
Output Impedance, Sourcing Current	V_{BST}−V_{SW} = 5 V		0.9	1.7	Ω
Output Impedance, Sinking Current	V_{BST}−V_{SW} = 5 V		0.7	1.7	Ω
DRVH Rise Time tr_{DRVH}	V_{CC} = 5 V, 3 nF load, V_{BST}−V_{SW} = 5 V		16	25	ns
DRVH Fall Time tf_{DRVH}	V_{CC} = 5 V, 3 nF load, V_{BST}−V_{SW} =5 V		11	18	ns
DRVH Turn−Off Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF	10		30	ns
DRVH Turn−On Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF	10		40	ns
SW Pulldown Resistance	SW to PGND		45		kΩ
DRVH Pulldown Resistance	DRVH to SW, BST−SW = 0 V		45		kΩ
LOW SIDE DRIVER					
Output Impedance, Sourcing Current			0.9	1.7	Ω
Output Impedance, Sinking Current			0.4	0.8	Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		16	25	ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		11	15	ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF	10		30	ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF	5.0		25	ns
DRVL Pulldown Resistance	DRVL to PGND, V_{CC} = PGND		45		kΩ
EN INPUT					
Input Voltage High		3.3			V
Input Voltage Mid		1.35		1.8	V
Input Voltage Low				0.6	V
Input bias current		−1.0		1.0	μA
Propagation Delay Time			20	40	ns
SW NODE					
SW Node Leakage Current				20	μA
Zero Cross Detection Threshold Voltage			−6.0		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 1. DECODER TRUTH TABLE

Input	ZCD	DRVL	DRVH
PWM High (Enable High)	ZCD Reset	Low	High
PWM Mid (Enable High)	Positive Current Through the Inductor	High	Low
PWM Mid (Enable High)	Zero Current Through the Inductor	Low	Low
PWM Low (Enable High)	ZCD Reset	High	Low
Enable at Mid	X	Low	Low

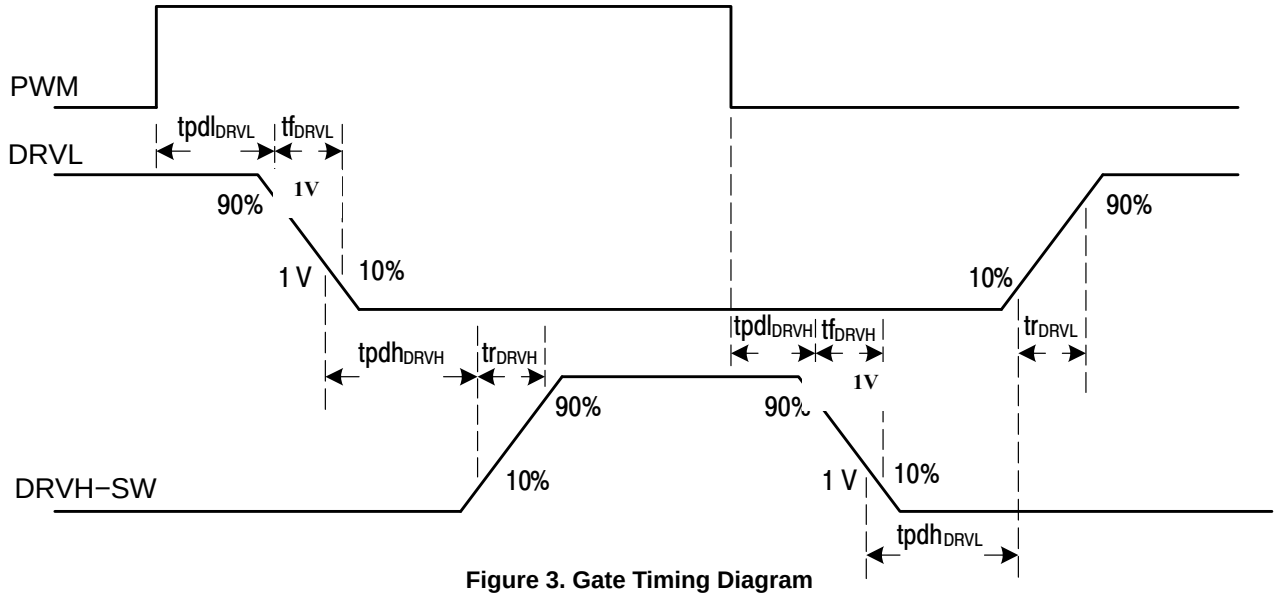


Figure 3. Gate Timing Diagram

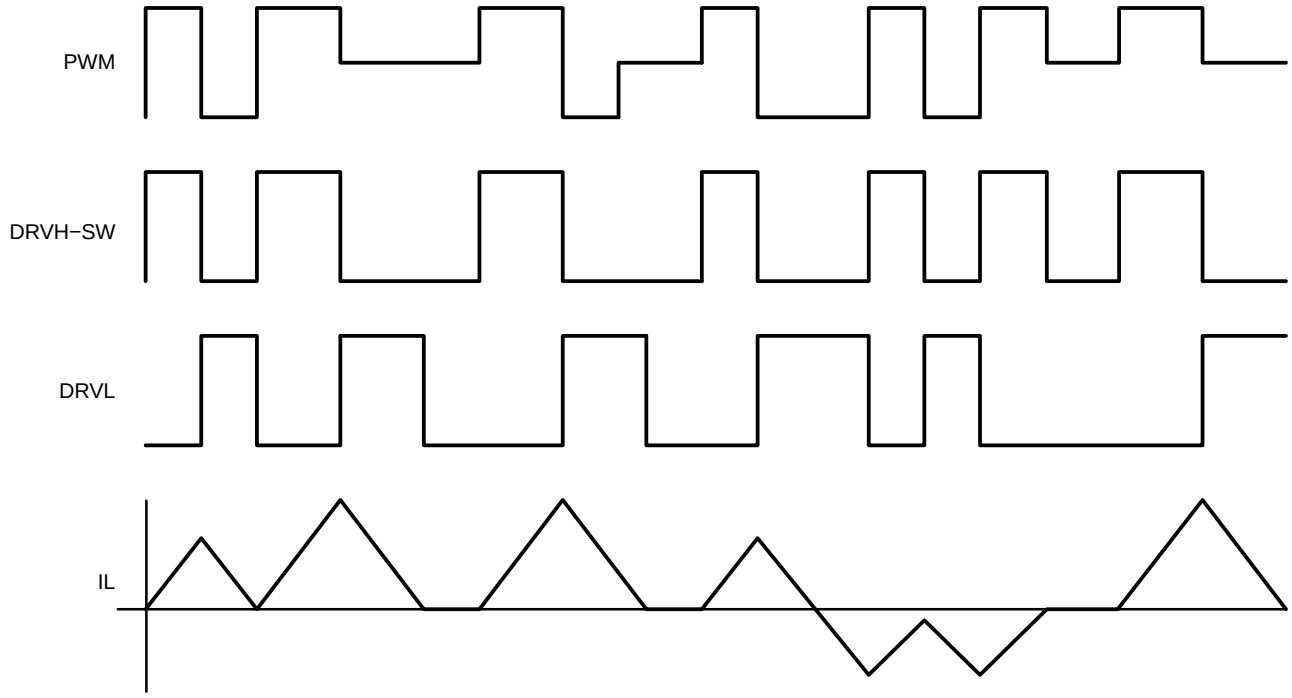


Figure 4. Timing Diagram

APPLICATION INFORMATION

The NCP81158 gate driver is a single−phase MOSFET driver designed for driving N−channel MOSFETs in a synchronous buck converter topology.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low−$R_{DS(on)}$ N−channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCC and GND pins.

High−Side Driver

The high−side driver is designed to drive a floating low−$R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81158 is starting up, the SW pin is held at ground, allowing the

bootstrap capacitor to charge up to VCC through the bootstrap diode. When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin rises. When the high−side MOSFET is fully turned on, SW will settle to VIN and BST will settle to VIN + VCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used for C_{BST}.

Power Supply Decoupling

The NCP81158 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage, a low−ESR capacitor should be placed near the VCC and GND pins. A MLCC between 1 μF and 4.7 μF is typically used.

Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull−down resistors on DRVH, DRVL and SW to prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

Three−State EN Input

Placing EN into a logic−high and logic−low will turn the driver on and off, respectively, as long as VCC is greater than the UVLO threshold. The EN threshold limits are specified in the electrical characteristics table in this datasheet. Setting the voltage on EN to a mid−state level will pull both DRVH and DRVL low.

Setting EN to the mid−state level can be used for body diode braking to quickly reduce the inductor current. By turning the LS FET off and having the current conduct through the LS FET body diode, the voltage at the switch node will be at a greater negative potential compared to having the LS FET on. This greater negative potential on switch node allows there to be a greater voltage across the output inductor, since the opposite terminal of the inductor is connected to the converter output voltage. The larger voltage across the inductor causes there to be a greater inductor current slew rate, allowing the current to decrease at a faster rate.

Three−State PWM Input

Switching PWM between logic−high and logic−low states will allow the driver to operate in continuous conduction mode as long as VCC is greater than the UVLO threshold and EN is high. The threshold limits are specified in the electrical characteristics table in this datasheet. Refer to Figure 21 for the gate timing diagrams and Table 1 for the EN/PWM logic table.

When PWM is set above PWM_{HI}, DRVL will first turn off after a propagation delay of $tpdl_{DRVL}$. To ensure non−overlap between DRVL and DRVH, there is a delay of $tpdh_{DRVH}$ from the time DRVL falls to 1 V, before DRVH is allowed to turn on.

When PWM falls below PWM_{LO}, DRVH will first turn off after a propagation delay of $tpdl_{DRVH}$. To ensure non−overlap between DRVH and DRVL, there is a delay of $tpdh_{DRVL}$ from the time DRVH – SW falls to 1 V, before DRVL is allowed to turn on.

When PWM enters the mid−state voltage range, DRVL goes high after the non−overlap delay, and stays high for the duration of the ZCD blanking + debounce timers. Once these timers expire, SW is monitored for zero current detection and pulls DRVL low once zero current is detected.

Thermal Considerations

As power in the NCP81158 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81158 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP81158 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, the NCP81158, soldered on to a 645 mm^2 copper area, using 1 oz. copper and FR4, can dissipate up to 1.05 W when the ambient temperature (T_A) is 25°C. The power dissipated by the NCP81158 can be calculated from the following equation:

$$P_D \approx VCC \cdot \left[\left(n_{HS} \cdot Qg_{HS} + n_{LS} \cdot Qg_{LS}\right) \cdot f + I_{standby}\right] \qquad \text{(eq. 2)}$$

Where n_{HS} and n_{LS} are the number of high−side and low−side FETs, respectively, Qg_{HS} and Qg_{LS} are the gate charges of the high−side and low−side FETs, respectively and *f* is the switching frequency of the converter.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

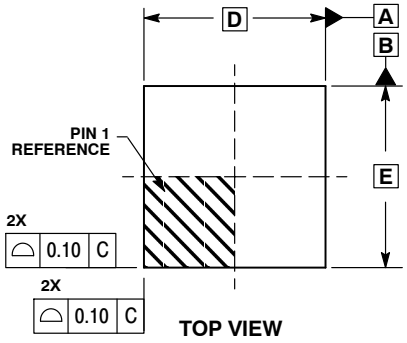
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CASE 506BJ−01
ISSUE O

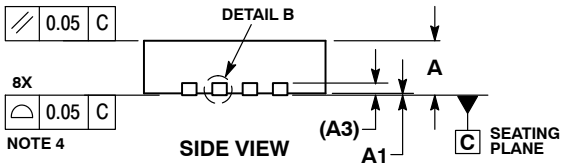
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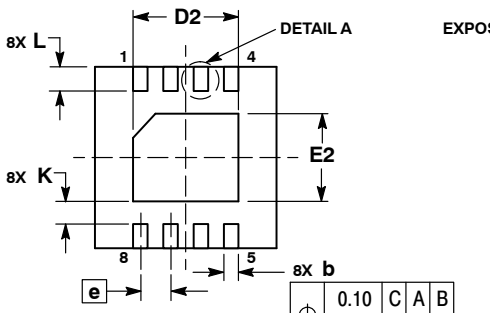
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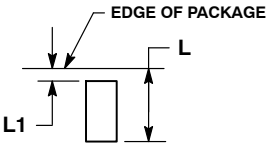
TOP VIEW



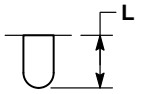
SIDE VIEW



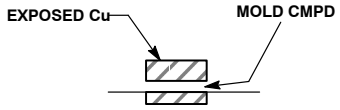
BOTTOM VIEW



DETAIL A
OPTIONAL
CONSTRUCTION



DETAIL A
OPTIONAL
CONSTRUCTION



DETAIL B
OPTIONAL
CONSTRUCTION

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.64	1.84
E	3.00 BSC	
E2	1.35	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

GENERIC MARKING DIAGRAM*

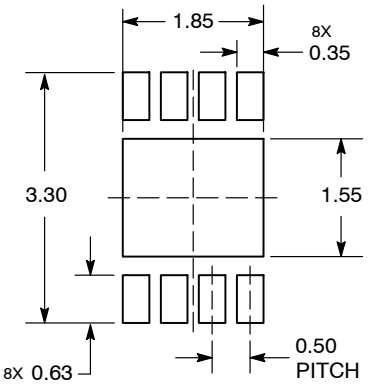


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN8 3X3, 0.5P**	**PAGE 1 OF 1**

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