NCS3402

Dual Nano-power Open Drain Output Comparator

The NCS3402 is a nano−power comparator consuming only 470 nA per channel supply current, which make this device ideal for battery power and wireless handset applications.

The NCS3402 has a minimum operating supply voltage of 2.7 V over the extended industrial temperature range (T_A = −40°C to 125°C), while having an input common−mode range of −0.1 to V_{DD} + 5 V.

The ultra low supply current makes the NCS3402 an ideal choice for battery powered and portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an over−current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

Features

- Low Supply Current: 470 nA/Per Channel
  - Input Common−Mode Range exceeds the rails
  - −0.1 V to VDD + 5 V
- Supply Voltage Range: 2.7 V to 16 V
- Reverse Battery Protection Up to 18 V
- Open Drain CMOS Output Stage
- Specified Temperature Range
  - −40°C to 125°C
- This is a Pb−Free Device

Typical Applications

- Voltage Sense Circuit
- PSU Monitoring Circuit
- Wireless Handsets
- Portable Medical Equipment

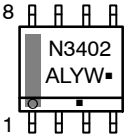
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http://onsemi.com

MARKING DIAGRAMS



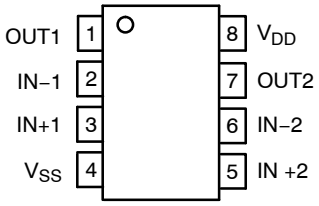
SOIC−8
D SUFFIX
CASE 751



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT1	Channel 1 Output
2	IN−1	Channel 1 Inverting Input
3	IN+2	Channel 2 Non−Inverting Input
4	V_{SS}	Negative Power Supply
5	IN+2	Channel 2 Non−Inverting Input
6	IN−2	Channel 2 Inverting Input
7	OUT2	Channel 2 Output
8	V_{DD}	Positive Power Supply

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	17	V
Differential Input Voltage	V_{ID}	±20	V
Input Voltage Range (Notes 1 and 2)	V_{IN}	0 to V_{CC} + 5	V
Input Current Range	I_{IN}	±10	mA
Output Current Range	Io	±10	mA
Operating Free−Air Temperature Range	T_A	−40 to +125	°C
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature 1.6 mm (1/16 inch) from case for 10 seconds	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. All voltage values, except differential voltages, are respect to GND
2. Input voltage range is limited to 20V or V_{CC} +5 V whichever is smaller

ESD RATINGS

Rating	Symbol	Value	Unit
Human Body Model	HBM	2000	V
Machine Model	MM	200	V

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics Thermal Resistance, Junction−to−Air SOIC8	$R_{\theta JA}$	176	°C/W

3. Power dissipation must be considered to ensure the maximum junction temperature (θ_{JA}) is not exceeded.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Min	Max	Unit
Supply voltage	V_{DD}	Single supply	2.7	16	V
		Split supply	±1.35	±8	
Common−mode input voltage range	V_{ICR}		−0.1	V_{DD}+5	V
Operating free−air temperature	T_A		− 40	125	°C

DC PERFORMANCE ELECTRICAL CHARACTERISTICS AT SPECIFIED OPERATING FREE−AIR TEMPERATURE, V_S = 2.7 V, 5 V, 15 V (unless otherwise noted)

Parameter	Symbol	Testing Conditions	T_A	Min	Typ	Max	Unit
Input offset voltage	V_{IO}	$V_{CM} = V_S/2$, R_S = 50 Ω, R_P = 1 MΩ	25°C		250	3600	μV
			Full range			4400	
Offset voltage drift	ΔV_{IO}		25°C		3		μV/°C
Common−mode rejection ratio	CMRR	V_{CM} = 0 to 2.7 V, R_S = 50 Ω	25°C	55	72		dB
			Full range	50			
		V_{CM} = 0 to 5 V, R_S = 50 Ω	25°C	60	76		
			Full range	55			
		V_{CM} = 0 to 15 V, R_S = 50 Ω	25°C	65	88		
			Full range	60			
Large−signal differential voltage amplification	A_{VD}	R_P = 1 MΩ	25°C		1000		V/mV

INPUT/OUTPUT CHARACTERISTICS SPECIFIED OPERATING FREE−AIR TEMPERATURE, V_S = 2.7 V, 5 V, 15 V (unless otherwise noted)

Input offset current (Note 4)	I_{IO}	$V_{CM} = V_S/2$, R_P = 1 MΩ, R_S = 50 Ω	25°C		20	100	pA
			Full range			1000	
Input bias current (Note 4)	I_{IB}		25°C		80	250	pA
			Full range			3000	
Differential input resistance	R_{ID}	$V_{in} = V_S/2$	25°C		300		MΩ
High−impedance output leakage current	I_{OZ}	$V_{CM} = V_S/2$, $V_O = V_{CC}$, V_{ID} = 1 V	25°C		50		pA
Low−level output voltage	V_{OL}	$V_{CM} = V_S/2$, I_{OL} = 2 μA, V_{ID} = −1 V	25°C		8		mV
		$V_{CM} = V_S/2$, I_{OL} = 50 μA, V_{ID} = −1 V	25°C		80	200	
			Full range			300	

POWER SUPPLY SPECIFIED OPERATING FREE−AIR TEMPERATURE, V_{CC} = 2.7 V, 5 V, 15 V (unless otherwise noted)

Supply current (per channel)	I_{CC}	R_P = No pullup	Output state low	25°C		470	550	nA
				Full range			750	
			Output state high	25°C		560	640	
				Full range			950	
Power supply rejection ratio	PSRR	$V_{CM} = V_S/2$, No load	V_{CC} = 2.7 V to 5 V	25°C	75	100		dB
				Full range	70			
			V_{CC} = 5 V to 15 V	25°C	85	105		
				Full range	80			

4. Guaranteed by design or characterization.

SWITCHING CHARACTERISTICS AT RECOMMENDED OPERATING CONDITIONS,
V_{CC} = 2.7 V, 5 V, 15 V, T_A = 25°C (unless otherwise noted)

Parameter	Symbol	Testing Conditions		T_A	Min	Typ	Max	Unit
Propagation delay time, low−to−high−level	$t_{(PLH)}$	f = 10 kHz, VSTEP = 100 mV, R_P = 1 MΩ, C_L = 10 pF	Overdrive = 2 mV	25°C		220		μs
			Overdrive = 10 mV			85		
			Overdrive = 50 mV			30		
Propagation delay time, high−to−low−level output	$t_{(PHL)}$		Overdrive = 2 mV	25°C		250		
			Overdrive = 10 mV			55		
			Overdrive = 50 mV			18		
Fall time	tf	R_P = 1 MΩ, C_L = 10 pF		25°C		5		μs

TYPICAL CHARACTERISTICS

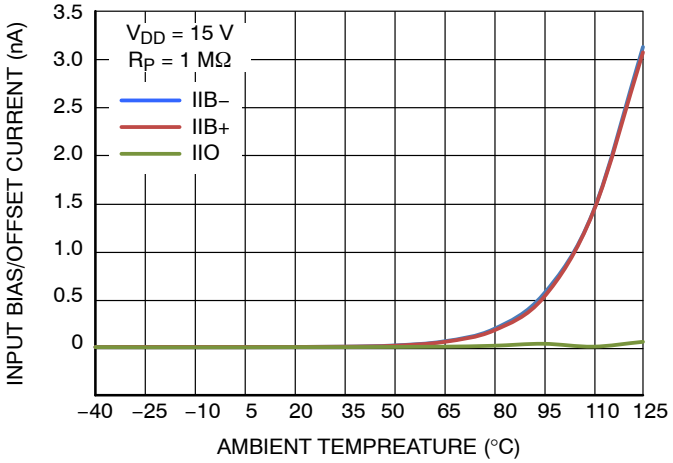


Figure 1. Input Bias/Offset Current vs. Temperature

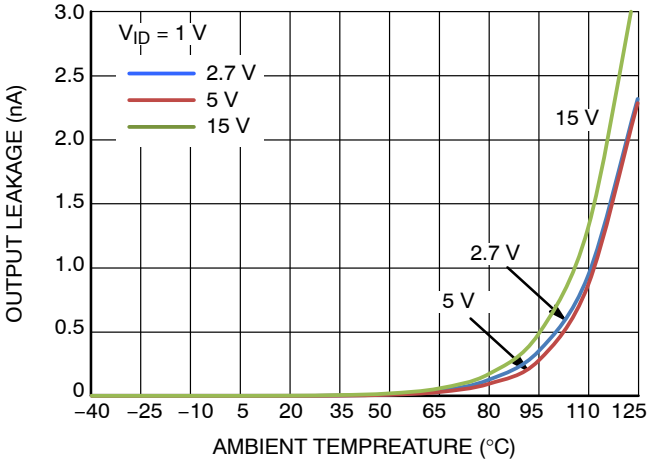


Figure 2. Open Drain Leakage Current vs. Temperature

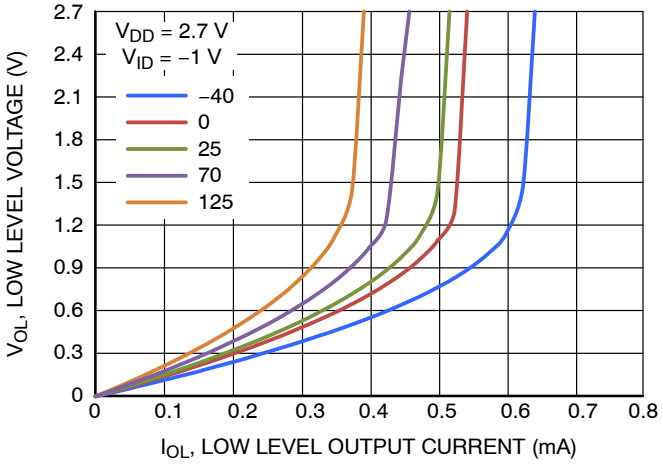


Figure 3. Low Level Output Voltage vs. Low Level Output Current

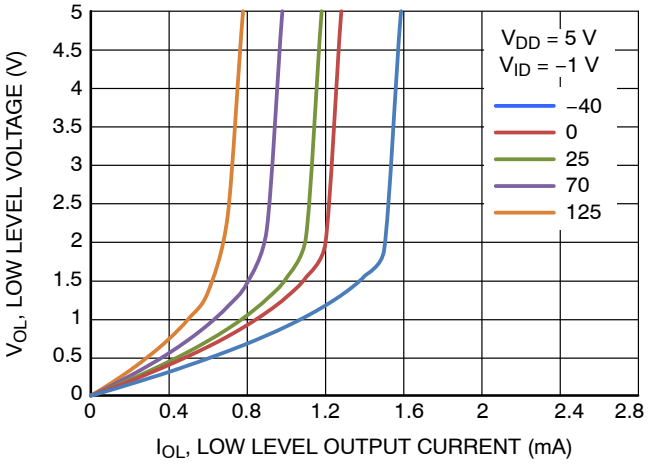


Figure 4. Low Level Output Voltage vs. Low Level Output Current

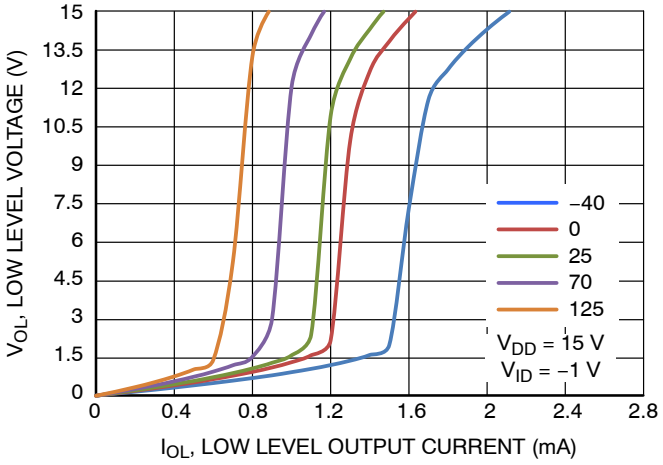


Figure 5. Low Level Output Voltage vs. Low Level Output Current

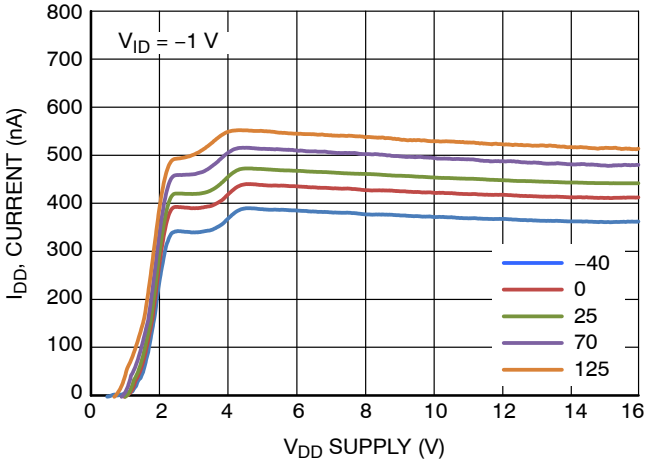


Figure 6. I_{DD} vs. V_{DD} vs. Temperature

TYPICAL CHARACTERISTICS

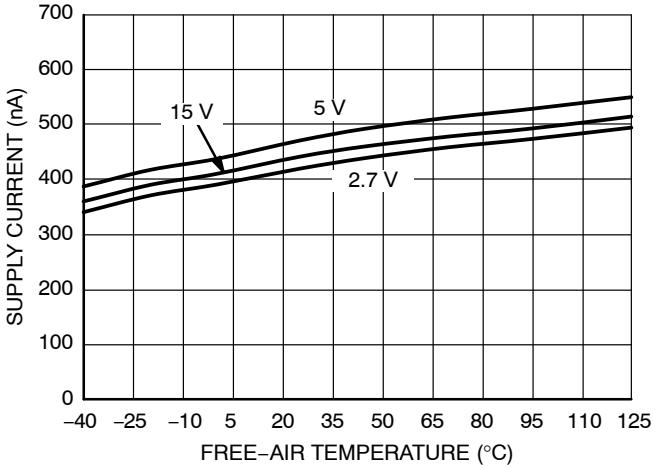


Figure 7. Supply Current vs. Free−Air Temperature

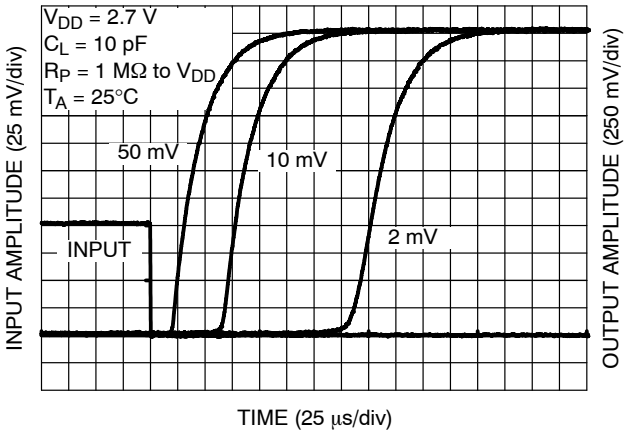


Figure 8. Propagation Delay L−H (2.7 V)

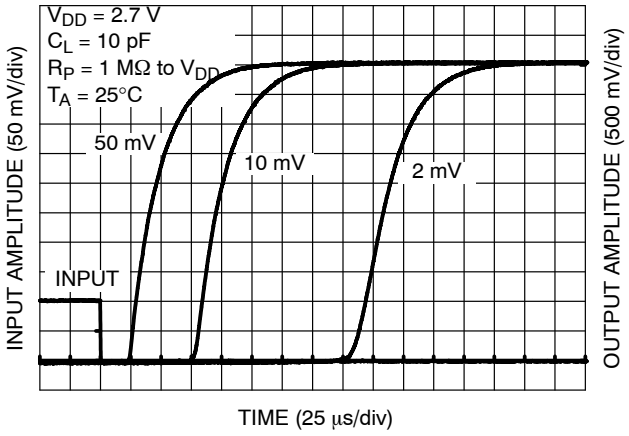


Figure 9. Propagation Delay L−H (5 V)

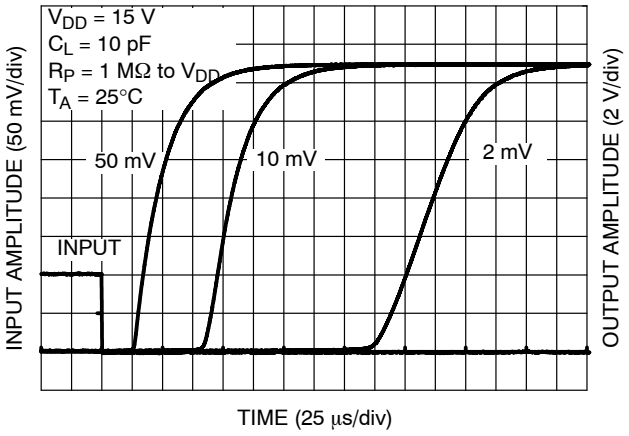


Figure 10. Propagation Delay L−H (15 V)

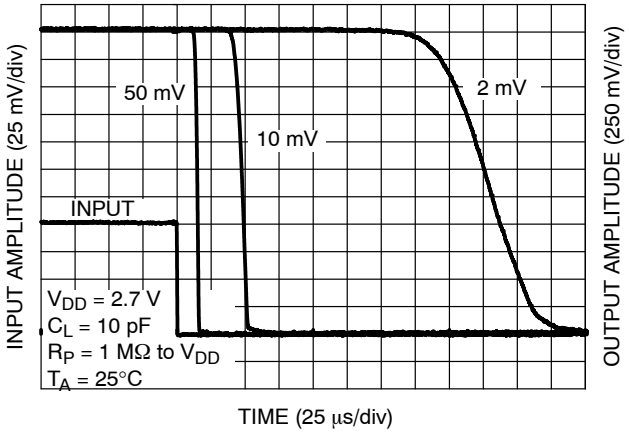


Figure 11. Propagation Delay H−L (2.7 V)

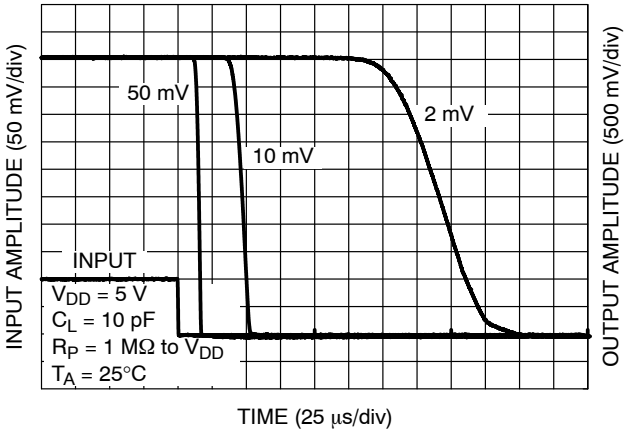


Figure 12. Propagation Delay H−L (5 V)

TYPICAL CHARACTERISTICS

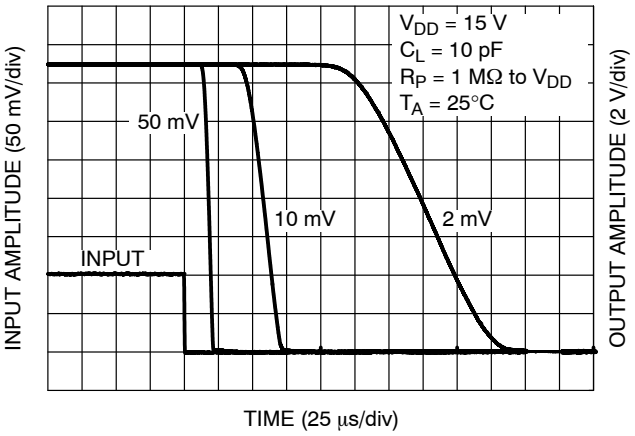


Figure 13. Propagation Delay H−L (15 V)

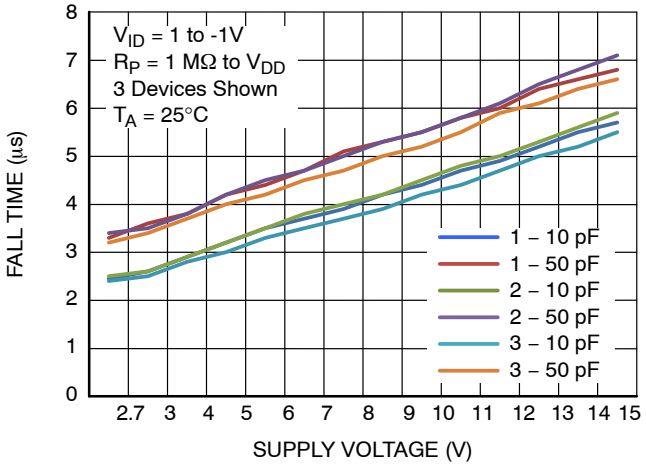


Figure 14. Output Fall Time vs. Power Supply

ORDERING INFORMATION

Device	Package	Shipping†
NCS3402DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

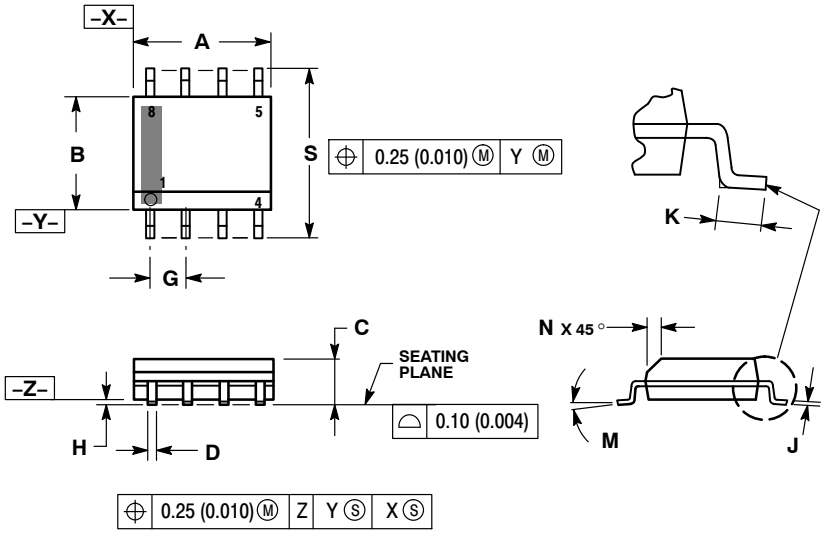
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

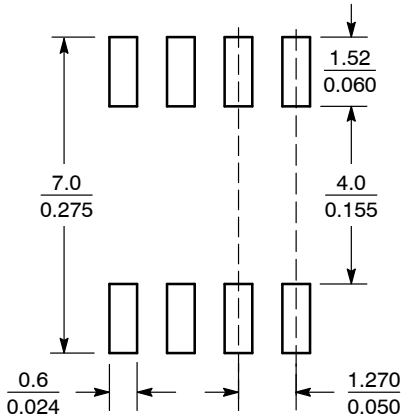
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

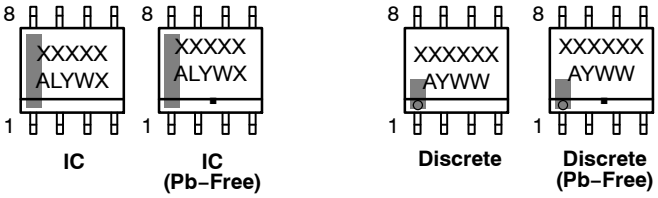
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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