NCS36510

Low Power System-on-Chip For 2.4 GHz IEEE 802.15.4 Applications

The NCS36510 is a low power, fully integrated, System on Chip that integrates a 2.4 GHz IEEE 802.15.4 compliant transceiver, Arm® Cortex®–M3 microprocessor, RAM and FLASH memory, a true random number generator, and multiple peripherals to support design of a complete and secure wireless network with minimal external components.

The NCS36510 offers advanced power management techniques that allow operation down to supply voltages as low as 1 V while minimizing current consumption. The NCS36510 is specifically designed for applications requiring maximum battery life while minimizing cost.

The NCS36510 incorporates an industry leading 32 bit Arm Cortex–M3 for high performance, low power and low cost processing. The NCS36510 includes 640 kB of embedded FLASH memory for program storage along with 48 kB of RAM for data storage.

NCS36510 uses a hardware accelerated MAC to minimize processor overhead while maximizing available processor power for running application software.

Peripherals include DMA, UART(2), SPI(2), I^2C(2), PWM, RTC, three programmable timers, WDT, 18 GPIO, 10 bit ADC with four external inputs and integrated temperature and voltage sensors.

Features

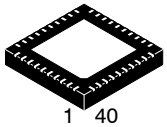
- Low Voltage Operation to as low as 1.0 V
- 0.65 μA Coma Mode Sleep Current
- 6.6 mW Receive Power Consumption
- –99 dBm Receiver Sensitivity
- 6.9 mW Transmit Power Consumption
- Programmable Output Power to ~8 dBm
- 2.4 GHz IEEE 802.15.4 Transceiver
- Arm Cortex – M3 Processor
- AES 128/256 Encryption Engine
- True Random Number Generator
- 640 kB Embedded FLASH Memory
- 48 kB Internal RAM Memory

Typical Applications

- Internet of Things
- Building and Industrial Automation
- ZigBee® / 6LoWPAN / WirelessHART® / Thread™

ON Semiconductor®

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40 PIN QFN, 6x6
MN SUFFIX
CASE 488AR

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCS36510MNTXG	QFN40 (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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BLOCK DIAGRAM

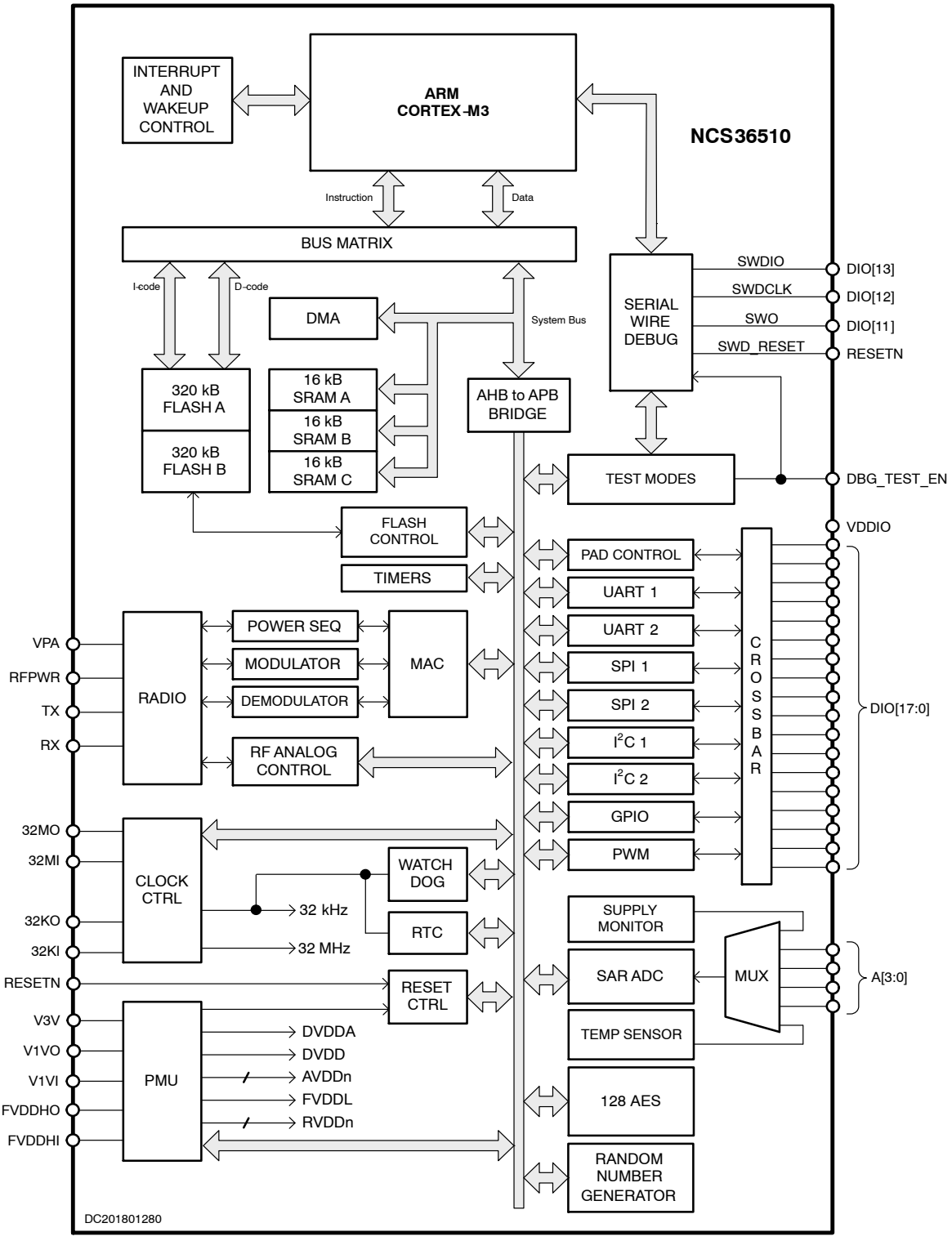


Figure 1. NCS36510 Block Diagram

FUNCTIONAL DESCRIPTION

The NCS36510 is a system on chip for IEEE 802.15.4 applications. Many functions are integrated to lower cost while delivering high performance at the lowest power consumption.

The NCS36510 PMU supports two supply voltage modes: 3 V and 1 V. In 3 V mode a voltage source from 2 V to 3.6 V is applied to V3V which feeds into the internal pre−regulator. The pre−regulator regulates the output, V1V, down to about 1.1 V. From 2 V to 2.6 V the pre−regulator uses an internal linear regulator to generate V1V. From 2.6 V to 3.6 V an internal switching regulator can be used to increase the power conversion efficiency. In 1 V mode the pre−regulator is disabled and the core is supplied directly. V1V can be as low as 1 V and as high as 1.6 V.

The RF receive path has been optimized for minimum power while maintaining high sensitivity. The receive chain employs two down conversion stages with the first one using an IF that is the LO divided by 16 and the second with a fixed low IF. After the second down conversion the signal is digitized for baseband processing which includes image rejection and demodulation. Automatic gain control is used to maximize dynamic range in the analog path.

The RF transmit path has also been optimized for low power. Direct modulation in the frequency synthesizer is used to remove the need for an additional mixer. A non−linear switching power amplifier is used to maximize power efficiency.

To minimize BOM costs, the RF transmit and receive pins can be connected together to avoid an external RF switch.

The LO for the IF and RF blocks are generated by a fully integrated fractional N frequency synthesizer. The reference clock for the frequency synthesizer is a 32 MHz external crystal oscillator.

The NCS36510 has two clock domains. The low speed 32.768 kHz clock is typically used to periodically cycle between the lowest power coma mode and run mode. The high speed 32 MHz clock is used in run mode and by the internal frequency synthesizer for LO generation.

Both clock domains have an internal and external user selectable clock reference. The external clock references are crystal based and more accurate than the internal clock references. The internal clock references can be calibrated against the external 32 MHz clock.

A hardware accelerated MAC offloads the processor to do application tasks.

The integrated processor is an industry leading 32 bit Arm Cortex−M3 with SWD debugging. Integrated memory modules include 640 kB of embedded FLASH and 48 kB of RAM. The FLASH memory is split into 2 x 320 kB banks, enabling over the air upgrades or lower power consumption if both memories are not needed. Both FLASH banks also include an 8 kB information block. The FLASH A information block includes ON Semiconductor factory trim values, the bootloader, and customer specific trim values. Four different software controlled power modes are available to maximize opportunities to save power in the application.

For enhanced software security the NCS36510 bootloader features an option for secure boot that disables the SWD port access. This prevents system takeover and also prevents hackers from reading register and memory contents.

The NCS36510 has an integrated 10 bit ADC. The input is single ended to reduce power consumption, but a pseudo−differential mode is available. Various input scale factors can be used to measure signals up to V3V, regardless of the power supply voltage. Hardware enabled relative measurements are also supported. Four independent external analog inputs are multiplexed at the input to the ADC. The ADC can also measure internal temperature and supply voltage.

Up to 18 general purpose digital I/Os are available and are programmable. Options include drive strength and pullup/pulldown resistors. The GPIOs can be used in conjunction with the following integrated peripherals: UART, SPI, I^2C, and PWM.

PIN CONFIGURATIONS

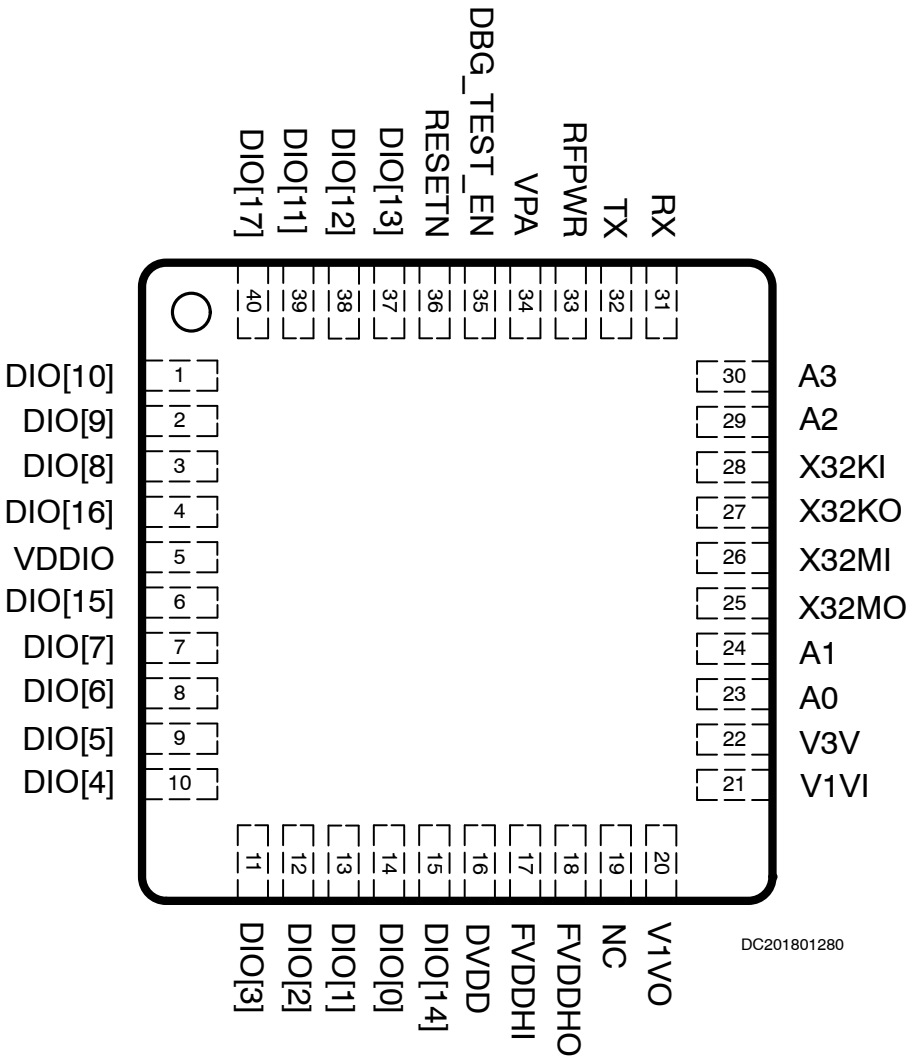


Figure 2. 40−Pin QFN Configuration (Top View)

PIN ASSIGNMENT

Table 1. 40−PIN QFN CONFIGURATION

Pin	Pin Name	Description
1	DIO[10]	General Purpose Digital I/O
2	DIO[9]	General Purpose Digital I/O
3	DIO[8]	General Purpose Digital I/O
4	DIO[16]	General Purpose Digital I/O
5	VDDIO	Digital I/O Bank Power
6	DIO[15]	General Purpose Digital I/O
7	DIO[7]	General Purpose Digital I/O
8	DIO[6]	General Purpose Digital I/O
9	DIO[5]	General Purpose Digital I/O
10	DIO[4]	General Purpose Digital I/O

Table 1. 40−PIN QFN CONFIGURATION (continued)

Pin	Pin Name	Description
11	DIO[3]	General Purpose Digital I/O
12	DIO[2]	General Purpose Digital I/O
13	DIO[1]	General Purpose Digital I/O
14	DIO[0]	General Purpose Digital I/O
15	DIO[14]	General Purpose Digital I/O
16	DVDD	Digital 950 mV Regulator
17	FVDDHI	Embedded FLASH 1.8 V Regulator, Input to external filter required for 1 V mode
18	FVDDHO	Embedded FLASH 1.8 V Regulator, Output from external filter required for 1 V mode
19	NC	Tie to GND or leave floating
20	V1VO	Core 1.1 V Regulator, Output to external filter required for 3 V mode using the switching regulator
21	V1VI	Core 1.1 V Regulator, Input to external filter required for 3 V mode using the switching regulator
22	V3V	Main power input
23	A0	ADC Channel Input
24	A1	ADC Channel Input
25	X32MO	32 MHz Crystal Output
26	X32MI	32 MHz Crystal Input
27	X32K0	32.768 kHz Crystal Output
28	X32KI	32.768 kHz Crystal Input
29	A2	ADC Channel Input
30	A3	ADC Channel Input
31	RX	RF LNA Input
32	TX	RF PA Output
33	RFPWR	RF PA Regulator Output
34	VPA	RF PA Regulator Input
35	DBG_TEST_EN	When high enables SWD debug interface, also used to allow special access to FLASH information blocks, and internal test modes.
36	RESETN	Active Low Reset
37	DIO[13]	General Purpose Digital I/O
38	DIO[12]	General Purpose Digital I/O
39	DIO[11]	General Purpose Digital I/O
40	DIO[17]	General Purpose Digital I/O
EP	Exposed Pad	GND, thermal pad under package

CPU

The NCS36510 integrates the powerful and energy efficient Arm Cortex−M3 processor, version R2.1. The processor uses the Thumb−2 instruction set and is optimized for high performance with reduced code size and low power operation. The Cortex−M3 efficiently handles multiple parallel peripherals and has integrated sleep modes including data retention for the lowest possible coma mode current. With industry standard tool chain and support, developing applications on the NCS36510 platform reduces time to market.

Adjustable clock rates and clock switching also provide further means of lowering the power consumption. Typically the CPU is clocked at 32 MHz to execute code as quickly as possible.

Next to the regular Arm Cortex−M3 processor interrupts, the NCS36510 implements 20 external source interrupts for peripheral devices. A powerful nested, pre−emptive and priority based interrupt handling assure timely and flexible response to external events.

MEMORY ORGANIZATION

This section documents the memory map of the NCS36510.

FLASH

NCS36510 contains a total of 640 kB of FLASH memory, organized as two banks of 320 kB each. Two independent FLASH banks are used to allow either OTA upgrades or dual stack applications. If a FLASH bank is unused, it can be powered down to save power.

Both FLASH banks include an 8 kB information block. The FLASH A information block contains the bootloader and factory programmed trim values. There are a minimum of three application related trims that can be programmed by the customer: 32.768 kHz external oscillator, 32 MHz external oscillator, and the RSSI offset. These application trims can be determined during the design phase, and for a given PCB design they can be set to a constant value for all boards of the same design. At the factory these are set to a nominal value.

The FLASH B information block does not contain any factory trim information.

FLASH ALIAS AND REMAP

NCS36510 has a FLASH remap feature that allows the FLASH A and FLASH B to change positions in the memory map when activated. This makes it easier to reboot the system from FLASH B if doing over the air firmware updates.

Another related feature is the FLASH alias. The FLASH alias allows the FLASH A and FLASH B contents to be visible in a fixed address space regardless of the remap setting.

Both FLASH remap and alias features are shown in the memory map diagrams.

During ON Semiconductor factory test, the factory trim values and bootloader are written to the FLASH A information block. No information is stored in the FLASH B information block. Software must be careful when using the FLASH remap feature as the factory trims and bootloader could be missed since FLASH A and FLASH B change places in the memory map. An easy way to avoid issues is to use the FLASH A information block alias during boot up because the alias memory map does not depend on the remap setting. The ON Semiconductor software already takes care of this remap functionality, but this feature is important to understand for customers writing their own software.

The bootloader is also stored in the FLASH A information block. To reprogram the bootloader it is required to drive the DBG_TEST_EN pin high and to write an unlock code to the FLASH. The factory trim contents must be read out, the entire FLASH information block erased, and then the bootloader and factory trims written back in. If the factory trims are lost on a device it will become inoperable as factory trims are not recoverable.

RAM

NCS36510 has a total of 48 kB of internal RAM, split into three banks of 16 kB. One or two of the RAM banks can be used in coma mode for data retention.

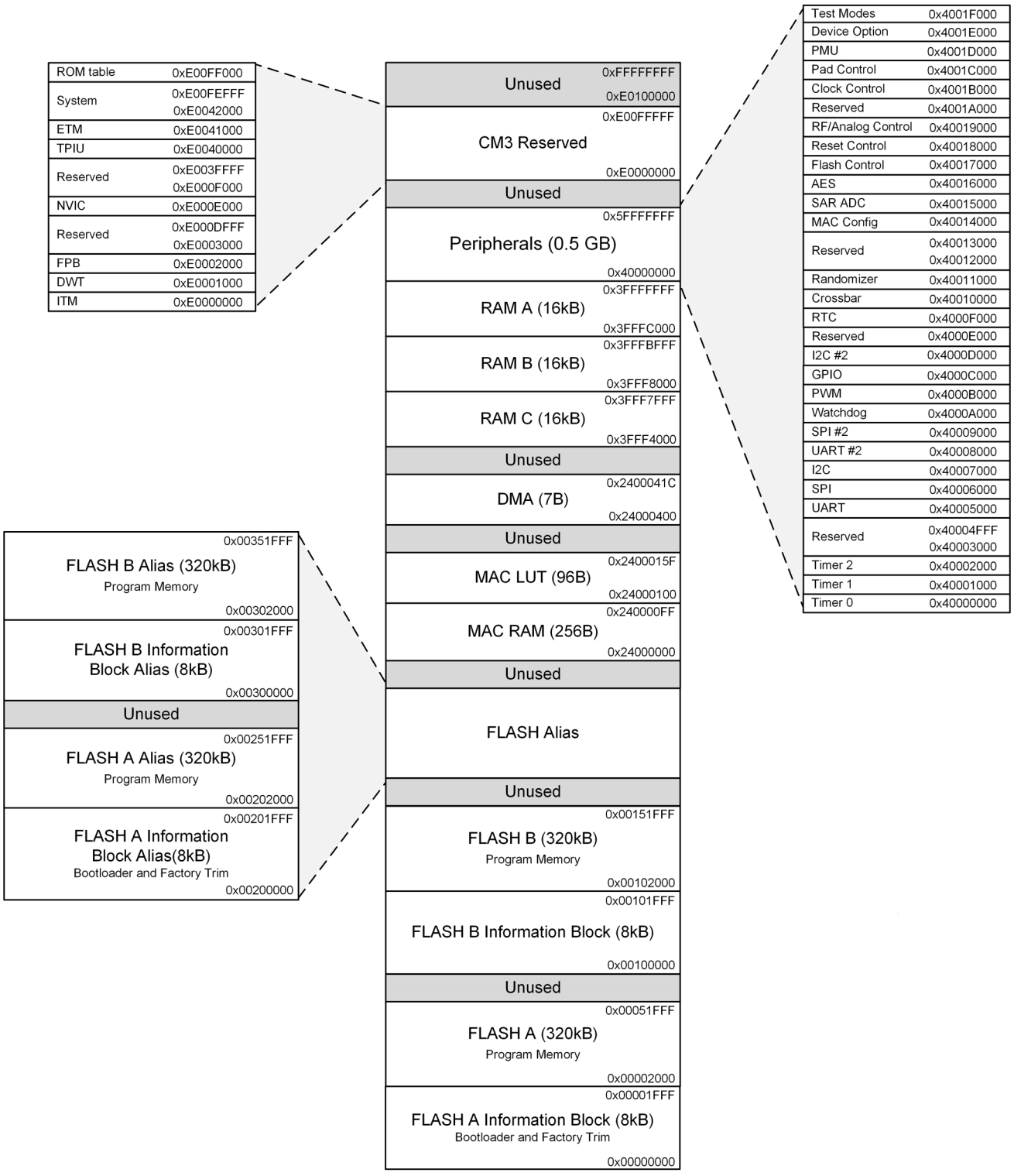


Figure 3. Default Memory Map

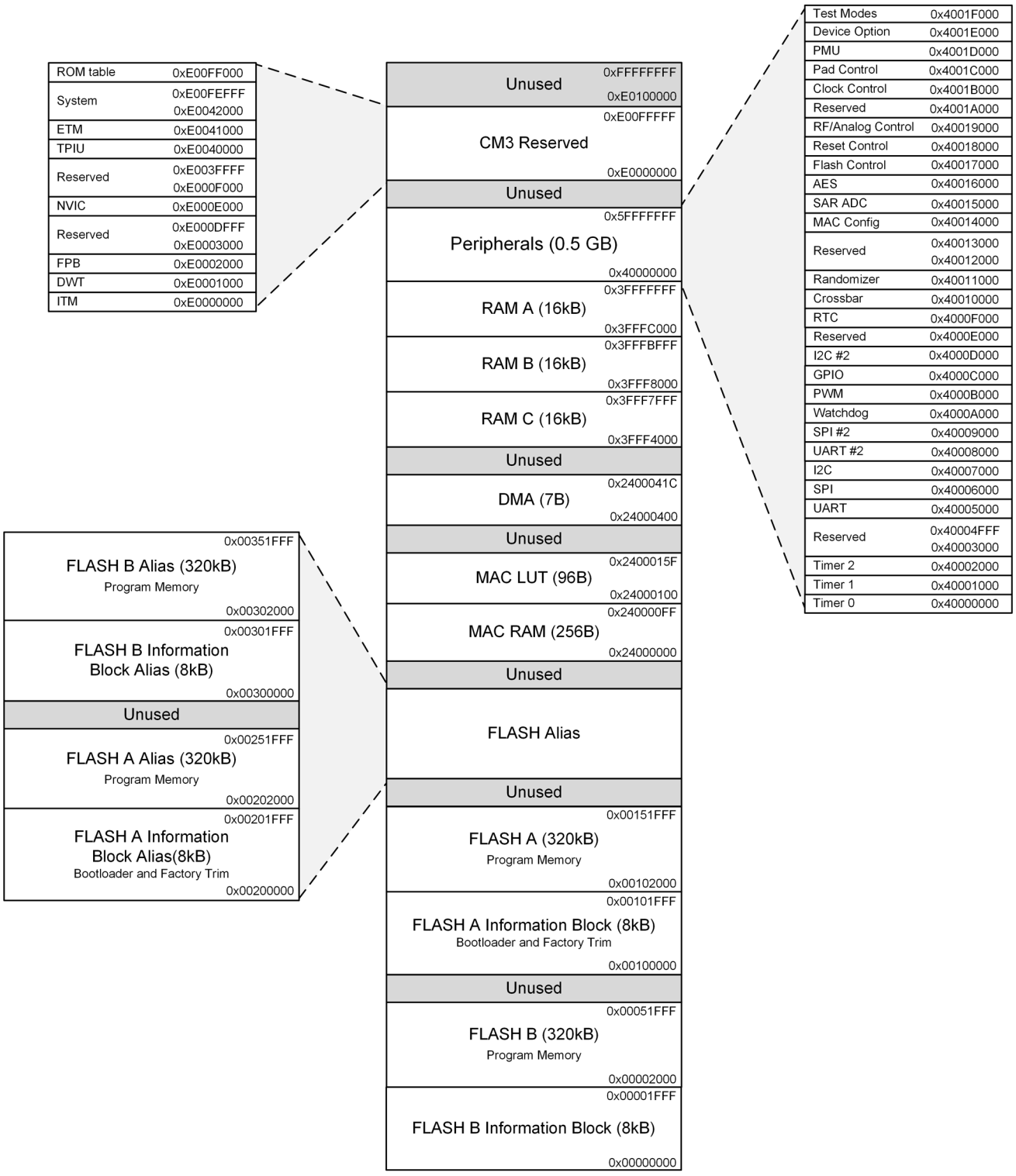


Figure 4. Remapped Memory Map

SYSTEM CLOCKS

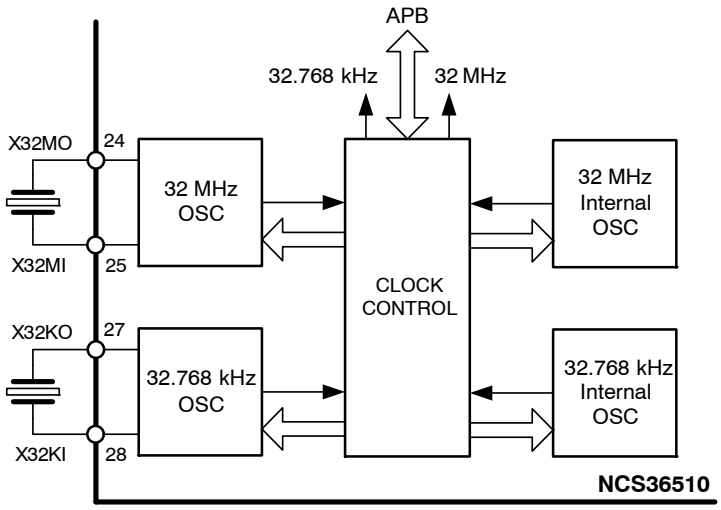


Figure 5. Clock System

The NCS36510 can be run from any of the four available clocks. There are two external oscillators, one 32 MHz and one 32.768 kHz. Both require external crystals to be used. There are two internal oscillators, one 32 MHz and one 32.768 kHz.

The 32 MHz external crystal based clock is needed for 802.15.4 RF carrier frequency accuracy requirements. The external 32.768 kHz crystal based clock is only needed if an accurate RTC is required.

An internal 32 MHz oscillator is typically used for fast boot up before the external 32 MHz oscillator is enabled and ready.

The 32 MHz system clock can be divided by the following values: 1, 2, 3, 4, 5, 6, 7, and 8. However typically the clock is not divided as it's more efficient to run code as quickly as possible and then put the device to sleep or go into coma mode.

The 32.768 kHz internal oscillator is typically used during low power modes as it has the lowest power consumption. If accuracy is a higher priority over power consumption then the external 32.768 kHz oscillator can be used instead.

Both internal oscillators can be trimmed by using the 32 MHz crystal oscillator based clock as a timing reference.

RESET

There are five sources of reset: internal POR and BO, external reset, software reset, and watchdog timer.

INTERNAL POWER−ON RESET AND BROWNOUT

The POR and BO functions are combined in the PMU. During startup, the POR is released when V3V is at a high enough voltage to support the internal digital logic voltage regulators. After power up the voltage at V1V is monitored and if it gets too low, a brownout reset is generated. A POR and a brownout have the same effect on the system which is a full reset including the processor debug logic.

Upon POR or BO the processor starts to fetch instructions from address 0x0. Please see note in FLASH section about remap and alias features.

EXTERNAL RESET

When the external reset pin is driven low, the NCS36510 is held in reset. The processor debug logic is not reset.

Warning: The NCS36510 has a POR test mode intended for use during ON Semiconductor factory testing only. If the DBG_TEST_EN pin is high, and the RESETN pin low while powering up the device, this POR test mode will be activated. The DIO[0] pin will mirror the internal POR signal. The only way to exit this mode is to power down the device, and restart with the DBG_TEST_EN pin low and or the RESETN pin high.

SOFTWARE RESET

Software reset can be called when switching from one application to the other, after remap of the FLASH banks, or on exit of a processor exception. The software requested reset will not reset all processor or peripheral device registers.

WATCHDOG TIMER

NCS36510 implements a programmable watchdog timer. The watchdog timer is disabled by default and the application software needs to instantiate the watchdog timer driver and enable it. The WDT has a register locking safety mechanism to prevent errant software from corrupting the registers. While locked the only supported operation is a clear. The watchdog is on the 32.768 kHz clock domain so it has a minimum resolution of 30.5 μS. It is 18 bits wide giving it a maximum timeout time of 8 seconds. When the WDT overflows, the system is reset and the reset sources register is updated to indicate the system was reset by the watchdog timer. If a debugger is attached then the WDT is paused.

EXCEPTION HANDLING

The Arm Cortex−M3 processor supports priority based nested vectored interrupts. The NCS36510 has 35 interrupts with 16 levels of programmable priority.

Table 2.

Exception Number	Exception Type	Priority	Description
1	Reset	−3 (Highest)	Reset
2	NMI	−2	Non−maskable interrupt. This is set to the watchdog interrupt.
3	Hard fault	−1	All fault conditions if the corresponding fault handler is not enabled.
4	MemManage fault	Programmable	Memory management fault
5	Bus fault	Programmable	Bus fault
6	Usage fault	Programmable	Exceptions resulting from program error.
7−10	Reserved		
11	SVC	Programmable	Supervisor Call
12	Debug Monitor	Programmable	Debug monitor (breakpoints, watchpoints, or external debug requests)
13	Reserved	Programmable	
14	PendSV	Programmable	Pendable Service Call
15	SYSTICK	Programmable	System Tick Timer
16	Timer 0	Programmable	Timer 0 interrupt
17	Timer 1	Programmable	Timer 1 interrupt
18	Timer 2	Programmable	Timer 2 interrupt
19	UART	Programmable	UART interrupt
20	SPI	Programmable	SPI interrupt
21	I2C	Programmable	I2C interrupt
22	GPIO	Programmable	GPIO interrupt
23	RTC	Programmable	Real−time−clock interrupt
24	Flash Controller	Programmable	Flash Controller
25	MAC	Programmable	MAC interrupt
26	AES	Programmable	AES interrupt
27	ADC	Programmable	ADC interrupt
28	Clock Calibration	Programmable	Clock calibration interrupt
29	UART #2	Programmable	UART Interrupt
30	UVI	Programmable	Under Voltage Indicator Interrupt
31	DMA	Programmable	DMA interrupt
32	CDBGP-WRUPREQ	Programmable	Debug request
33	SPI #2	Programmable	SPI #2 Interrupt
34	I2C #2	Programmable	I2C #2 Interrupt
35	FVDDH Comp	Programmable	FVDDH Supply Comparator Trip

WIRELESS TRANSCEIVER

The wireless transceiver consists of a:

- Radio
  - Receiver
  - Transmitter
  - Antenna Diversity
- Modem

RADIO

The NCS36510 radio is a single ended interface to minimize power consumption and external components. The transmit and receive pins are separated in the package but are typically connected on the application board. When transmitting the receiver is disabled, and vice versa. A biasing inductor is typically shared between the ports to minimize external components.

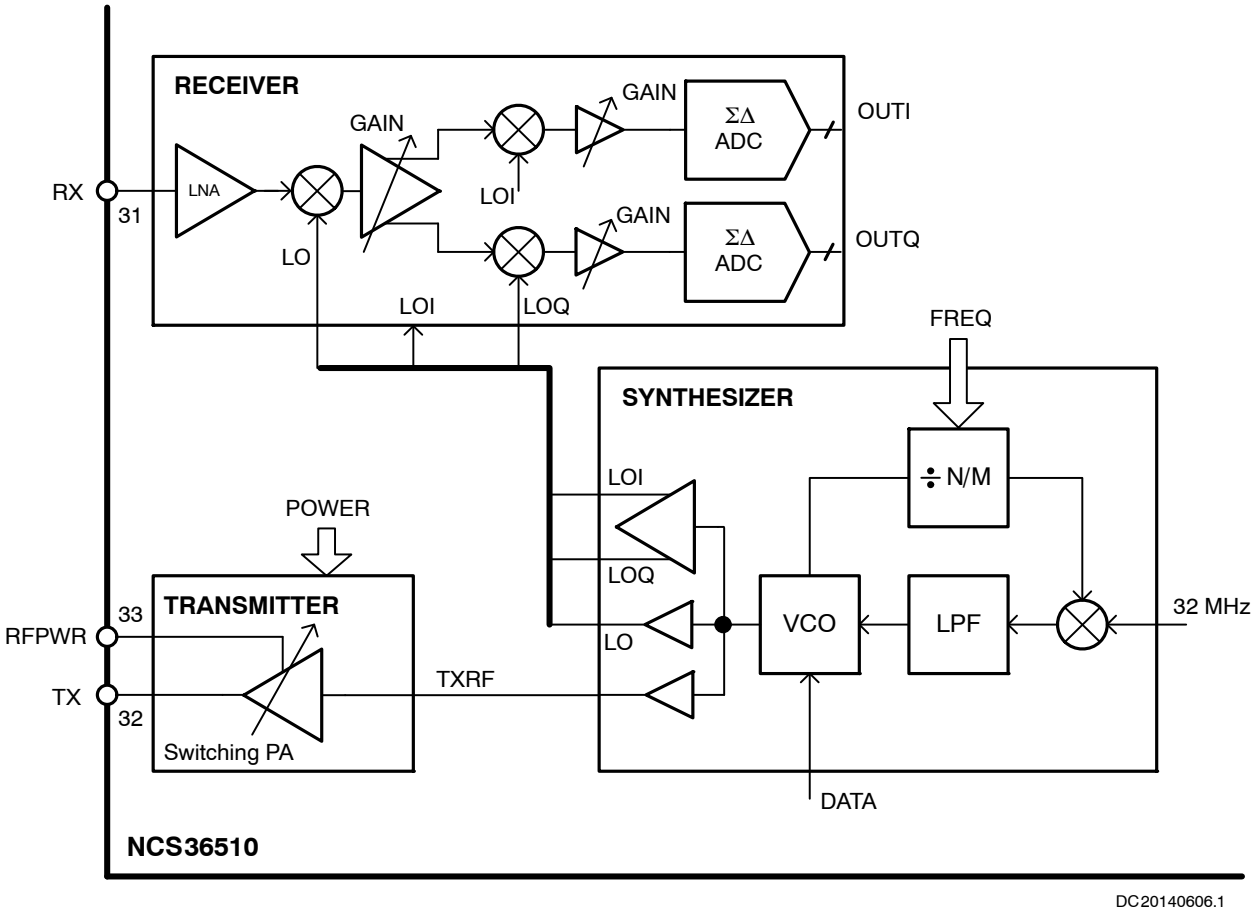


Figure 6. Radio Block Diagram

An external matching circuit is required to transform the impedance of the connected transmit/receive port to the antenna impedance to maximize power transfer and receiver sensitivity.

Receiver

A fully integrated fractional N frequency synthesizer is used to generate the necessary LO. The RF input is amplified by a LNA and is followed by a sliding IF mixer to down convert the signal to the first IF of LO/16. After further gain the signal is down converted again to baseband as real and imaginary components (I and Q). The I and Q signals are then converted to the digital domain for baseband processing. The receive path employs an AGC algorithm to maximize dynamic range.

Transmitter

The transmitter directly modulates the output baseband signal to RF in the frequency synthesizer. This avoids an additional mixer and saves power. The non−linear switching PA offers the highest efficiency theoretically possible.

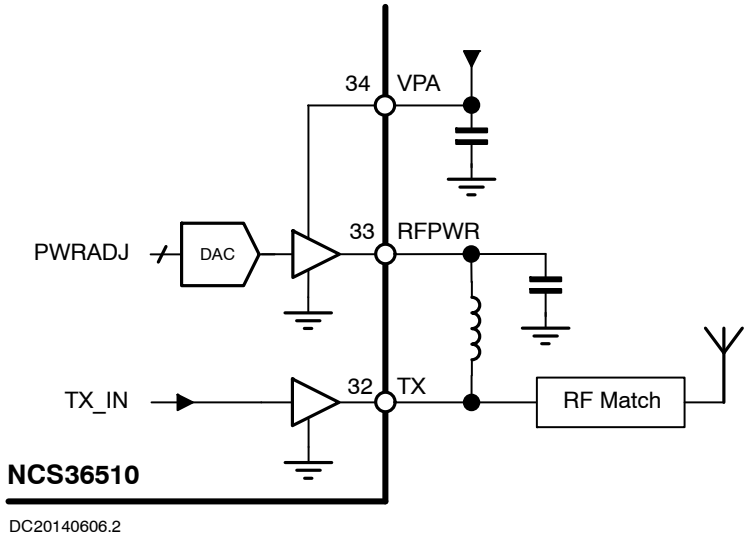


Figure 7. Transmitter

The PA requires an external inductor from the Tx pin to the RFPWR pin.

The supply voltage at VPA can be from 1 V to 3.6 V, independently from the other power domains. Typically VPA is connected to V3V.

The RF output power is determined by the power setting set at the RFPWR regulator. The maximum DC voltage at RFPWR is about 2 V. When the transmitter is off, the RFPWR node is pulled to ground through an internal switch.

Antenna Diversity

Using a single antenna in a RF multi−path environment may make it difficult to receive signals consistently. To combat this natural phenomenon, antenna diversity control support is offered. Antenna diversity requires an external antenna switch to switch between two separate antennas located at least a quarter wavelength away from each other. Using a GPIO port, an external antenna switch can be automatically switched to maximize sensitivity.

MODEM

The NCS36510 modem combines a proprietary blend of hardware and software to implement the requirements of the IEEE 802.15.4 standard. By efficiently splitting the hardware and software interface for the modem, processor bandwidth is maximized and power consumption is minimized.

PERIPHERAL DEVICES

PERIPHERAL API

The software development kit contains drivers for all the NCS36510 peripherals. Each peripheral can be initialized and operated through an API.

PERIPHERAL ENABLE AND DISABLE

To save power, the clock to each peripheral can be gated off. Writes to the disabled peripherals are ignored.

CROSS BAR

NCS36510 has 18 digital IO pins to communicate with external devices. These pins are shared between the following internal peripheral devices:

1. UART 1
2. UART 2
3. I^2C 1
4. I^2C 2
5. SPI 1
6. SPI 2
7. PWM
8. GPIO
9. SWD

The application needs to configure the cross bar to wire the desired peripheral device to the desired IO pins, given the system constraints. The tables below indicate what peripheral device can be wired to what pin.

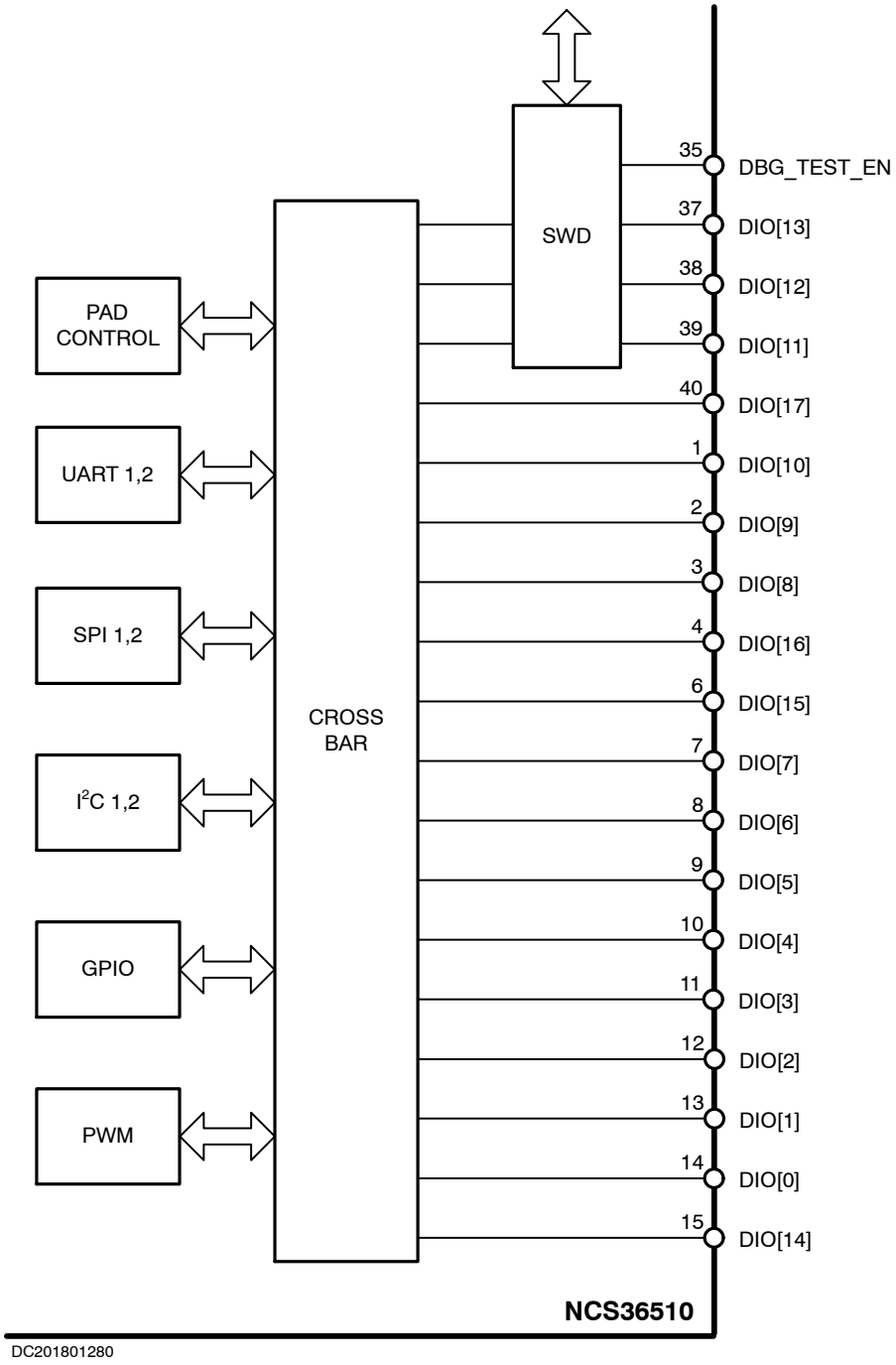


Figure 8. Cross Bar

The debug port is wired to digital IO 11, 12 and 13, only when the DBG_TEST_EN pin is pulled to logic ‘1’. Debug port IO’s can’t be assigned to different IO’s.

Table 3. CROSS BAR

		DIO																
		17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART	Transmit Data																		X
	Receive Data																	X	
	Clear To Send																X		
	Request To Send															X			
	Data Terminal Ready														X				
	Data Set Ready													X					
	Data Carrier Detect												X						
	Ring Indicator											X							
UART#2	Transmit Data										X								
	Receive Data									X									
	Clear To Send								X										
	Request To Send							X											
I²C	SCLK					X		X						X			X		
	SDATA						X		X						X	X			
I2C#2	SCLK	X			X														
	SDATA		X	X															
SPI#1	SCLK										X				X				
	SDATAO									X				X					
	SDATAI								X				X						
	SSNI							X				X							
	SSNO<0>						X				X								X
	SSNO<1>					X				X								X	
	SSNO<2>								X								X		
	SSNO<3>							X								X			

Table 3. CROSS BAR

		DIO																	
		17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI#2	SCLK				X														
	SDATAO			X															
	SDATAI		X																
	SSNI	x																	
	SSNO<0>	x																	
PWM	Output					X	X			X		X	X						
GPIO	17	x																	
	16		X																
	15			X															
	14				X														
	13					X													
	12						X												
	11							X											
	10								X										
	9									X									
	8										X								
	7											X							
	6												X						
	5													X					
	4														X				
	3															X			
	2																X		
	1																	X	
	0																		X

DIGITAL INPUT/OUTPUT

NCS36510 has 18 identical GPIO. The following list documents the programmable options available independently for each GPIO.

Each GPIO input is compatible with CMOS levels and has hysteresis.

Options:

- Bi−directional capability
- Individually configurable interrupt lines
- Rising, falling, or both edge interrupt
- High, low, or both logic level interrupt
- Loopback mode
- Push pull or open drain
- Four programmable drive strengths
- Pullup, pulldown or neither

SAR ADC

The NCS36510 has a fully integrated 10 bit SAR ADC. The ADC is single ended to reduce power consumption. A six input multiplexer allows up to four external signals to be measured. The other two inputs are for internal temperature and battery voltage (V3V) sensors.

The SAR ADC completes a conversion as fast as 5 μs with a 4 MHz sample clock in 20 clock cycles.

To support a wide range of input voltages, there is a programmable resistive voltage divider on the external inputs. The table below shows the ideal settings.

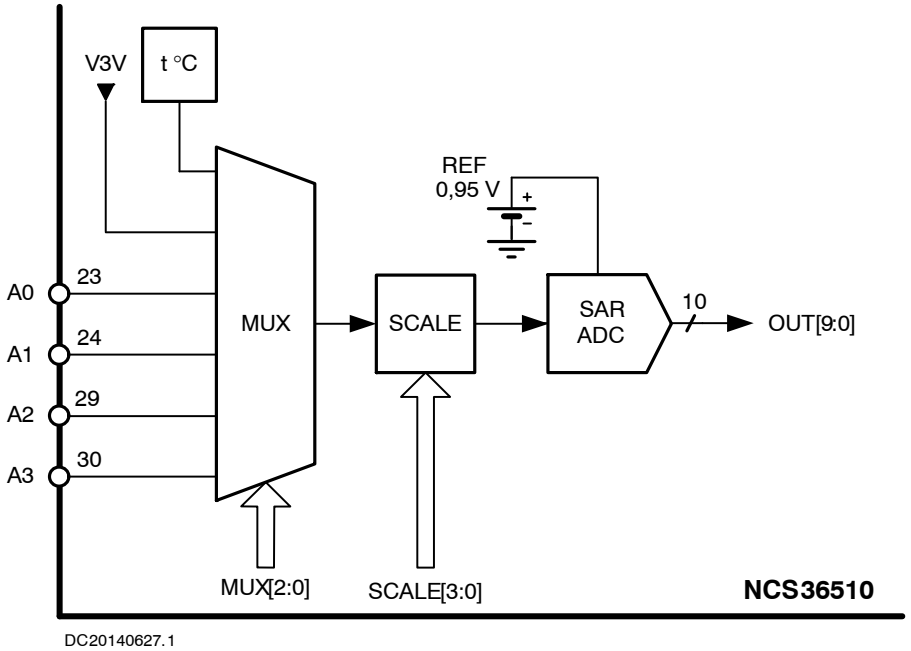


Figure 9. ADC Block Diagram

Warning: The user has the responsibility to respect the absolute maximum ratings. The voltage on the ADC pins cannot exceed V3V + 0.3 V, regardless of the input scaling.

Several modes of ADC operation are available including absolute, ratio based, and pseudo−differential.

All ADC conversions are referenced to an internal fixed reference of nominally 950 mV. Absolute conversions represent the input signal compared to this fixed reference.

Table 4. ADC SCALE FACTORS

Scale Factor	Maximum Input	Input Resistance
1.00	950 mV	High Impedance
0.69	1.3 V	80 kΩ
0.53	1.7 V	52 kΩ
0.43	2.1 V	43 kΩ
0.36	2.5 V	38 kΩ
0.31	2.9 V	36 kΩ
0.28	3.3 V	34 kΩ
0.24	3.7 V	32 kΩ

For applications that require measuring an external signal versus an external reference, a ratio based conversion mode is supported. Two ADC conversions are done back to back and automatically divided to get a ratio.

Pseudo−differential mode is similar to ratio based mode, except the final computation is the difference of the two signals instead of the ratio.

Ratio based pseudo−differential mode consists of three conversions. The first two are taken as a differential signal, the third is considered as a reference. The resulting differential voltage is automatically divided by the third conversion resulting in a pseudo−differential ratio.

This SAR ADC has a finite input time constant. The mux has a finite resistance, and the input of the ADC has a finite capacitance. The input voltage must be fully settled to get an accurate conversion. The input time constant also depends on the scale factors programmed. The following table contains typical values for time constants as a function of the input scale factor. For maximum accuracy, at least 7 time constants of settling time are recommended.

Table 5. TYPICAL ADC SETTLING TIMES

Scale Factor	Time Constant, τ	7τ
1.00	160 ns	1.12 μs
0.69	110 ns	770 ns
0.53	85 ns	595 ns
0.43	68 ns	476 ns
0.36	58 ns	406 ns
0.31	50 ns	350 ns
0.28	44 ns	308 ns
0.24	39 ns	273 ns

The ADC can be used in either single or continuous conversion modes.

There is a status bit that can be polled to determine if the ADC is busy. An interrupt can also be configured to avoid consuming processor cycles polling the status bit.

Averaging can improve the accuracy of the SAR ADC conversions as compared to single shot measurements.

PWM

The PWM peripheral generates a programmable duty cycle digital output signal. The duty cycle can be programmed from 0% to 100% with 8 bit resolution.

The PWM frequency can be either the system clock divided by 256 or the system clock divided by 4096.

The system clock is typically 32 MHz giving the lower PWM frequency of 7.8125 kHz or the upper frequency of 125 kHz.

UART

NCS36510 implements two UART devices, UART 1 and UART 2.

UART 1 is a complete implementation of a 16550 UART. By configuring the crossbar UART1 can be set up as a complete 16550 UART, with all control wires.

UART 2 is a reduced functionality version of UART1. Specifically the crossbar can be setup to support transmit and receive along with clear to send and request to send. UART 1 can also be configured the same way if desired.

The UART baud rate generator produces timing strobes at the baud rate (for the transmitter) and at 16 times the selected baud rate (for the receiver). The receiver examines the incoming data and uses the first edge of the start bit to determine the bit timing. Bits can be received with up to half a bit time error and still be captured properly. Transmit and receive paths can be configured to use a single register for data or to use FIFOs.

The UART 1 and UART 2 FIFO buffers are 16 by 8 bits.

Interrupts are identified by an interrupt pending flag with more detailed interrupt status registers that can be read. The statuses include (in descending priority order): receiver line status, received data available, character timeout, transmitter holding register empty, and modem status.

I^{2}C

NCS36510 implements two I^{2}C bus master interfaces, I^{2}C1 and I^{2}C2. Both are identical.

The I^{2}C bus is an industry−standard two−wire (clock and data) serial communication bus. The I^{2}C bus is a single master, multiple slave bus. I^{2}C specifies that the I^{2}C master will initiate all read and write transactions, and that the I^{2}C slave will respond to these requests.

The I^{2}C command FIFO is 32 x 8 bits and the read FIFO is 16 x 8 bits.

The I^{2}C system clock can either be clocked by the internal APB clock or by the external I^{2}C bus clock. If using the APB clock an I^{2}C system clock divider can be used to divide the clock up to a value of 0x1F. The resulting I^{2}C clock frequency can be calculated as follows:

$$\text{I}^2\text{C System Clock Frequency} = \frac{\text{APB PCLK}}{(\text{divider} + 2)}$$

The I^{2}C system clock is always a factor of 4 faster than the I^{2}C bus clock to allow for proper internal clock phasing and synchronization.

Interrupts are generated when the read and/or command FIFOs are not empty and upon errors.

SPI

NCS36510 implements two SPI Bus controllers, SPI1 and SPI2. SPI1 supports up to 4 slave selects. SPI2 supports 1.

The SPI bus controller can be configured under software control to be a master or slave device. The data is transmitted synchronously with the MOSI relative to the SCLK generated by the master device. The master also receives data on the MISO signal in a full duplex fashion. When the core is configured as a slave, the MISO signal is tri−stated to allow for multiple slaves to transmit data to the master when the slave's slave select control is enabled.

The SPI can operate in 8, 16, or 32 bit mode. The SPI FIFO is 16 x 32 bits.

The SPI master clock is a divided version of the APB clock. The divider is programmable from 0x00 to 0xFF. The resulting SPI master clock is given by:

$$\text{SPI Master Clock} = \frac{\text{APB PCLK}}{2 \cdot (\text{divider} + 1)}$$

Interrupts are generated for the following conditions: receive (RX) FIFO full, RX FIFO half full, RX FIFO not empty, transmit (TX) FIFO not full, TX FIFO half empy, TX FIFO empty, transfer error, and slave select synchronized to APB clock.

RTC

The RTC consists of two counters that are clocked by the 32.768 kHz clock. Both counters have their own alarm, interrupt, and clear functions.

The first counter is a 15 bit sub−second counter (2^15−1/32768 = 1s). It can be used for wait times less than one second.

The other counter is a 32 bit seconds counter. The seconds counter is incremented by the sub−second counter rollover. The second counter can count up to ~136 years so it can be used as a UNIX (POSIX or Epoch) time counter if desired.

When both second and sub−second counters are enabled the RTC will generate an interrupt when both counters expire, allowing for non−integer second timing (for example 3.6 s).

MAC

The NCS36510 MAC is comprised of a proprietary mix of hardware and software. The developer interfaces with the MAC through a software API.

The MAC implements all necessary functions of the IEEE 802.15.4 specification as required to develop non−beaconed wireless networks including:

- Channel access
- Frame validation
- Acknowledged frame delivery (ACK)
- Association/Disassociation

- Hooks for security
- 16 bit or 64 bit extended addresses
- CSMA−CA
- ACK
- ED
- LQI
- 16 channels

SECURITY

The AES 128/256 module provides hardware support for the encryption and decryption operations used in IEEE 802.15.4. To support security required for IEEE 802.15.4, the use of CCM is required. CCM is a combination of counter mode (CTR) and cipher block chaining (CBC). It can perform a “Counter” (CTR) or a Cipher Block Chaining (CBC) encryption in 12 clocks for 128 bit encryption, or 16 clocks for 256 bit encryption.

The definition of CCM mode encryption is documented in the NIST publication SP800−38C. Details of the implementation of the AES module can be found in federal information processing standard fips197. For more information, visit the following website: https://en.wikipedia.org/wiki/Block_cipher_mode_of_operation.

TIMERS

NCS36510 has three independent 16 bit down count timers.

Each of the three independent timers can:

- Be clocked at either the system clock rate, or a choice of 8 prescale values; 0, 2, 8, 16, 32, 128, 256, and 1024
- Be loaded with a value from a preload register
- Generate an interrupt on 0 counts
- Be operated in free−running or periodic modes. In periodic mode the interrupt is generated one clock later than the pre−load value since 0 is included in the count.

TRUE RANDOM NUMBER GENERATOR

NCS36510 implements a TRNG. The randomizer can be used to generate 32−bit random numbers. The TRNG can optionally be preloaded with a 32−bit random seed value. The random number is generated using a maximum length LFSR.

DMA CONTROLLER

The DMA controller is a single channel direct memory access controller. It can be used to directly transfer data from one memory to another.

After initial setup, the DMA controller initiates data transfer from the user specified source address to the internal FIFO. It then performs another transfer to move the data from the FIFO to the user specified destination address. The FIFO size is 32 words by 32 bits.

The DMA controller transfers data on word, 1/2 word, and byte aligned boundaries. The DMA controller supports beat modes of 4, 8, and 16 using incrementing bursts. Unspecified length bursts and single transfers are also supported. Wrapping bursts are not supported.

The bursts are automatically controlled and are based on the number of specified bytes to transfer.

Interrupts are generated upon transfer completion and/or error conditions.

SWD DEBUG INTERFACE

NCS36510 implements a standard Arm SWD interface. Use any SWD compliant hardware debugger interface to interact with the internals of the NCS36510. Section 13.2 details how to connect the in circuit debugger hardware. The DBG_TEST_EN pin has to be driven high for the SWD interface to work. Note that the NCS36510 cannot go into coma mode with the debugger attached.

Warning: Some debuggers do not work at 1 V.

POWER MANAGEMENT UNIT

NCS36510 has an advanced PMU supporting two voltage supply modes: 3 V and 1 V, and four operating modes: Run, Sleep, Deep Sleep, and Coma.

PRE−REGULATOR

In 3 V mode the V3V voltage is pre−regulated to a voltage of about 1.1 V. The default voltage regulator is the linear regulator. The application is responsible for controlling the switching regulator, including monitoring the V3V voltage with the internal voltage sensor. The switching regulator is only allowed if V3V > 2.6 V.

In 1 V mode, the pre−regulator is disabled. Connecting the V3V and V1VO/I pins to 1 V will automatically generate an internal logic signal and the system will be configured in 1 V mode.

Warning: Connecting V1VO/I to V3V when V3V is greater than the absolute maximum rating for the V1VO/I domains will result in damage to NCS36510.

The pre−regulator voltage is split into two pins, V1VO (V1V Output), and V1VI (V1V Input). Between these pins a power supply filter must be put on the application board to suppress the switching regulator noise. Throughout this document this pre−regulator voltage may be referred to as simply V1V. The user has the responsibility to filter this voltage as specified to obtain the published performance specifications.

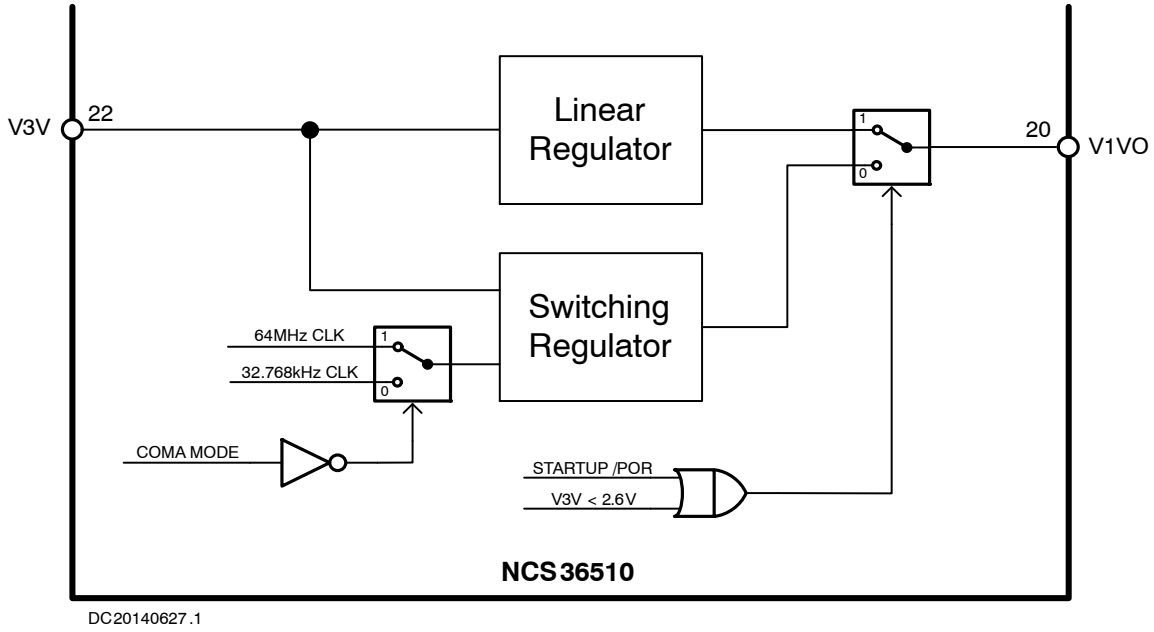


Figure 10. Pre−Regulator System

SYSTEM OF LINEAR REGULATORS

The pre−regulator voltage (V1V) is the input voltage (V1VI) for an array of internal linear regulators that are automatically enabled and disabled in the appropriate modes to minimize power consumption. These internal regulators supply the internal analog and digital blocks.

Warning: The DVDD regulator is pinned out for de−coupling only. The application is not allowed to use this regulator to power anything other than the NCS36510 internal circuits.

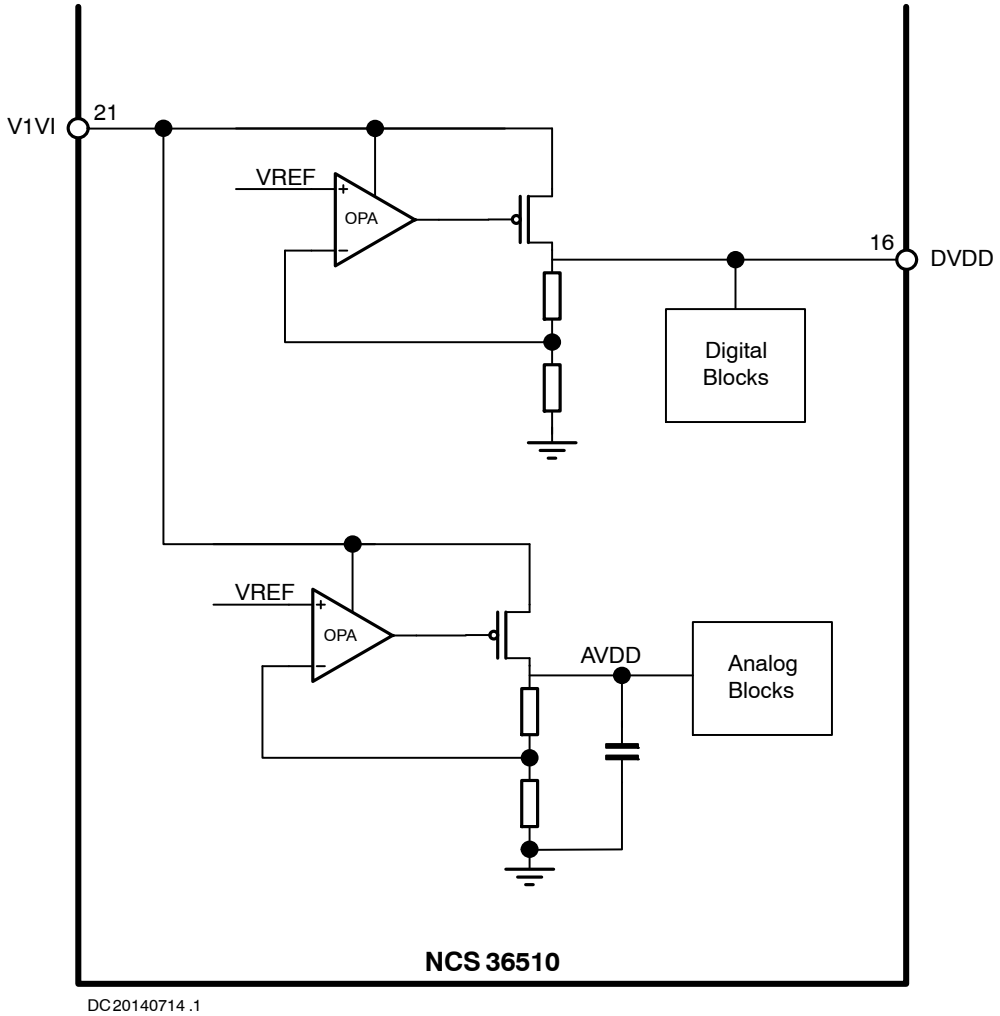


Figure 11. Linear Regulator System

EMBEDDED FLASH POWER SUPPLIES

To support the embedded FLASH two internal power supplies are implemented. One is the FVDDH, which is 1.8 V, and the other is FVDDL, which is 1.2 V.

In 3 V mode, the FVDDH is generated by a linear regulator powered by V3V. In 1 V mode, a voltage multiplier is used to boost the V3V input voltage to the required level.

The FVDDH voltage is split into two pins, FVDDHO (FVDDH Output), and FVDDHI (FVDDHI Input). Between these pins a power supply filter must be put on the application board to suppress the voltage multiplier noise. Throughout this document this voltage may be referred to as simply FVDDH. The user has the responsibility to filter this voltage as specified to obtain the published performance specifications.

In either 3 V or 1 V modes the FVDDL voltage is generated by a linear regulator from FVDDHI.

Warning: The application is not allowed to use this regulator to power anything other than the NCS36510 internal circuits.

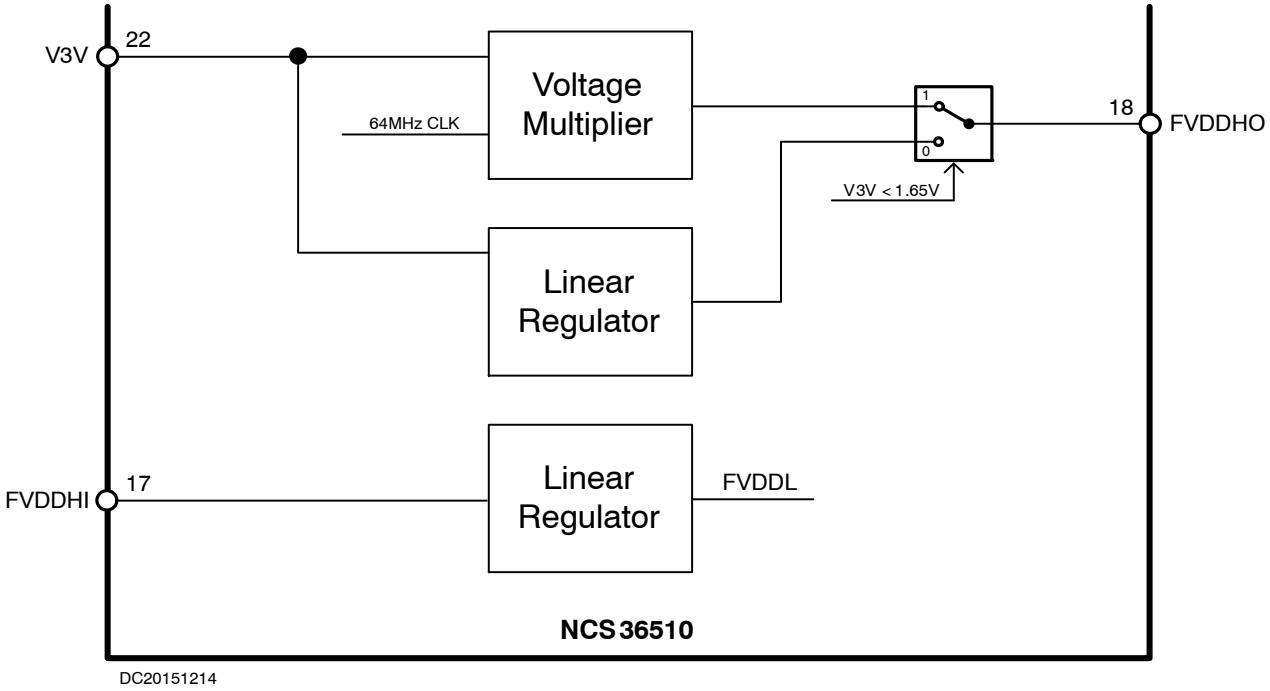


Figure 12. Flash Regulator System

OPERATING MODES

Operating runs are selected by software as highlighted below.

- Run
- Sleep
- Deep Sleep
- Coma

Table 6. POWER MODES

Mode	Digital	FLASH	Retention SRAM A	Retention SRAM B	32 MHz Clock
Run	ON	ON	ON	ON	ON
Sleep	ON	ON	ON	ON	ON
Deep Sleep	ON	OFF	ON	ON	ON
COMA	OFF	OFF	Programmable	Programmable	OFF

The software application needs to decide when to enter any of the sleep modes.

RUN MODE

In run mode all digital systems are powered and running including external and/or internal oscillators. The processor is executing code.

SLEEP MODE

Sleep mode is the same as run mode except the processor clock is gated. Since the processor clock is gated, the processor is not executing code. When an interrupt is detected, the processor enters run mode and executes code starting from the last known location.

DEEP SLEEP MODE

Deep sleep mode is the same as sleep mode except the FLASH memories are also powered down. Since the processor clock is gated, the processor is not executing code. When an interrupt is detected, the FLASH memories are powered up and the processor enters run mode and executes code starting from the last known location.

COMA MODE

In coma mode, only retention registers are powered in the digital system. All processor, trim, and peripheral registers retain their values. The high speed oscillator(s) are powered down. The low speed oscillator clocks the CPU. The processor clock is gated and waiting for an interrupt. When an interrupt is received, the FLASH memory and remaining digital systems will power up and the processor will enter run mode and start executing code from the location, just after where the power saving mode was entered. The processor will stall until the FLASH memories are properly powered. What FLASH banks are powered is decided upon the FLASH power settings in the FLASH control block, managed by the software FLASH driver.

ELECTRICAL CHARACTERISTICS

Table 7. ABSOLUTE MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
V3V Pin Voltage		−0.3 to 3.9	V
VPA Pin Voltage		−0.3 to 3.9	V
VDDIO Pin Voltage		−0.3 to 3.9	V
DVDD Pin Voltage		−0.3 to 1.8	V
FVDDHI/FVDDHO Pin Voltage		−0.3 to 2.38	V
V1VO/V1VI Pin Voltage		−0.3 to 2.0	V
Digital Pin Voltage (Note 1)		−0.3 to VDDIO+0.3, ≤ 3.9	V
Analog Pin Voltage (Note 2)		−0.3 to V3V+0.3, ≤ 3.9	V
Crystal Pin Voltage (Note 3)		−0.3 to DVDD+0.3, ≤ 1.8	V
RX Pin Voltage		−0.3 to VPA+0.3, ≤ 3.9	V
TX Pin Voltage		−0.3 to VPA+0.3, ≤ 3.9	V
RFPWR Pin Voltage		−0.3 to VPA+0.3, ≤ 3.9	V
Maximum Junction Temperature	$T_{J(max)}$	125	°C
Storage Temperature Range	T_{STG}	−40 to 125	°C
ESD Capability, Human Body Model (Note 4)		2000	V
ESD Capability, Charged Device Model (Note 5)		500	V
Latchup Current Level (Note 6)		100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. GPIO[17:0], RESETN, DBG_TEST_EN
2. A0, A1, A2, A3
3. X32KI, X32KO, X32MI, X32MO
4. ESD Human Body Model tested per JEDEC JS−001−2012.
5. ESD Charged Device Model tested per JEDEC JESD22−C101.
6. JESD78 Rev. D at Room Temperature.

Table 8. NORMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
V3V Supply Voltage – 3 V Mode	V3V3	2.0	3.0	3.6	V
V3V Supply Voltage – 1 V Mode (connected to V1V)	V3V1	1.0	1.15	1.6	V
VPA Supply Voltage	VPA	1.0	3.0	3.6	V
VDDIO Supply Voltage	VDDIO	1.0	3.3	3.6	V
V1V Supply Voltage (Note 7)	V1V	1.0	1.15	1.6	V
Ambient Temperature	T_A	−40	27	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. V1V is only an input in 1 V mode

Table 9. ELECTRICAL CHARACTERISTICS
For typical values T_A = 27°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted.
Power supplies V3V = VPA = 3 V, VDDIO = 3.3 V, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
COMA MODE SLEEP CURRENT						
Coma Mode Sleep Current (Note 8)	1 V Mode (Note 9) 3 V Mode, Switching Regulator 3 V Mode, Linear Regulator (Note 10)			1.0 0.65 4.96		μA

8. Coma mode = CPU running on internal 32 kHz osc and waiting for interrupt, both retention RAMS disabled, all other functions powered down
9. V1V = V3V = VPA = 1.0 V
10. V3V = VPA = 2.0 V

COMA MODE LEAKAGE CURRENT						
Coma Mode Leakage Current (Notes 9 and 11)	1 V Mode			0.18		μA

11. Coma mode = No clock present, CPU static, both retention RAMS disabled, all other functions powered down.

RF POWER CONSUMPTION						
1V Mode Transmit Current (Notes 12, 13 and 14)	+2.6 dBm (Max. Power Setting) 0 dBm −16 dBm (Min. Power Setting)			6.9 6.7 4.7		mA
3V Mode Transmit Current – Switching Regulator (Notes 12, 13 and 14)	+7.6 dBm (Max. Power Setting) 0 dBm −16 dBm (Min. Power Setting)			14.3 7 2.64		mA
3V Mode Transmit Current – Linear Regulator (Notes 12, 13 and 14)	+7.6 dBm (Max. Power Setting) 0 dBm −16 dBm (Min. Power Setting)			16.2 9 4.7		mA
1V Mode Receive Current (Notes 12 and 14)				6.6		mA
3V Mode Receive Current (Notes 12 and 14) – Switching Regulator				3.6		mA
3V Mode Receive Current (Notes 12 and 14) – Linear Regulator				6.5		mA

12. Peripherals disabled, CPU halted, 32 MHz crystal oscillator, CW Mode, 2.44GHz
13. Transmit power depends on RF matching circuit
14. ON Semiconductor evaluation board, TX and RX pins connected together, conducted measurement, 50Ω system

CPU POWER CONSUMPTION						
CPU power consumption, offset value “b”	CPU current = (Clock Freq MHz)*m + b			575		μA
CPU power consumption, slope value “m”	CPU current = (Clock Freq MHz)*m + b			142		μA/MHz
32MHz CPU power consumption				5.11		mA
16MHz CPU power consumption				2.9		mA
8MHz CPU power consumption				1.71		mA
4MHz CPU power consumption				1.12		mA

15. Measured by forcing DVDD to 1.0V while running demo application, does not include VDDIO current

MODE SWITCHING TIMES						
RUN to COMA (Note 16)				2		μs
RUN to DEEP SLEEP (Note 16)				2		μs
COMA to RUN (Note 16)				400		μs
DEEP SLEEP to RUN (Note 16)				200		μs
COMA to DEEP SLEEP (Note 16)				200		μs

16. Measured using demo application on ON Semiconductor reference design, using GPIOs and power supply current to estimate mode switching times

Table 9. ELECTRICAL CHARACTERISTICS
For typical values T_A = 27°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted.
Power supplies V3V = VPA = 3 V, VDDIO = 3.3 V, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
GENERAL						
RAM − Total	3 banks of 16 kB RAM, up to two banks retained in COMA mode		16		48	kB
FLASH − Total	2 banks of 320 kB FLASH, independent power controls		320		640	kB
FLASH Erase Cycles Before Failure (Note 17)			10k			cycles
FLASH Read Current (Note 17)					2.3	mA
FLASH Erase Current (Note 17)					5	mA
FLASH Write Current (Note 17)					3	mA
Data Retention at 85°C			10			years

17. Guaranteed by design.

RF RECEIVER						
1V Mode Receive Sensitivity (Notes 18 and 21)	Maximum of −85 dBm at a PER of 1% as defined by (Note 19)			−99		dBm
3V Mode Receive Sensitivity − Linear Regulator (Notes 18 and 21)	Maximum of −85 dBm at a PER of 1% as defined by (Note 19)			−99		dBm
3V Mode Receive Sensitivity − Switching Regulator (Notes 18 and 21)	Maximum of −85 dBm at a PER of 1% as defined by (Note 19)			−98		dBm
Saturation (Note 18)	Maximum of −20 dBm at a PER of 1% as defined by (Notes 19, 20)		−20			dBm
High−Side Adjacent Channel Rejection (Note 18)	Signal at −82 dBm, O−QPSK modulated interferer ±5 MHz, PER of 1% as defined by (Note 19) Minimum of 0dB required by (Note 19)			30		dB
Low−Side Adjacent Channel Rejection (Note 18)	Signal at −82 dBm, O−QPSK modulated interferer ±5 MHz, PER of 1% as defined by (Note 19) Minimum of 0 dB required by (Note 19)			32		dB
High−Side Alternate Channel Rejection (Note 18)	Signal at −82 dBm, O−QPSK modulated interferer ±10 MHz, PER of 1% as defined by (Note 19) Minimum of 30dB required by (Note 19)			34		dB
Low−Side Alternate Channel Rejection (Note 18)	Signal at −82 dBm, O−QPSK modulated interferer ±10 MHz, PER of 1% as defined by (Note 19) Minimum of 30dB required by (Note 19)			37		dB
Co−channel Rejection (Note 18)	Signal at −82 dBm, O−QPSK modulated interferer, PER of 1%			−5		dBC
Image Rejection	Signal at −82 dBm, CW interferer, PER of 1%			6		dBC
RSSI dynamic range (Note 18)	Energy Detect − Minimum of 40 dB required by (Note 19)			80		dB
RSSI Accuracy (Note 18)	Energy Detect − Maximum of ±6 dB required by (Note 19)			±3		dBm
Spurious Emissions 1GHz to 12.75GHz (LO Leakage) (Note 18)	Radiated Measurement, converted to dBm ETSI EN 300 328 Requirement is −47dBm			−69		dBm

Table 9. ELECTRICAL CHARACTERISTICS
For typical values T_A = 27°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted.
Power supplies V3V = VPA = 3 V, VDDIO = 3.3 V, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RF RECEIVER						
Frequency Error Tolerance (Note 22)				±100		ppm

18. ON Semiconductor evaluation board, TX and RX pins connected together, conducted measurement, 50 Ω system.
19. IEEE 802.15.4 Standard.
20. Maximum saturation level not yet characterized
21. 2.48 GHz
22. Difference between center frequency of the received RF signal and LO frequency, measured on ON Semiconductor bench evaluation board.

RF TRANSMITTER						
Carrier Offset (Note 18)	At maximum recommended power setting as defined by (Note 19) Maximum of ±40 ppm as required by (Note 19)			2		ppm
1 V Mode – Maximum Output Power (Note 18)	Conducted measurement, 50 Ω load Minimum of −3 dBm as required by (Note 19)			2.6		dBm
3 V Mode – Maximum Output Power (Note 18)	Conducted measurement, 50 Ω load Minimum of −3 dBm as required by (Note 19)			7.6		dBm
Minimum Output Power (Note 18)	Conducted measurement, 50 Ω load			−16		dBm
Error Vector Magnitude (Note 18)	At maximum recommended power setting as defined by (Note 19) Maximum of 35% as required by (Note 19) 3 V mode with switching regulator enabled			14	25	%
Spurious Emissions (Note 18), Worst Case Requirement	Maximum power setting, conducted measurement, 50 Ω load 3 V Mode with switching regulator enabled −41.23 dBm required for (Note 23) Limit 54 dBμV/m = −41.23 dBm EIRP (Note 24)			−46		dBm

23. FCC Part 15.247, ETSI EN 300 440, ETSI EN 300 328
24. Field strength to dBm converter: http://www.compeng.com.au/radiated−power−calculator/

EXTERNAL OSCILLATOR – 32.768 kHz						
Crystal frequency				32.768		kHz
Accuracy requirements			−100		100	ppm
ESR					80	kΩ
Crystal shunt capacitance (C0)					2.0	pF
INTERNAL OSCILLATOR – 32.768 kHz						
Uncalibrated			26	36	47	
Calibrated frequency			32.68	32.768	32.85	kHz
EXTERNAL OSCILLATOR – 32 MHz						
Crystal frequency				32		MHz
Accuracy requirements			−30		30	ppm
ESR					50	Ω
Crystal shunt capacitance (C0)					2.0	pF
INTERNAL OSCILLATOR – 32 MHz						
Uncalibrated frequency			28	32	41	MHz
Calibrated frequency			31	32	33	MHz
10b SAR ADC						
Conversion time				5		μs

Table 9. ELECTRICAL CHARACTERISTICS
For typical values T_A = 27°C, for min/max values T_A = −40°C to 85°C; unless otherwise noted.
Power supplies V3V = VPA = 3 V, VDDIO = 3.3 V, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
10b SAR ADC						
INL (Note 18)	No averaging, 16 samples averaged			6, 4		Codes
DNL (Note 18)	No averaging, 16 samples averaged			4, 1		Codes
TEMPERATURE SENSOR						
−40C Value (Note 25)				777		Codes
+30C Value (Note 25)				664		Codes
+85C Value (Note 25)				546		Codes
Uncalibrated Accuracy (Note 26)				+/−5		°C

25. From Automated Test Equipment (ATE)
26. Guaranteed by design.

POR/BROWNOUT						
Reset trip points (Note 27)	Trip high (POR) Trip Low (Brownout)			0.654 0.651		V

27. V1V power domain.

DIGITAL I/O						
Highest input voltage recognized as a logic low		V_{IL}			0.3 * VDDIO	V
Lowest input voltage recognized as a logic high		V_{IH}	0.7 * VDDIO			V
Input leakage	VDDIO = 2.97 V			3		nA
Input hysteresis (Note 30)		V_{hyst}	375	411	650	mV
Logic high source current, I_{OH}	VDDIO = 3.3 V Pad driven to V_{OH} = 0.8 * VDDIO	I_{OH3V0} I_{OH3V1} I_{OH3V2} I_{OH3V3}	−1.5 −3 −5.5 −12	−1 −2 −4 −8	−0.8 −1.7 −3.1 −6	mA
Logic low sink current, I_{OL}	VDDIO = 3.3 V Pad driven to V_{OL} = 0.2 * VDDIO	I_{OL3V0} I_{OL3V1} I_{OL3V2} I_{OL3V3}	1 2.25 4.25 8.1	1.6 3.1 6 11.6	2.25 4.25 8 15	mA
Pullup/Pulldown Resistance (Notes 28 and 29)			8	10	12	kΩ

28. RESET pin has a fixed pullup
29. DBG_TEST_EN has a fixed pulldown
30. Guaranteed by design.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – RECEIVER

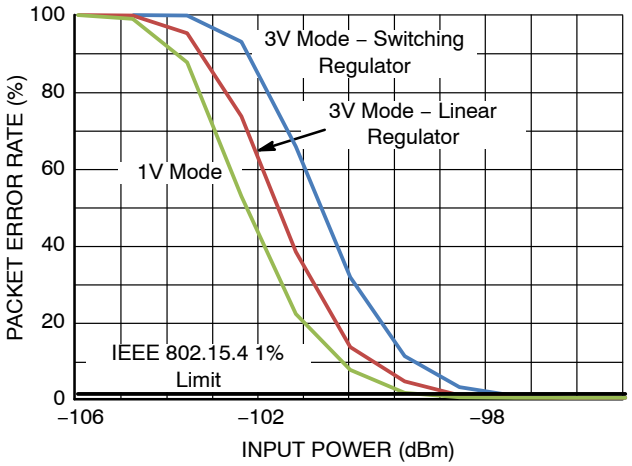


Figure 13. Packet Error Rate

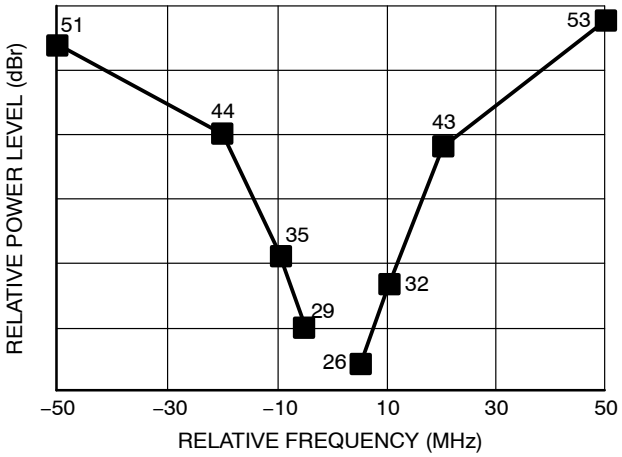


Figure 14. CW Mode Blocking / De−sensitization, 2.44 GHz

TYPICAL CHARACTERISTICS – TRANSMITTER 3 V MODE

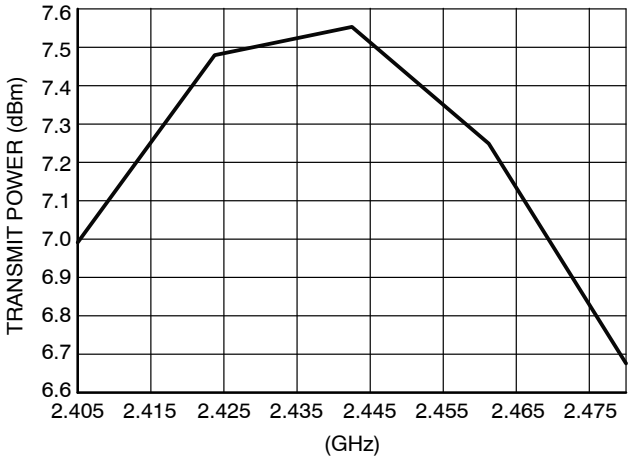


Figure 15. 3 V Mode with Switching Regulator Transmitter Output Power in CW Mode at Maximum Power

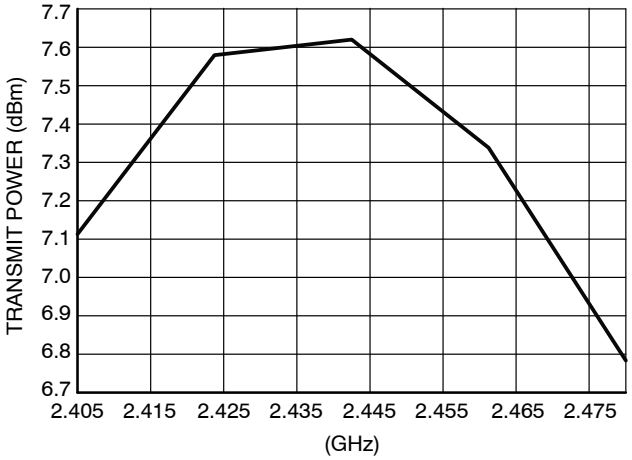


Figure 16. 3 V Mode with Linear Regulator Transmitter Output Power in CW Mode at Maximum Power

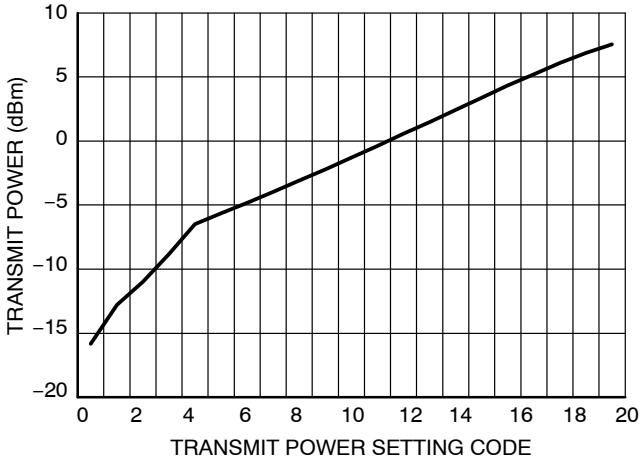


Figure 17. 3 V Mode with Switching Regulator Trasmit Power in CW Mode, 2.4425 Hz

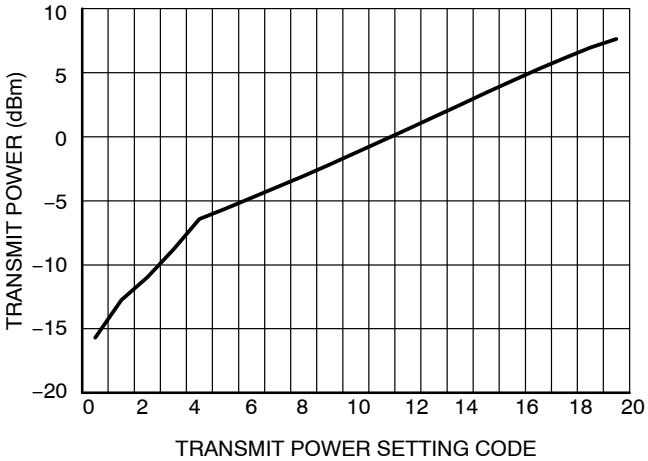


Figure 18. 3 V Mode with Linear Regulator Transmit Power in CW Mode, 2.4425 GHz

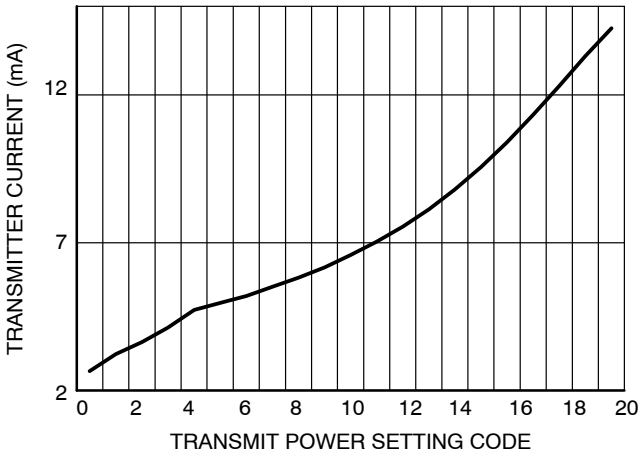


Figure 19. 3 V Mode with Switching Regulator Transmitter Current versus Power Setting, 2.4425 GHz

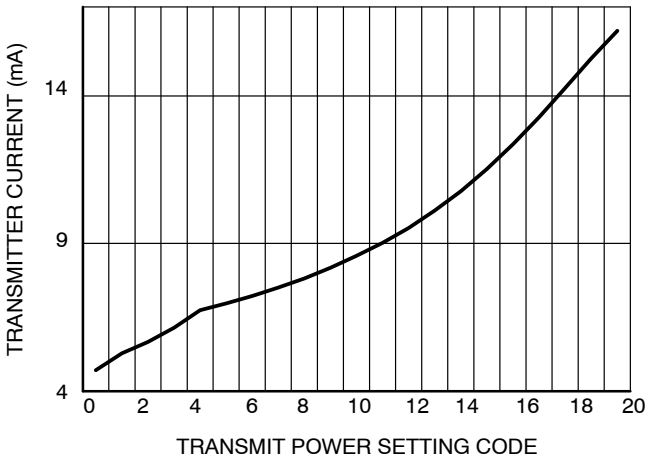


Figure 20. 3 V Mode with Linear Regulator Transmitter Current versus Power Setting, 2.4425 GHz

TYPICAL CHARACTERISTICS – TRANSMITTER 1 V MODE

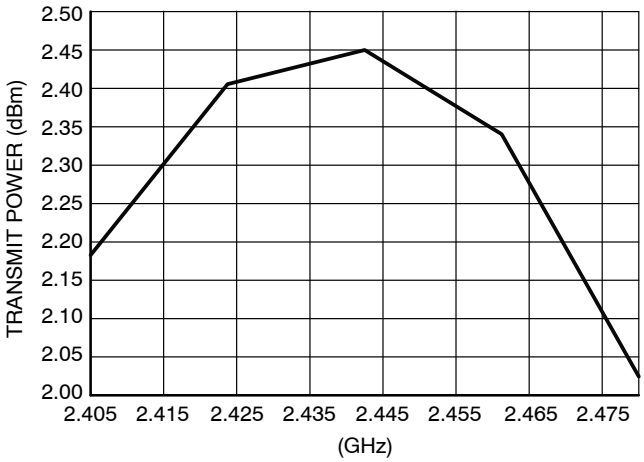


Figure 21. 1 V Mode Transmitter Output Power in CW Mode

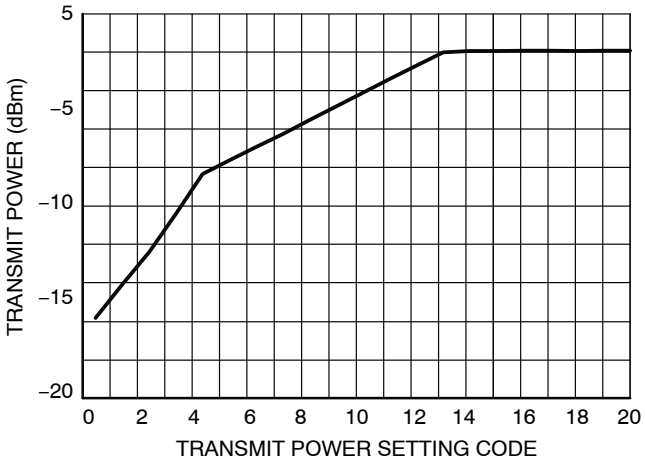


Figure 22. 1 V Mode Transmit Power in CW Mode, 2.4425 GHz

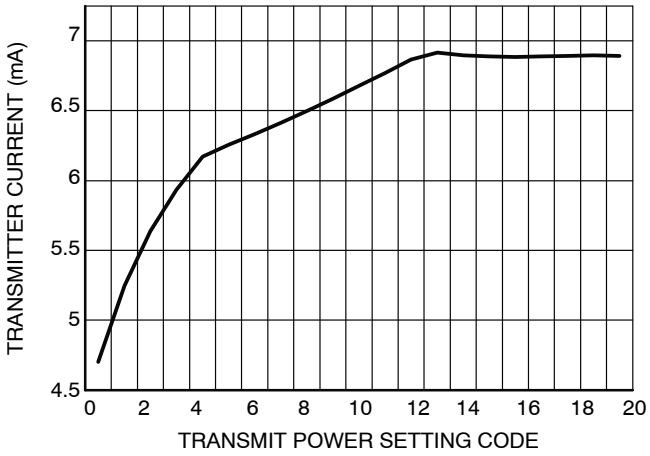


Figure 23. 1 V Mode Transmitter Current versus Power Setting

APPLICATION SECTION

TYPICAL APPLICATION DIAGRAMS

Application drawings for 3 V and 1 V mode systems and their recommended components are shown below. Because the RF matching components are system dependent their values are not specified.

VDDIO and V3V/VPA supplies are normally connected in battery powered applications. In other systems, it's common to run the VDDIO at 3.3 V to interface to other digital chips in the system. The NCS36510 will work properly at 3.3 V or any other voltage that is within specification to provide maximum application power supply flexibility.

The back of the NCS36510 package has an exposed conductive pad that is required to be soldered to a ground plane for proper operation. This pad is the ground for all of the power domains on NCS36510, including the RF circuitry.

3 V System

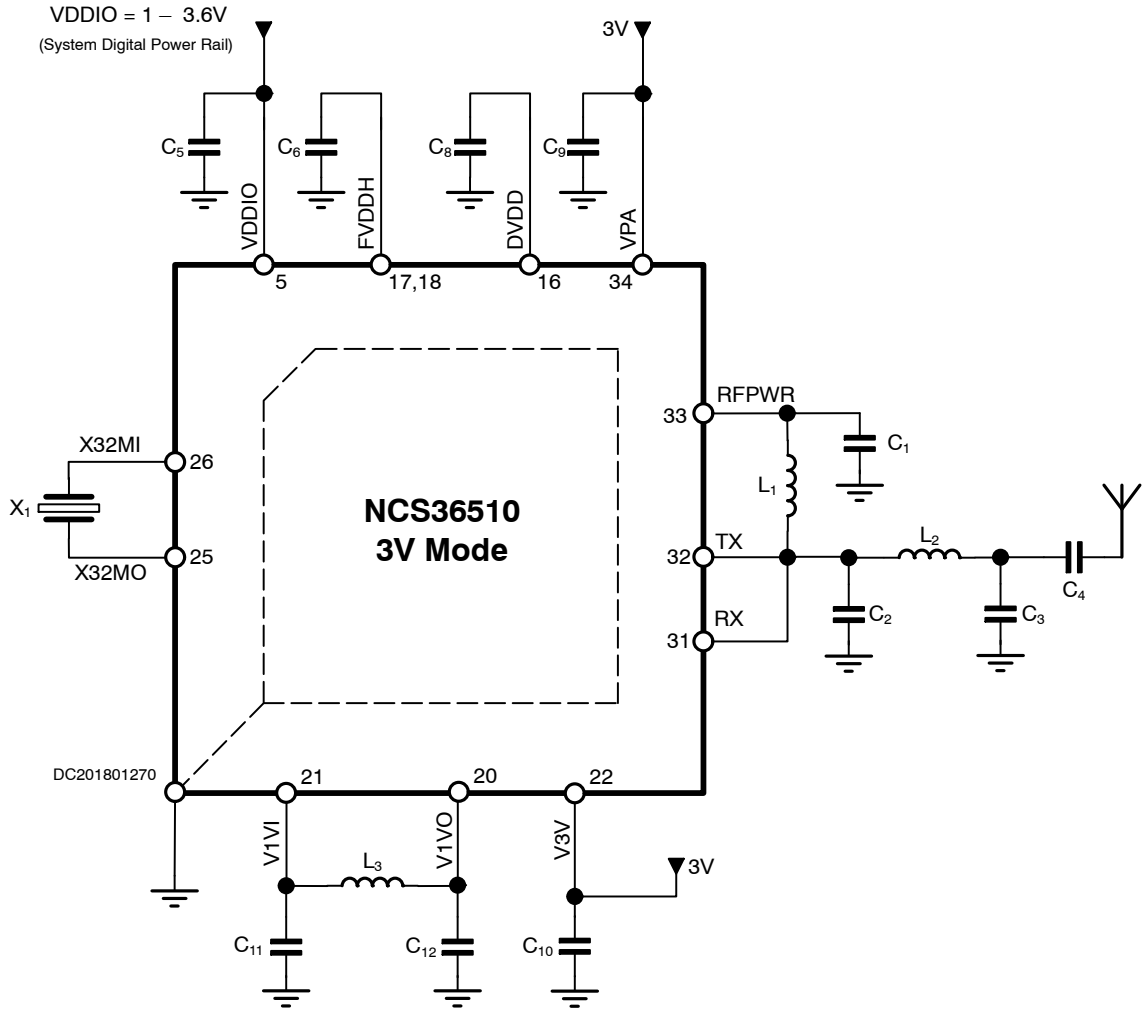


Figure 24. 3 V System Application Diagram

Table 10. COMPONENT LIST

Component	Description	Value
C_1	Decoupling RFPWR	100 pF
C_2, C_3	RF match and harmonic filter	
C_4	RF DC Block	100 pF
C_5	Decoupling VDDIO	220 nF
C_6	Decoupling FVDDH	33 nF
C_7	Decoupling FVDDL	33 nF
C_8	Decoupling DVDD	33 nF
C_9	VPA	220 nF

Table 10. COMPONENT LIST (continued)

Component	Description	Value
C_{10}	Decoupling V3V	220 nF
C_{11}, C_{12}	V1V LC filter	220 nF
L_1	RF power amplifier bias	
L_2	RF match and harmonic filter	
L_3	V1V LC filter	22 μH
X_1	32 MHz crystal	

1 V System

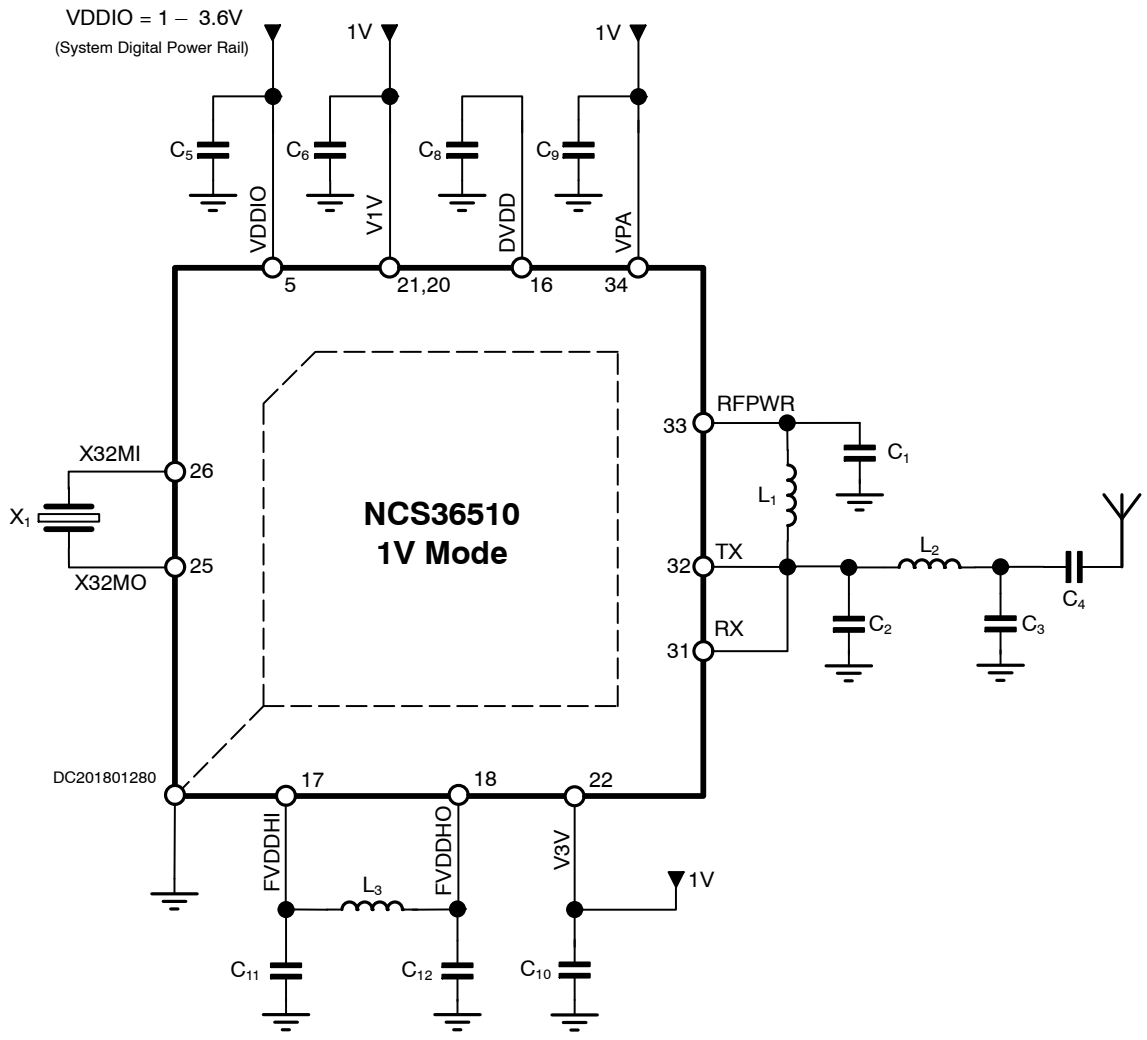


Figure 25. 1V System Application Diagram

Table 11. COMPONENT LIST

Component	Description	Value
C_1	Decoupling RFPWR	100 pF
C_2, C_3	RF match and harmonic filter	
C_4	RF DC Block	100 pF
C_5	Decoupling VDDIO	220 nF

Table 11. COMPONENT LIST (continued)

Component	Description	Value
C_6	Decoupling V1V	1 μF
C_7	Decoupling FVDDL	33 nF
C_8	Decoupling DVDD	33 nF
C_9	VPA	220 nF
C_{10}	Decoupling V3V	220 nF
C_{11}, C_{12}	FVDDH LC filter	220 nF
L_1	RF power amplifier bias	
L_2	RF match and harmonic filter	
L_3	FVDDH LC filter	22 μH
X_1	32 MHz crystal	

DEBUG PORT CONNECTION

To connect the Serial Wire Debug interface, DBG_TEST_EN pin needs to be tied to logical '1' level and the debugger pins are wired per below.

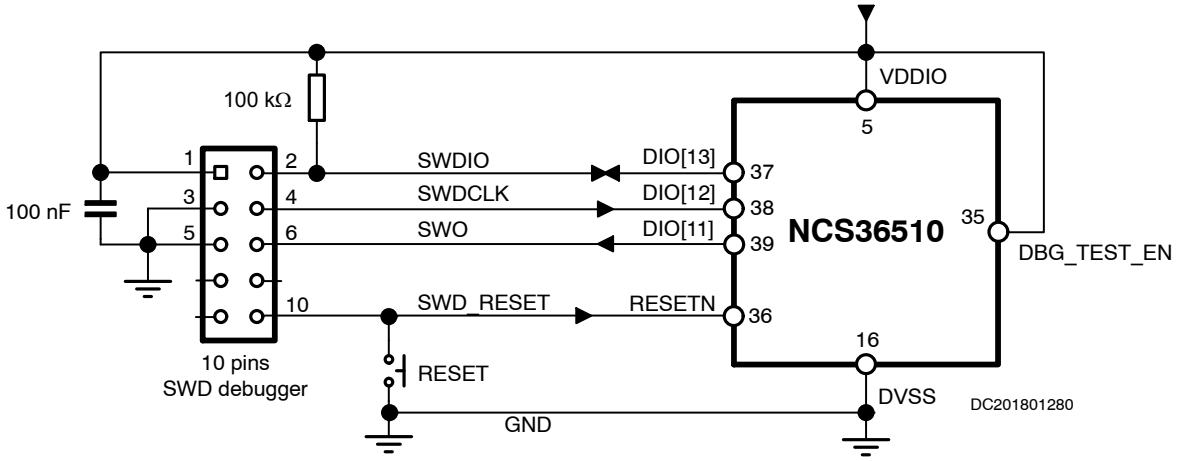


Figure 26. Debugger Connection Diagram

Table 12. DEBUGGER CONNECTIONS

DBG_TEST_EN State	Part Pin Name	Part Direction	Debugger Pin Name	Debugger Pin Number	Function
1	DIO[13]	Input/Output	SWDIO	2	Serial wire data in & out
1	DIO[12]	Input	SWCLK	4	Serial wire clock
1	DIO[11]	Output	SWO	6	Trace output
	RESETN	Input	RESETn	10	Resets the target

Note that when the debugger is connected, most of the power saving modes are disabled. Only deep sleep mode with all FLASH banks powered is supported, when the power management unit is configured accordingly.

Not all debuggers will work down to 1 V. So it's recommended to do debugging at higher voltages to maintain fast and functional operation.

Table 1. REFERENCES

Topic	Reference	Web Link
WPAN Standard	IEEE 802.15.4−2006 Standard	https://standards.ieee.org/findstds/standard/802.15.4−2006.html
CCM Encryption	NIST SP800−38C	http://csrc.nist.gov/publications/PubsSPs.html#SP 800
AES Encryption Standard	FIPS 197	http://www.nist.org/nist_plugins/content/content.php?content.39
Cryptography	Wikipedia	https://en.wikipedia.org/wiki/Block_cipher_mode_of_operation
Arm Cortex M3	Product Information and Support	http://www.arm.com/products/processors/cortex−m/cortex−m3.php
ZigBee Alliance	Website	http://www.zigbee.org/
6LoWPAN WG	Website	https://datatracker.ietf.org/wg/6lowpan/charter/
Thread Group	Website	http://threadgroup.org/
HART Communication Group	Website	http://en.hartcomm.org/main_article/wirelesshart.html

Table 2. DEFINITIONS

Abbreviation	Meaning
ACK	Refers to an acknowledge packet, part of 802.15.4
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AHB	AMBA High−performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
API	Application Programming Interface
BCD	Binary Coded Decimal
BO	Brownout − loss of power below specified operating threshold
BOM	Bill Of Materials
CBC	Cipher Block Chaining
CCM	Counter with CBC
CPU	Central Processing Unit
CSMA−CA	Carrier Sense Multiple Access with Collision Avoidance, part of 802.15.4
CTR	Counter mode
DMA	Direct Memory Access
DWT	Data Watchpoint and Trace unit
ED	Energy Detection, part of 802.15.4
ESR	Equivalent Series Resistance
ETM	Embedded Trace Macrocell
EVM	Error Vector Magnitude
FIFO	First In First Out
fips197	AES encryption standard
FPB	Flash Patch Breakpoint unit
GPIO	General Purpose I/O
I2C	Serial wire interface
IF	Intermediate frequency
IOH	Digital pad current when pad is driven to VOH
IOL	Digital pad current when pad is driven to VOL

Table 2. DEFINITIONS (continued)

Abbreviation	Meaning
ITM	Instrumentation Trace Macrocell
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LQI	Link Quality Indicator, part of 802.15.4
MAC	Medium Access Control layer
MISO	Master In Slave Out, part of I2C protocol
MOSI	Master Out Slave In, part of I2C protocol
MUX	Multiplexer
NIST	National Institute of Standards and Technology
NVIC	Nested Vectored Interrupt Controller
OTA	Over The Air
PA	Power Amplifier
PMU	Power Management Unit
POR	Power On Reset
PWM	Pulse Width Modulation
QFN	Quad Flat No Leads, package type
RF	Radio Frequency
RSSI	Receive Signal Strength Indicator
RTC	Real Time Clock
RX	Receive or Receiver
SAR ADC	Successive Approximation Register Analog to Digital Converter
SCLK	SPI Clock, part of SPI protocol
SDK	Software Development Kit
SPI	Serial Peripheral Interface
SW	Software
SWD	Serial Wire Debug
TPIU	Bridge between the ETM and ITM
TRNG	True Random Number Generator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver/Transmitter
UVI	Under−Voltage Indicator
VCO	Voltage Controlled Oscillator
VOH	Digital pad maximum output voltage of pullup driver at a current of IOH
VOL	Digital pad maximum output voltage of pulldown driver at a current of IOL
WDT	Watch Dog Timer

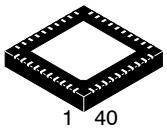
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

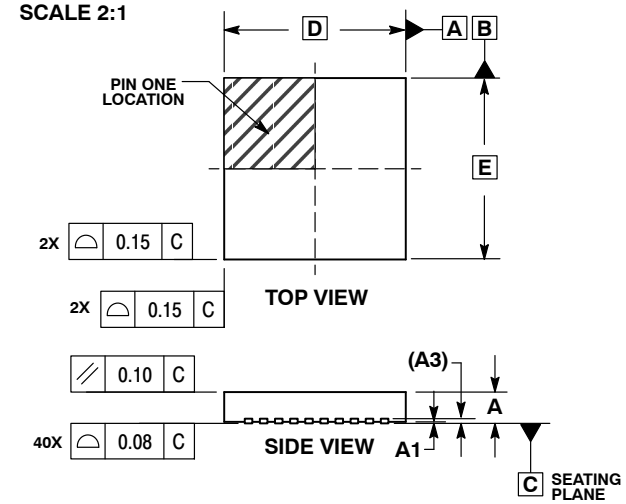
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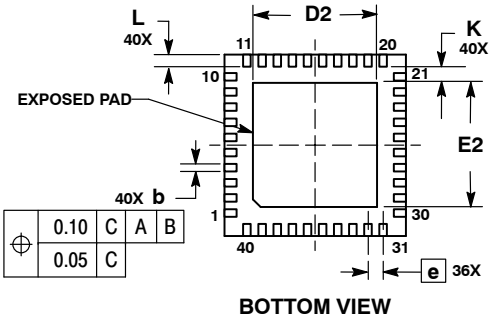
QFN40 6x6, 0.5P
CASE 488AR−01
ISSUE A

DATE 18 APR 2007



SCALE 2:1





BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	4.00	4.20
E	6.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
K	0.20	−−−

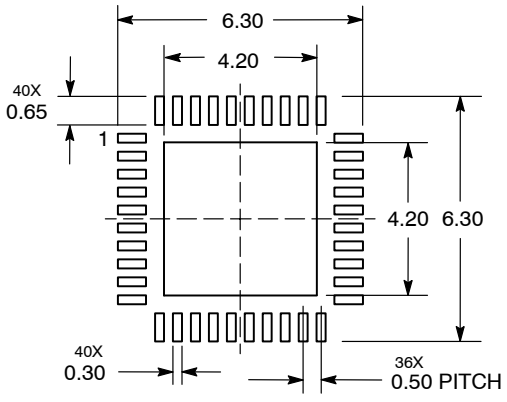
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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