# Self Test With Lockout Ground Fault Circuit Interrupter (GFCI)

# NCS37010

The NCS37010 is a fully UL943 compliant signal processor for GFCI applications with self test and lockout. The device integrates a flexible power supply (including both shunt and LDO regulators), differential fault, and grounded−neutral detection circuits. Proprietary impedance measurement and signal processing techniques are used to minimize the number of external components and improve performance. The device also includes a specialized DSP controller that offers best in class immunity to nuisance loads without the need for external analog filters. At power up the NCS37010 performs a self test at 60ms and removes the lockout if the test passes. This self test consists of a differential, ground−neutral and solenoid test.

### Features

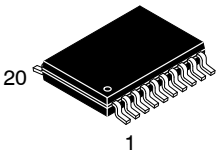
- 6.0 – 12 V Operation (120 – 480 V AC Mains with the Appropriate Series Impedance)
- −40 to 85°C
- Very low power consumption: < 15 mW @ 6 V
- 16 Pin QFN or 20 Pin TSSOP Package
- Single Current Transformer (CT) Detection of Both Differential and Grounded−Neutral Faults
- Full Self Test and Trip Indicator Monitoring.
- Self Test on Power Up Enables Lockout Functionality
- Self Syncing Internal Oscillator Adjusts to AC Mains Frequency to Guarantee Full Resolution on 50 and 60 Hz Distribution Systems
- Optimized Solenoid Deployment (Coil is Not Energized Near the AC Mains Zero Crossings)
- Randomized Testing Sequence to Minimize Noise and Potential Interactions on the AC Mains
- >5 mA SCR Driver for Use with High Igt SCR's for Improved Noise Immunity
- Superior Immunity to Nuisance Loads/Noise (up to 10 A) Without Loss of Detection Capability or CT Saturation
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Load Panel GFCI Breakers
- GFCI Receptacles
- In−line GFCI Circuits (Power Cords)



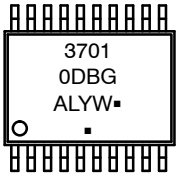

**QFN16**
**CASE 485FQ**




**TSSOP−20**
**DB SUFFIX**
**CASE 948E**

**MARKING DIAGRAMS**

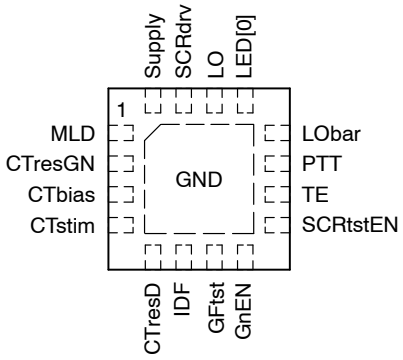



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**PIN CONNECTIONS**

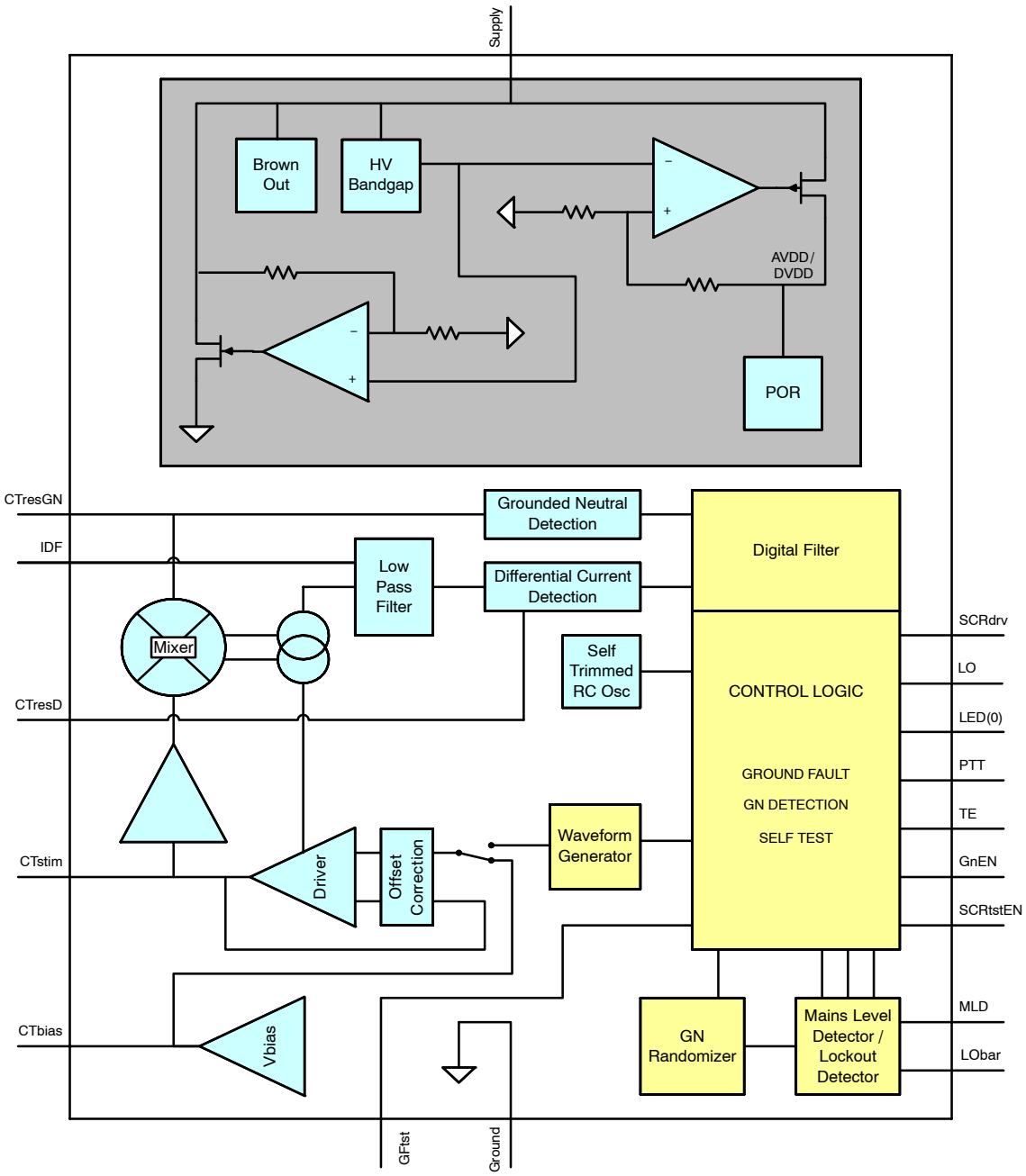



(Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 10 of this data sheet.

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GFCI ASIC

**Figure 1. Simplified Block Diagram**

## QFN PIN DESCRIPTION

| Pin # | Name | Pad Description |
|---|---|---|
| 0 | Ground | QFN center slug |
| 1 | MLD | Mains Level Detect (Zero Cross) |
| 2 | CtresGN | Determines IV converter gain for detection threshold / matched to CT turns ratio (Ground−Neutral) |
| 3 | Ctbias | Direct connection to the CT |
| 4 | Ctstim | Direct connection to the CT |
| 5 | CTresD | Determines IV converter gain for detection threshold / matched to CT turns ratio (Differential Current) |
| 6 | IDF | Front end noise filter capacitor |
| 7 | GFtst | Output to induce external differential current. |
| 8 | GnEN | Ground−Neutral fault detection enable pin. |
| 9 | SCRtstEN | SCR/solenoid self test enable pin. |
| 10 | TE | Tie to Ground or leave floating. |
| 11 | PTT | Push to test input. |
| 12 | LObar | Load monitor input. |
| 13 | LED[0] | LED[0] output driver. |
| 14 | LO | Lockout SCR output driver. |
| 15 | SCRdrv | Used to trigger the solenoid at a fault detection |
| 16 | Supply | Power supply |

## TSSOP PIN DESCRIPTION

| Pin # | Name | Pad Description |
|---|---|---|
| 1 | CTstim | Differential and ground to neutral stimulus point for the current transformer. |
| 2 | Ground | Ground connection for IC. |
| 3 | CTresD | Determines IV converter gain for detection threshold / matched to CT turns ratio (Differential Current). |
| 4 | IDF | Determines corner frequency of the differential current path filter. |
| 5 | GFtst | Output to induce external differential current. |
| 6 | GnEN | Ground−Neutral fault detection enable pin. |
| 7 | SCRtstEN | SCR/solenoid self test enable pin. |
| 8 | TE | Tie to Ground or leave floating. |
| 9 | PTT | Push to test input. |
| 10 | LObar | Load monitor input. |
| 11 | Ground | Ground connection for IC. |
| 12 | LED[0] | LED[0] output driver. |
| 13 | LO | Lockout SCR output driver. |
| 14 | SCRdrv | Used to trigger the solenoid at a fault detection. |
| 15 | DVDD | Internal digital 5 V regulated supply. |
| 16 | AVDD | Internal analog 5 V regulated supply. |
| 17 | Supply | 12V shunt regulated power supply. |
| 18 | MLD | Mains Level Detect (Zero Cross) and AM slope detect (for oscillator sync/trim and AM init) |
| 19 | CtresGN | Determines IV converter gain for detection threshold / matched to CT turns ratio (Ground−Neutral). |
| 20 | CTbias | External 2 V bias for the current transformer. |

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage Range | Vs | 6.0 to 12 | V |
| Input Voltage Range (Note 1) | $V_{in}$ | −0.3 to 6.0 | V |
| Output Voltage Range | $V_{out}$ | −0.3 to 6.0 V or ($V_{in}$ + 0.3), whichever is lower | V |
| Maximum Junction Temperature | $T_{J(max)}$ | 140 | °C |
| Storage Temperature Range | $T_{STG}$ | −65 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2 | kV |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |
| Lead Temperature Soldering<br>Reflow (SMD Styles Only), Pb−Free Versions (Note 3) | $T_{SLD}$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, QFN16, 3x3.3 mm (Note 4)<br>Thermal Resistance, Junction−to−Air (Note 5) | $R_{\theta JA}$ | 64 | °C/W |
| Thermal Characteristics, TSSOP−20 (Note 4)<br>Thermal Resistance, Junction−to−Air (Note 5) | $R_{\theta JA}$ | See note above. | °C/W |

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 $mm^2$ (or 1 $in^2$) of 1 oz copper thickness and FR4 PCB substrate.

## OPERATING RANGES (Note 6)

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | | −40 | | 85 | C |
| IDD in typical power state | | | 2 | | mA |
| Stimulus Generator Frequency | Tri−tone | 3.1 | | 3.4 | kHz |
| SCR Trigger Current | | | | 8 | mA |
| SCR Trigger output voltage | With 5 V supply | 4.5 | | 5.5 | V |
| Fault Current Sensitivity | Programmable with CTresD | 4.6 | 4.8 | 5 | mA |
| Ground Fault Response Time | 5 − 20 mA | | 150 | | ms |
| Ground Fault Response Time | 20 − 40 mA | | 75 | | ms |
| Ground Fault Response Time | >40 mA | | 25 | | ms |
| Saturation Fault Response Time | >300 mA | | 1.4 | | ms |
| CT Turns Ratio | | 200 | | 300 | |
| Ground − Neutral Detection Threshold | Total series impedance (Rn and Rg) | 3 | | 6 | Ω |
| Internal Oscillator Frequency | | | 2 | | MHz |
| CT Stimulus Current | Internally limited | | | 1 | mA |
| CT Driver Closed Loop BW | | | | 500 | KHz |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

## APPLICATIONS INFORMATION

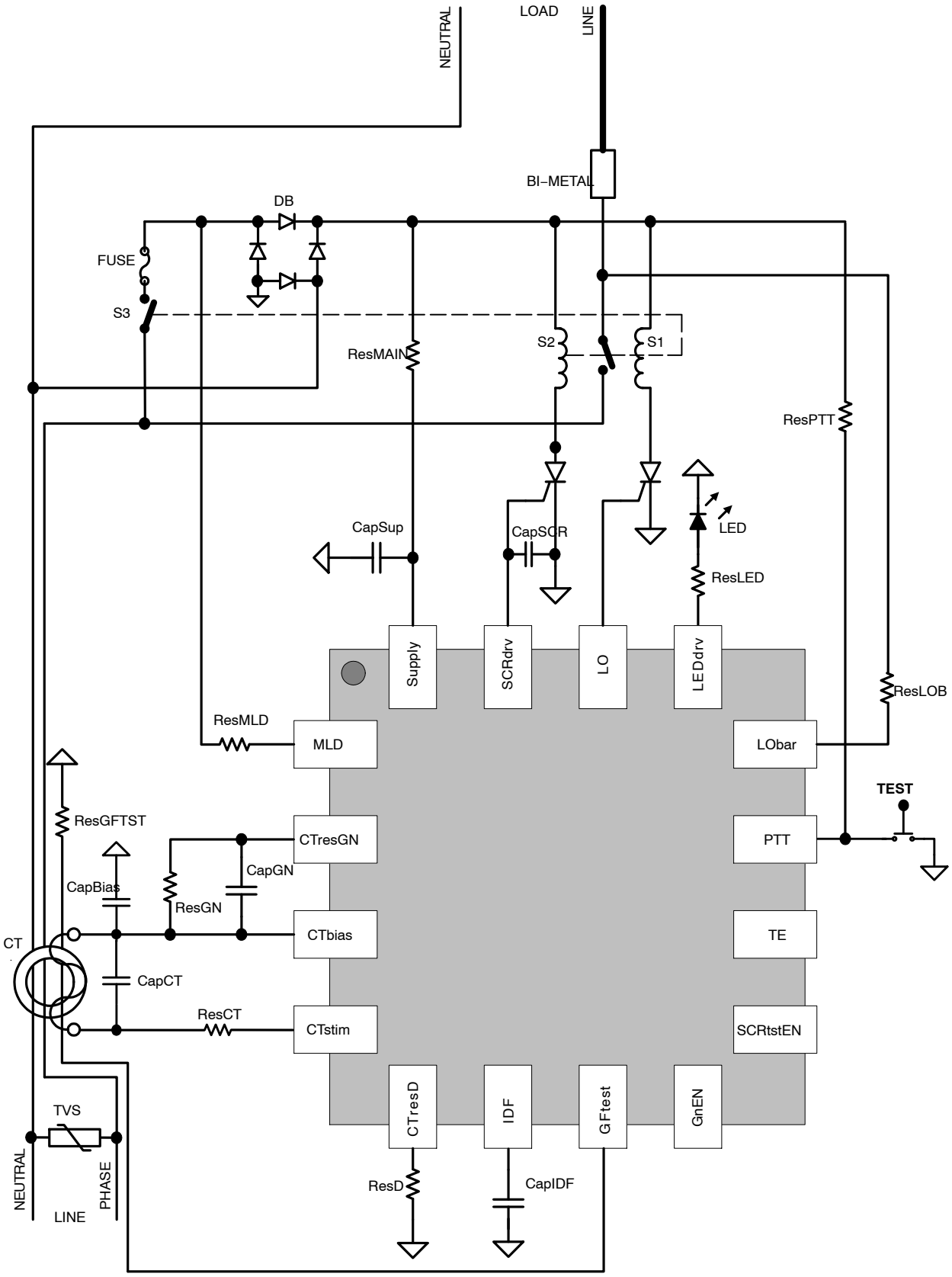



**Figure 2. Self Test GFCI Breaker with Lockout**

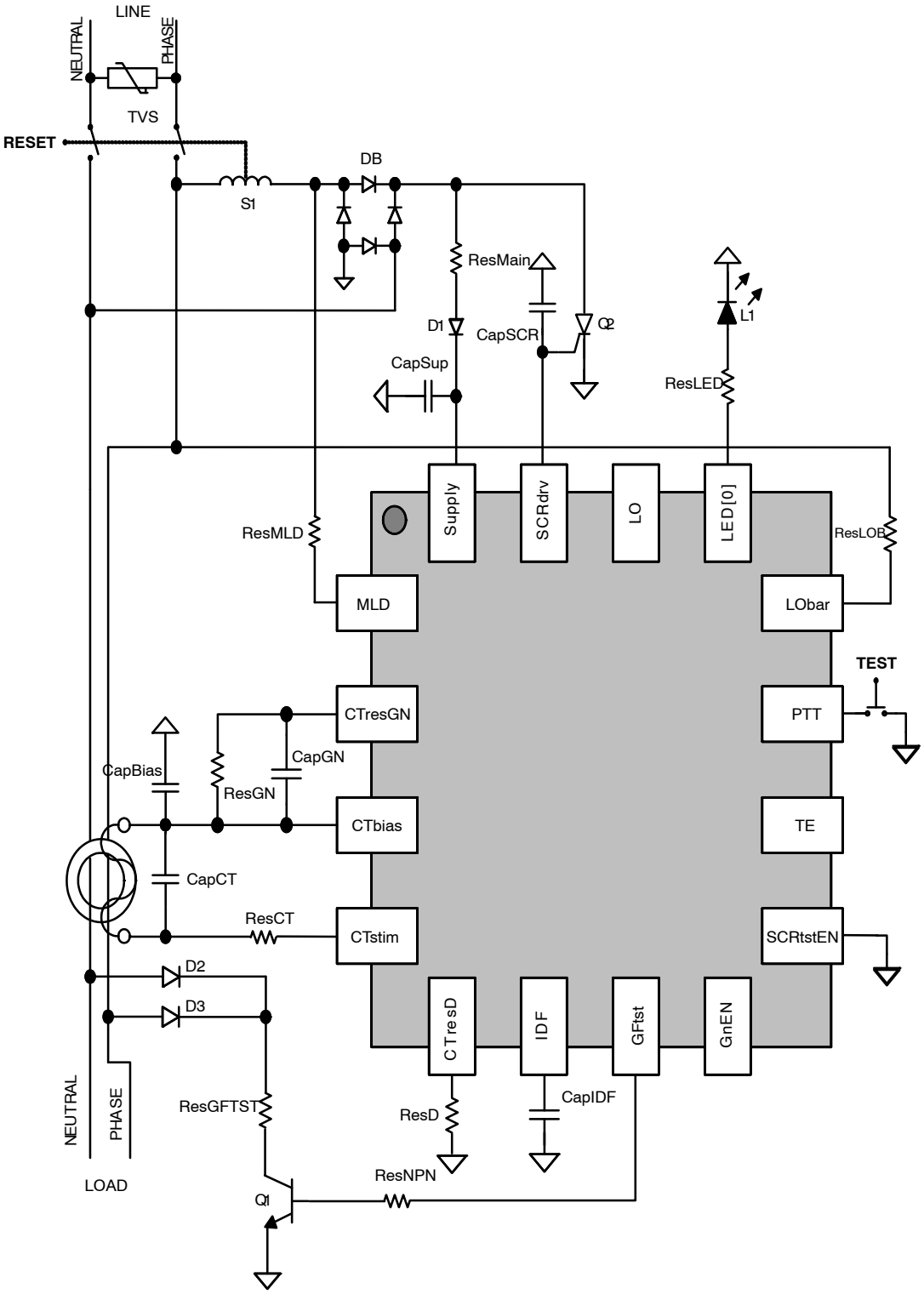



**Figure 3. Self Test GFCI Receptacle with Lockout on Power Up**

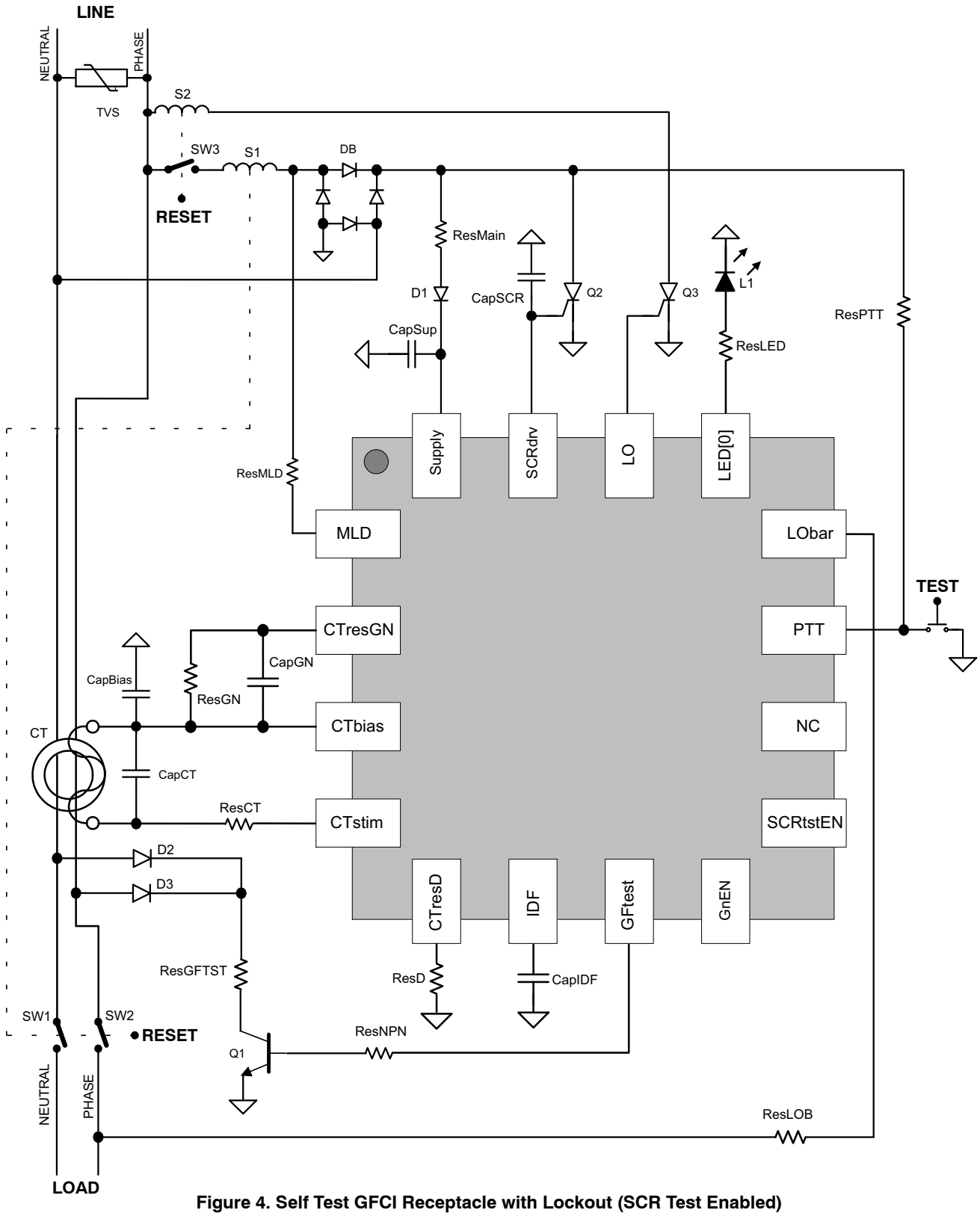



**Figure 4. Self Test GFCI Receptacle with Lockout (SCR Test Enabled)**

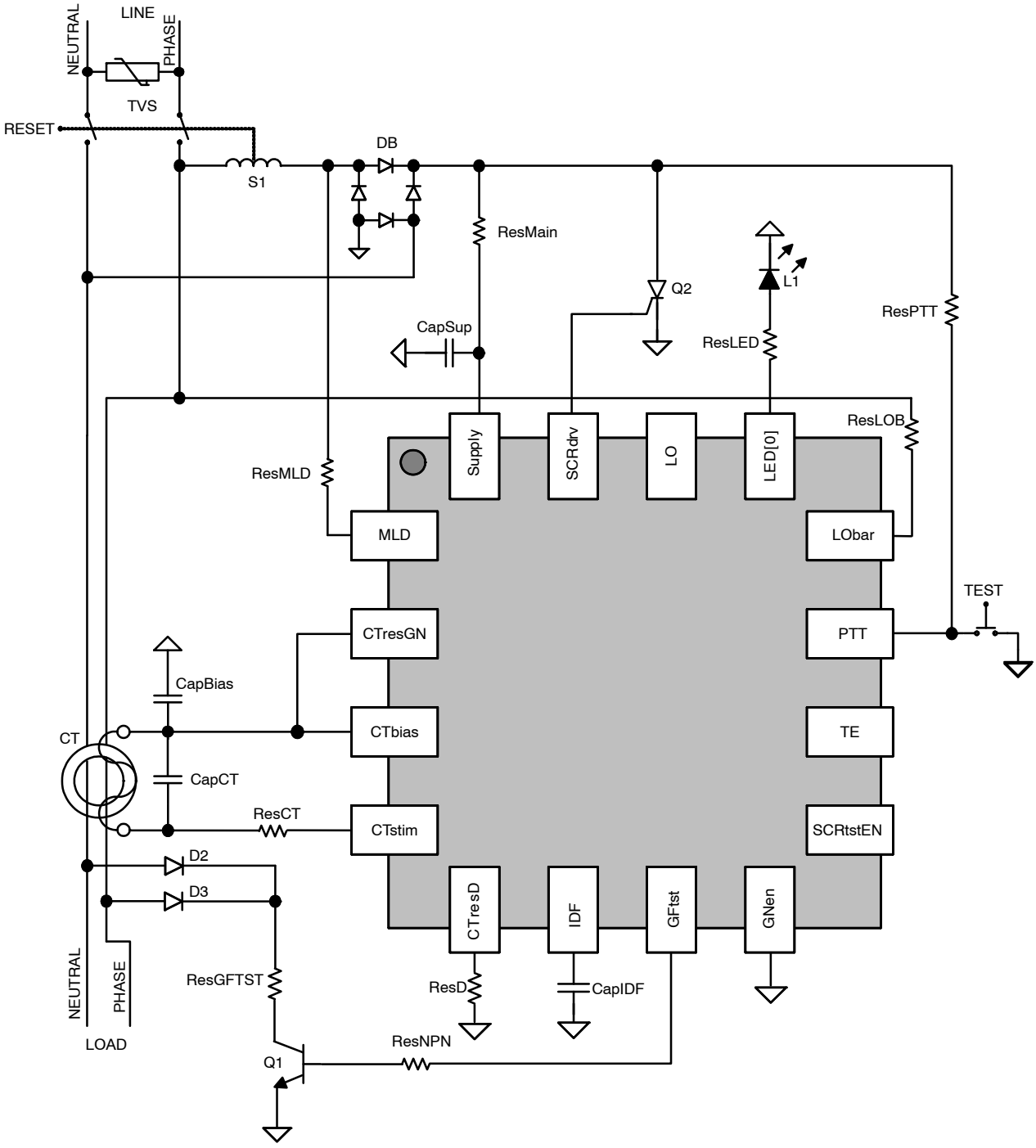



**Figure 5. Self Test GFCI Plug (Differential Only)**

**RECOMMENDED EXTERNAL COMPONENTS:**

| Component Type | Instance | Value | Note |
|---|---|---|---|
| SCR | Q2−Q3 | – | ON−MCR08 |
| Diode | Dx | – | ON−1N4007 |
| NPN | Q1 | – | ON−MMBT6517LT1G |
| NMOS | M1 | | ON−NTK3043K |
| LED | L1 | – | LED pins drive opposite polarities |
| Capacitor | CapSUP | 1 – 4.7 μF | For a full bridge rectifier |
| Capacitor | CapGN | 1 – 10 nF | Matched to current transformer |
| Capacitor | CapIDF | 220 nF | Sets the differential corner frequency at 1 kHz |
| Capacitor | CapBias | 10 nF | Filtering component for CTbias voltage. |
| Capacitor | CapCT | 2.2 – 10 nF | Filtering and resonant capacitor for CT. |
| Capacitor | CapSCR | – | Filtering component. |
| Resistor | ResD | 40 – 80k | Matched to current transformer. |
| Resistor | ResGN | 100 – 400k | Matched to current transformer. |
| Resistor | ResMLD | 400 – 800k | Limiting resistor for the Mains Level Detector (MLD) input. |
| Resistor | ResTI | 400 – 800k | Limiting resistor for the Trip Indicator(TI) input. |
| Resistor | ResMAIN | 8 – 45k | Full bridge rectifier power supply. |
| Resistor | ResGFTST | 1.3 – 30k | Sets the external differential test current (8 mA). |
| Resistor | ResLED | 1 – 5k | Sets the brightness of the LEDs. |
| Resistor | ResPTT | 400 – 800k | Needed for the SCR/Solenoid test. |
| Resistor | ResNPN | 10k | Bias resistor for NPN gate. |
| TVS | T1 | – | ~250 – 400 V |

**LED FUNCTIONS**

| Device Function | Device State | Status Indicator (Breaker) |
|---|---|---|
| Normal | No Power/ Line Load Reversed | OFF |
| | Power Up | Blink once within 3 sec (Red) |
| | Reset (Entered through PTT) | OFF |
| | Tripped | OFF |
| Abnormal | Self−Test Fails (Tripped) | OFF |
| | Self−Test Fails (Reset) | Blink (Red) |
| | No Trip on Fault | Blink (Red) |
| | Self−Test Fails to remove Lockout | Blink (Red) |

### Filtering

The analog signal capture portion of the IC includes a single pole filter that can be set externally with Cidf. This provides an additional layer of protection against false tripping under steady state noise conditions. High frequency steady state noise is common with pumps, motors or other cyclic noise generators.

$$Cidf = 220\ nF = 1\ kHz\ low\ pass.$$

For additional filtering suggestions please contact ON Semiconductor.

### Setting Trip Sensitivity

The CTresD resistor sets the threshold for the differential current fault levels. Increasing CTresD causes the fault levels to trip at lower differential currents. CT efficiency at 60 Hz must be considered.

$$CTresD = 200 * \#Turns - Subject\ CT\ efficiency\ at\ 60\ Hz$$

The CTresGN resistor sets the threshold for ground to neutral fault detection. The Rt parameter is the desired ground to neutral resistance trip level. Higher CTresGN values will cause the part to trip at higher ground to neutral impedances.

$CtresGN = \#Turns^2 * Rt / 2$ – Subject to CT efficiency from 3 kHz to 4 kHz

### Setting Grounded-Neutral response time

Cgn is used to define the response time of the grounded−neutral detection circuit. The analog portion converts the impedance into a DC voltage and a high frequency (aliased) component. The capacitor is used to remove the high frequency component leaving just the DC representation of the impedance.

$$CTcapGN = 1.8E^{-4}/CTresGN$$

### Self Test

Automatic self test will occur every 17 minutes. If a failure is observed it will be retested every second until it passes. If it fails 3 successive tests then the GFCI will indicate that it has failed self test and will trip. See the LED functions table to see the different self test indicators.

Differential ground fault test – tests the CT and the internal differential detection signal path by asserting the GFtest output high for 1 half cycle. The test will pass if a 6 – 8 mA differential current is enabled during this half wave. Greater than 20 mA current during this test will cause a fault to be detected.

Ground neutral fault test – tests the internal ground neutral stimulus and detection paths by enabling an internal 50k resistor between the CTstim and CTbias pins. If the resistor and capacitor on CTresGN are connected this will pass the GN self test.

Solenoid test – Asserts the SCRdrv output when the voltage on MLD is approximately 4 V. The PTT pin is coupled through a resistor to the output of the bridge rectifier. If the voltage at PTT drops below 2V when the SCRdrv pin is asserted then the test will pass. The SCRdrv output will be de−asserted when the test passes or when it reaches the zero crossing of the MLD pin. The Solenoid/SCR test can be disabled by tying the SCRtstEN pin to electronics ground.

### Lockout

On power−up the NCS37010 will determine connection state of the load by monitoring the LObar input pin. If the load is connected it will continue performing self test every 17 minutes and monitor for differential and GN faults.

If the load is not connected a self test will be performed at 60ms after power−up. If self test passes the connection to the load will be enabled through the LO output which will be asserted for 16 ms.

### PTT

When the PTT input pin is de−asserted for greater than 80 ms a self test will be performed. If this test is successful the SCR will be fired which will trip the GFCI unit. If the test is unsuccessful the LED[0] pin will flash indicating a failure.

### GnEN

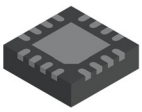
The GnEN pin if left floating will enable GN fault detection which will allow for a full UL943 GFCI. If it is tied low then GN detection will be disabled. This setting is ideal for in−line GFCI plugs and breakers that are targeted for differential detection only.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCS37010MNTWG | QFN16<br>(Pb−Free) | 3000 / Tape & Reel |
| NCS37010DBRG | TSSOP−20<br>(Pb−Free) | 2500 / Tape & Reel |

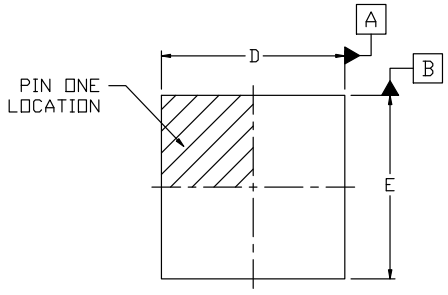
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

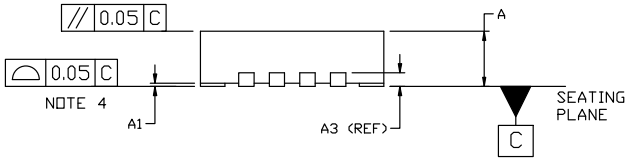


**QFN16 3x3, 0.5P**
CASE 485FQ
ISSUE B

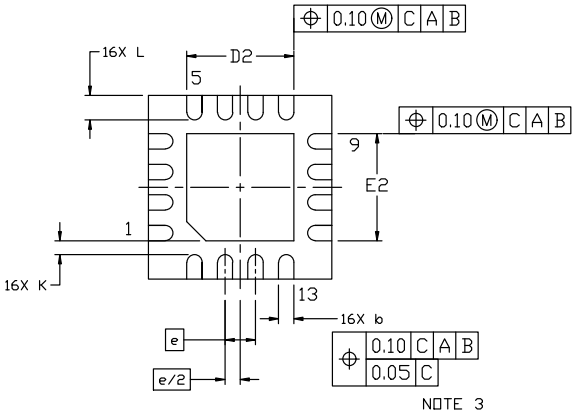
DATE 12 JUL 2022




TOP VIEW




SIDE VIEW

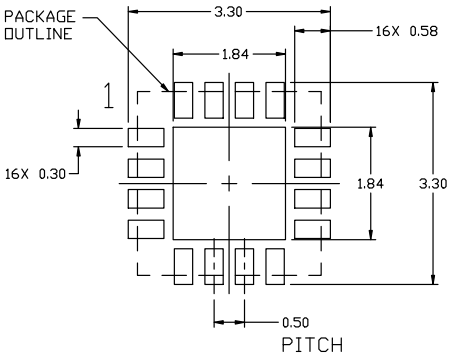



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASUREDBETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | --- | --- | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.24 | 0.30 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 1.65 | 1.75 | 1.85 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.65 | 1.75 | 1.85 |
| e | 0.50 BSC | | |
| K | 0.18 TYP | | |
| L | 0.30 | 0.40 | 0.50 |




RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON84763G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **QFN16 3x3, 0.5P** | **PAGE 1 OF 1** |

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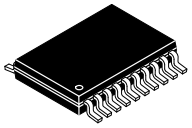
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# MECHANICAL CASE OUTLINE
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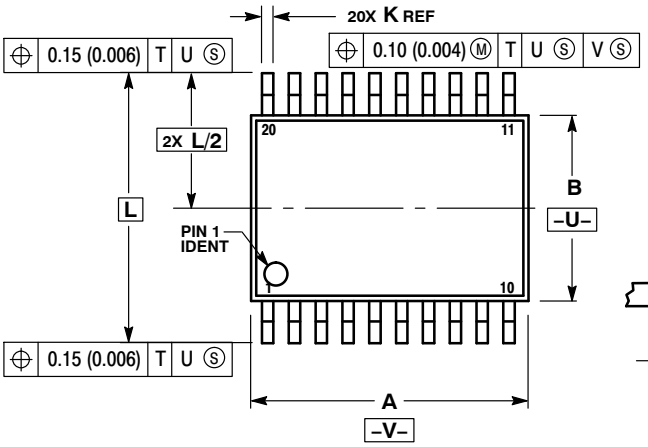
ON Semiconductor®

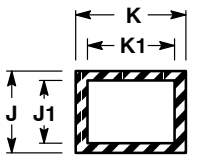
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CASE 948E
ISSUE D

DATE 17 FEB 2016

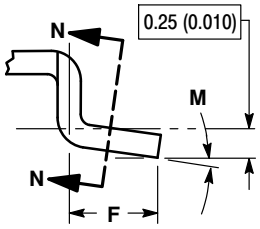


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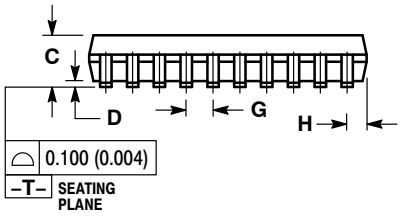


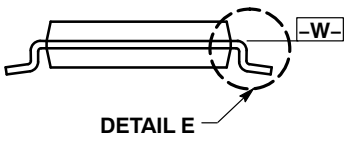




SECTION N−N




DETAIL E

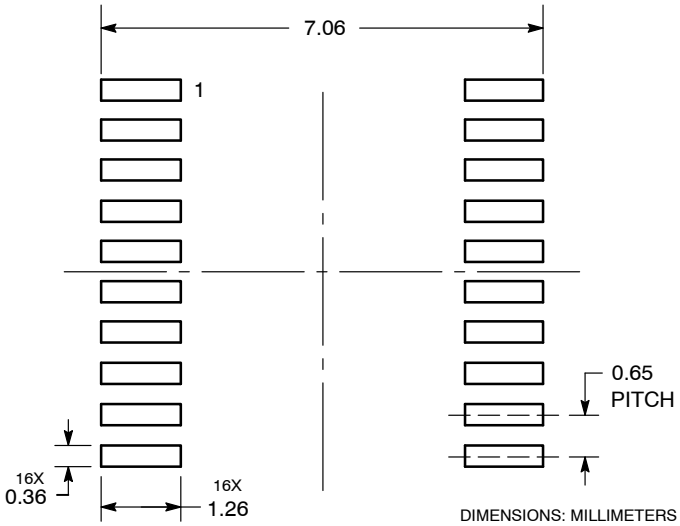



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

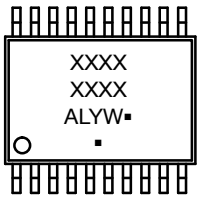
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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|---|---|---|
| DESCRIPTION: | TSSOP−20 WB | PAGE 1 OF 1 |

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