NCS5651

2 Amp PLC Line Driver

ON Semiconductor®

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1 20

QFN20
CASE 485E

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCS5651MNTXG	QFN20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part or orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Description

The NCS5651 is a high efficiency, Class A/B, low distortion power line driver. It is optimized to accept a signal from a Power Line Carrier modem. The device consists of two Operational Amplifiers (opamps).

The output opamp is designed to drive up to 2 A peak into an isolation transformer or simple coil coupling to the mains. At an output current of 1.5 A, the output voltage is guaranteed to swing within 1 V or less of either rail giving the user improved SNR.

In addition to the output amplifier, a small−signal opamp is provided which can be configured as a unity gain follower buffer or can provide the first stage of a 4−pole low pass filter.

The NCS5651 offers a current limit, programmable with a single resistor, R_{LIM}, together with a current limit flag. The device provides two independent thermal flags with hysteresis: a thermal warning flag to let the user know the internal junction temperature has reached a user programmable thermal warning threshold and a thermal error flag that indicates the internal junction temperature has exceeded 150°C.

The NCS5651 has a power supply voltage range of 6−12 V. It can be shut down, leaving the outputs highly−impedant. The NCS5651 comes in a 20−lead QFN package ($4 \times 4 \times 1$ mm^3) with an exposed thermal pad for enhanced thermal reliability.

Features

- Rail−to−Rail: Drop of Only ±1 V with I_{OUT} = 1.5 A
- V_{BB} Supply Voltage: 6−12 V
- Flexible 4th−Order Filtering
- Current−Limit Set with One Resistor
- Diagnostic Flags Level Shifted to V_{CC} to Simplify Interface with External MCU
  - Thermal Warning Flag with Flexible Threshold Setting
  - Thermal Error flag and Shutdown
  - Overcurrent Flag
- Enable/Shutdown Control
- Extended Junction Temperature Range: −40°C to +125°C
- Small Package: 20−pin $4 \times 4 \times 1$ mm^3 NQFP with Exposed Thermal Pad
- Optimized for Operation in the CENELEC A to D Frequency Band
- This is a Pb−Free Device

Typical Applications

- Power Line Communication Driver in AMM and AMR Metering Systems
- Valve, Actuator, and Motor Driver
- Audio

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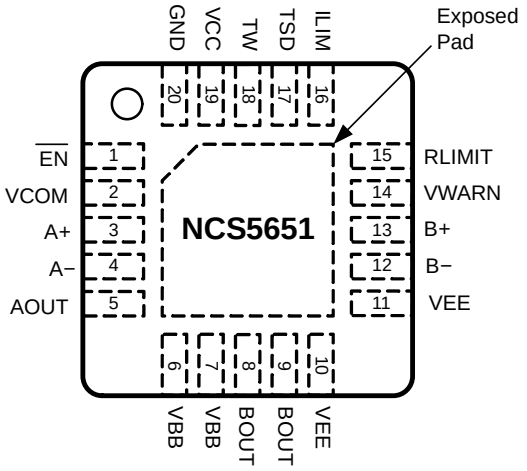


Figure 1. Pin Out NCS5651 in 20−pin NQFP (top view)

Table 1. NCS5651 PINOUT

Signal Name	Type	Pin #	Pin Description
ENB	Input	1	Enable input (active low)
VCOM	Power	2	Virtual Common Voltage = (VCC − VEE)/2 (Note 1)
A+	Input	3	Non inverting input of opamp A
A−	Input	4	Inverting input of opamp A
AOUT	Output	5	Output of opamp A
VBB	Power	6, 7	Positive Power Supply Amplifiers
BOUT	Output	8, 9	Output of opamp B
VEE	Power	10, 11	Negative Power Supply Amplifiers
B−	Input	12	Inverting input of opamp B
B+	Input	13	Non inverting input of opamp B
VWARN	Input	14	Thermal Warning Temp Set
RLIMIT	Input	15	Output B Current Limit Set Resistor
ILIM	Output	16	Current Limit Flag
TSD	Output	17	Thermal Shutdown Flag
TW	Output	18	Thermal Warning Flag
VCC	Power	19	Logic supply
GND	Power	20	Logic ground
EXP	Power	−	Exposed pad. To be connected to VEE potential

1. The principal purpose of pin 2 is to facilitate the implementation of the 4th−order low pass filter when operating on single−sided supply by providing a virtual common at mid−supply. When operating on dual balanced supplies, Pin 2 must be left floating and the external common of the dual supplies should be used for the filter implementation

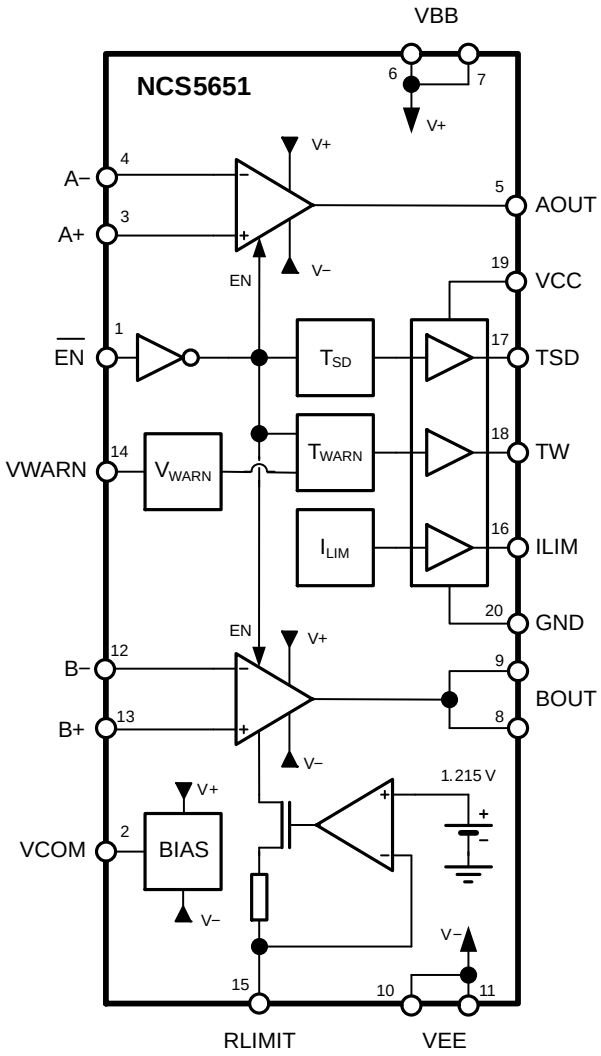


Figure 2. NCS5651 Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
T_J	Junction temperature	−40	+160	°C
T_{STG}	Storage temperature	−65	+165	°C
V_S	Supply voltage (V_{BB} to V_{EE})	−0.3	13.2	V
V_{ICR}	Common Mode Voltage Range input	V_{EE} − 0.3	V_{BB} + 0.3	V
V_{CCM}	Logic Supply Voltage		5.5	V
V_I	Logic Input Voltage	GND − 0.3	V_{CC} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL CHARACTERISTICS $R_{\theta JA}$ obtained with 2S2P test boards according to JEDEC JESD51 standard.

Symbol	Rating	Typical Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Air (Note 3)	38	°C/W

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Temperature	−40	+125	°C
V_S	Supply voltage (V_{BB} to V_{EE})	6	12	V
V_{CC}	Logic Supply voltage)	3.0	5.0	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. Refer to the electrical characteristics and the application information for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS V_{BB} = 12 V; −40°C ≤ T_J ≤ +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OPERATIONAL AMPLIFIER A						
$V_{OS,A}$	Input offset voltage			± 3	± 10	mV
$PSRR_A$	Power supply rejection ratio			25	150	μV/V
$I_{B,A}$	Input bias current (Note 3)				1	nA
$e_{n,A}$	Input voltage noise density	f = 1 kHz; V_{IN} = GND; BW = 131 kHz		250		nV/√Hz
$V_{CM,A}$	Common Mode voltage range		V_{EE} − 0.1		V_{BB} − 3	V
$CMRR_A$	Common Mode Rejection Ration	V_{EE} − 0.1 ≤ V_{CM} ≤ V_{CC} − 3	70	85		dB
$Z_{IDM,A}$	Differential Input Impedance			0.2 | 1.5		GΩ | pF
$Z_{ICM,A}$	Common Mode Input Impedance			0.2 | 3		GΩ | pF
$A_{OL,A}$	Open Loop Gain (Note 3)	R_L = 500 Ω	80	100		dB
GBW_A	Gain Bandwidth Product			80		MHz
$FPBW_A$	Full Power Bandwidth (Note 3)	CLG = +5; V_{OUT} = 11 V_{PP}		1.5		MHz
SR_A	Slew Rate			60		V/μs
$THD+N_A$	Total Harmonic Distortion + Noise	CLG = +1; R_L = 500 Ω; V_O = 8 V_{PP}; f = 1 kHz; C_{in} = 220 μF; C_{out} = 330 μF		0.015		%
		CLG = +1; R_L = 50 Ω; V_O = 8 V_{PP}; f = 1 kHz; C_{in} = 220 μF; C_{out} = 330 μF		0.023		%
$V_{OH,A}$	Output swing from Positive Rail	R_L = 500 Ω to mid−supply		0.3	1	V
$V_{OL,A}$	Output swing from Negative Rail			0.3	1	V
$I_{SC,A}$	Short−Circuit Current			280		mA
$Z_{O,A}$	Output Impedance	CLG = 4; f = 100 kHz		0.25		Ω
$C_{LOAD,A}$	Capacitive Load Drive			100		pF
OPERATIONAL AMPLIFIER B						
$V_{OS,B}$	Input offset voltage			± 3	± 10	mV
$PSRR_B$	Offset versus power supply			25	150	μV/V
$I_{B,B}$	Input bias current (Note 3)				1	nA
$e_{n,B}$	Input voltage noise density	f = 1 kHz; V_{IN} = GND; BW = 131 kHz		125		nV/√Hz
$V_{CM,B}$	Common Mode voltage range		V_{EE} − 0.1		V_{BB} − 3	V
$CMRR_B$	Common Mode Rejection Ratio	V_{EE} − 0.1 ≤ V_{CM} ≤V_{BB} − 3	70	85		dB
$Zi_{DIF,B}$	Differential Input Impedance			0.2 | 11		GΩ | pF
$Zi_{CM,B}$	Common Mode Input Impedance			0.2 | 22		GΩ | pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by characterization or design
4. CLG = Closed Loop Gain
5. The V_{COM} voltage is generated by an internal resistive divider. The pin should not be loaded.
6. Characterization data only. Not tested in production.

Table 5. ELECTRICAL CHARACTERISTICS V_{BB} = 12 V; −40°C ≤ T_J ≤ +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OPERATIONAL AMPLIFIER B						
$A_{OL,B}$	Open Loop Gain (Note 3)	R_L = 5 Ω	80	100		dB
GBW_B	Gain Bandwidth Product			60		MHz
$FPBW_B$	Full Power Bandwidth (Note 3)	CLG = +5; V_{OUT} = 11 V_{PP}	200	400		kHz
SR_B	Slew Rate			70		V/μs
$THD+N_B$	Total Harmonic Distortion + Noise	CLG = +1; R_L = 50 Ω; V_O = 8 V_{PP}; f = 1 kHz		0.015		%
		CLG = +1; R_L = 50 Ω; V_O = 8 V_{PP}; f = 100 kHz		0.023		%
$V_{OH,B}$	Output swing from Positive Rail	I_{OUT} = −1.5 A @ T_J = 25°C		0.7	1	V
		I_{OUT} = −1.0 A @ T_J = 125°C		0.7	1	
$V_{OL,B}$	Output swing from Negative Rail	I_{OUT} = +1.5 A @ T_J = 25°C		0.4	1	V
		I_{OUT} = +1.0 A @ T_J = 125°C		0.4	1	
$I_{SC,B}$	Short−Circuit Current			280		mA
$Z_{O,B}$	Output Impedance	CLG = 1; f = 100 kHz; ENB = 0		0.065		Ω
$Z_{O,B}$	Output Impedance	ENB = 1		12		MΩ
$C_{LOAD,B}$	Capacitive Load Drive			500		nF
BOTH AMPLIFIERS COMBINED						
$T_{J,SD}$	Junction temperature shutdown threshold	(Note 6)	+150	+160		°C
$T_{J,SD,R}$	Junction temperature shutdown recovery threshold	(Note 6)		+135		°C
T_W	Thermal warning tolerance (Note 4)	T_W is determined by the ratio of 2 resistors		± 10		°C
I_{LIM}	Current Limit Tolerance	I_{LIM} is determined by a single resistor		± 50		mA
I_{QE}	Quiescent Current, enabled	ENB = 0		20	40	mA
I_{QD}	Quiescent Current, disabled	ENB = 1		120	150	μA
V_{COM}	Common mode reference output voltage	(Note 5)	5.8	6.0	6.2	V
	Common mode reference output impedance	(Notes 5 and 6)		110		kΩ
LOGIC						
V_{IH}	ENB input level high		GND + 2			V
V_{IL}	ENB input level low				0.8	V
I_{IH}	ENB input current	V_{ENB} = 3.3 V		10		μA
I_{IL}		V_{ENB} = 0 V		0.1		μA
V_{OH}	Flag Output High level				GND + 2	V
V_{OL}	Flag Output Low level		GND + 0.8			V
t_{sd}	Output Shutdown time	ENB 0 → 1		60		ns
t_{en}	Output Enable time	ENB 1 → 0		5	10	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by characterization or design
4. CLG = Closed Loop Gain
5. The V_{COM} voltage is generated by an internal resistive divider. The pin should not be loaded.
6. Characterization data only. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

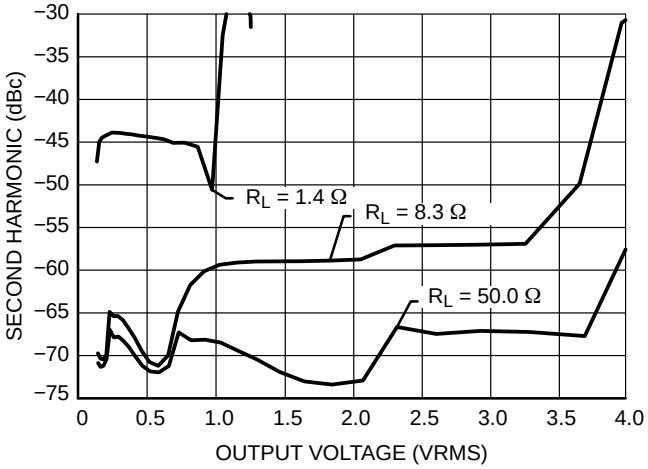


Figure 3. Second Harmonic Distortion of the Output opamp vs. Output Amplitude, for *f* = 100 kHz and R_L (top to bottom) = 1.4 Ω, 8.3 Ω, 50 Ω.

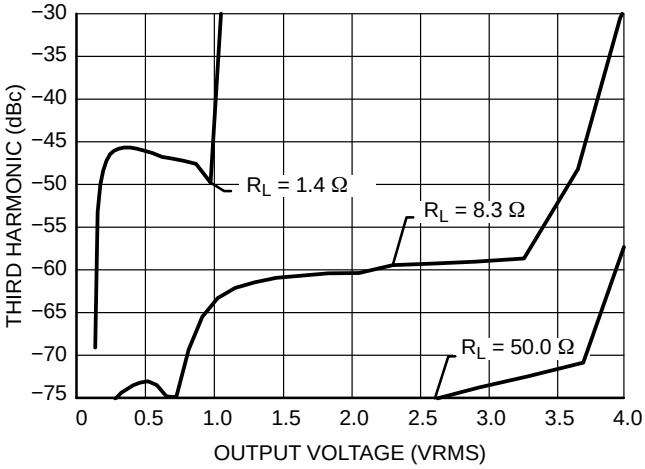


Figure 4. Third Harmonic Distortion of the Output opamp vs. Output Amplitude, for *f* = 100 kHz and R_L (top to bottom) = 1.4 Ω, 8.3 Ω, 50 Ω.

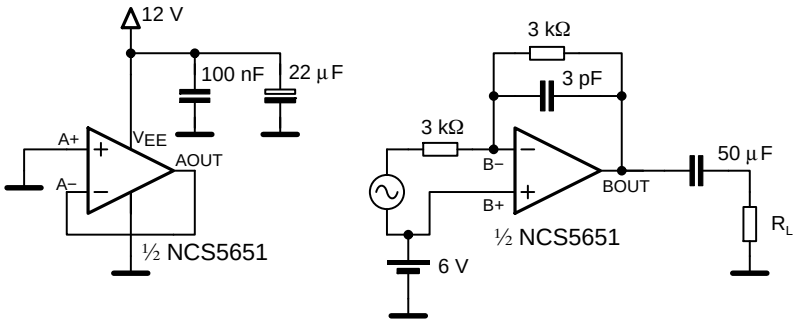


Figure 5. Test Circuit for Figures 3 and 4

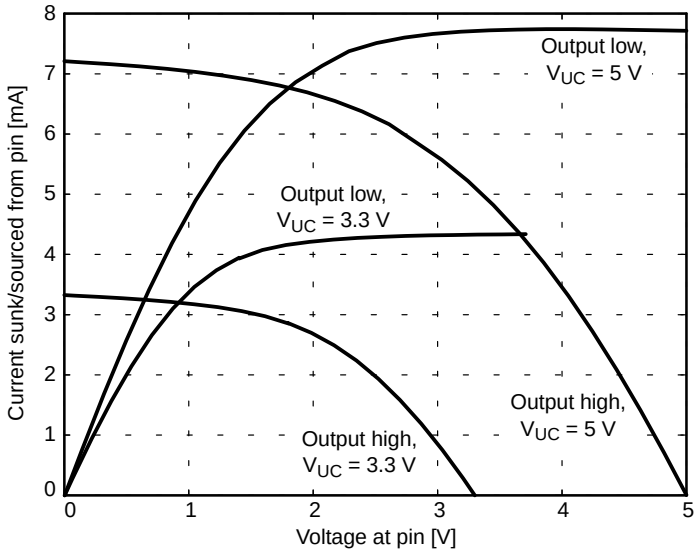


Figure 6. Digital Output Pin (ILIM, TSD, TW) Current Sourcing and Sinking Capability

TYPICAL APPLICATION

A typical power line communication (PLC) application for the NCS5651 is shown in Figure 7. The input amplifier is used in an MFB topology with the power amplifier configured as an inverting amplifier (C4 is required for stability). The circuit formed by D1−D5, L1 and R6 protects the amplifier from high−energy transients from the mains. For more information on power line communication, refer to [3]. For more information on circuit design with the NCS5651, refer to the NCN49597/9 user manual [1].

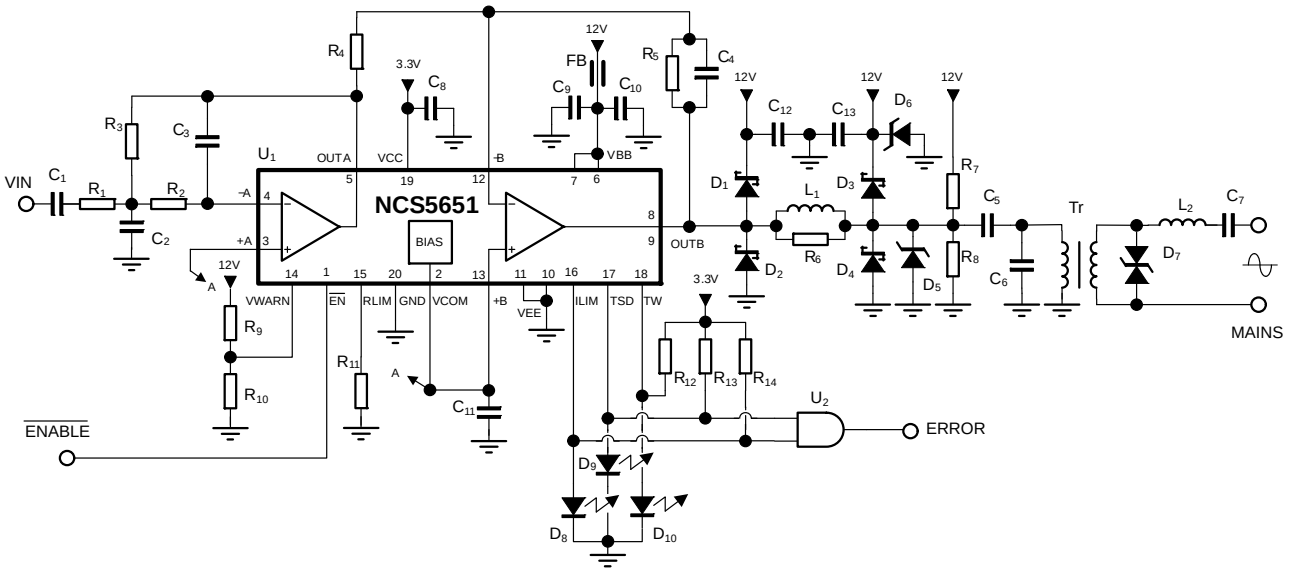


Figure 7. Typical Application Schematic for PLC modem

Table 6. BILL OF MATERIALS

Reference Designator	Value (typical)	Note	Manufacturer	Part Number
U_1		Power operational amplifier	ON Semiconductor	NCS5651
U_2		AND gate	ON Semiconductor	MC74VHC1G32
D_1, D_2		Schottky diode	ON Semiconductor	MBRA140
D_3, D_4		Schottky diode	ON Semiconductor	MBRA340
D_5		Zener Transient Voltage suppressor	ON Semiconductor	1SMA11ATG3
D_6		Zener Transient Voltage suppressor	ON Semiconductor	1SMA12ATG3
D_7		Zener Transient Voltage suppressor	ON Semiconductor	P6SMB11CAT3G
D_8, D_9, D_{10}		Low power indication LED		
R_x	TBD			
C_x	TBD			
L_1	3,3 μH	Saturation current ≥ 2 A		
L_2	10−27 μH	Depending on transformer and communication carrier frequency		
FB	600 Ω @ 10 MHz	Ferrite bead, ≥ 1.5 A current rating		
Tr		Coupling transformer		

APPLICATION INFORMATION

Exposed Thermal Pad

The NCS5651 is capable of delivering 1.5 A into a complex load. Output signal swing should be kept as high as possible. This will minimize internal heat generation, reducing the internal junction temperature. The NCS5651 can swing to within 1 V of either rail without adding distortion.

An exposed thermal pad is provided on the bottom of the device to facilitate heat dissipation. The printed circuit board and soldering process must be carefully designed to minimize the thermal resistance between the exposed pad and the ambient. Refer to [1,2] for more information.

Multi−Feedback Filter (MFB)

CENELEC EN 50065−1 is a European standard for signaling on low−voltage electrical installations in the frequency range 3 kHz to 148. 5 kHz. More specifically Part 1 of that specification deals with frequency bands and electromagnetic disturbances introduced into the electrical mains. A practical solution to meet this requirement is to place a 4th−order filter between the output of the modem and the isolation transformer connected to the mains. In this datasheet a MFB filter topology is proposed to help meet the requirements of the CENELEC standard. Four pole filters require two op amps for implementation. The NCS5651 has an input pre−amplifier and an output power amplifier. Therefore only passive components (R's and C's) need to be added. In addition the NCS5651 has a mid−supply virtual common at pin 2 (V_{com}) to facilitate implementation of the filter topology.

Figure 8 shows the frequency response for each stage and the overall filter.

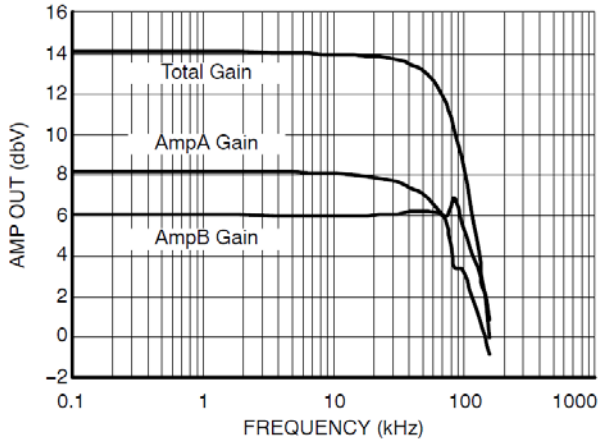


Figure 8. Frequency Response of an EN 50065−1 Compliant Filter

Decoupling

Optimal stability and noise rejection will be implemented with power supply bypassing placed as physically close to the device as possible. A parallel combination of 10 μF and 10 nF is recommended for each sensitive point. For either single−supply operation or split supply operation, bypass should be placed directly across V_{BB} to V_{EE}. In addition add bypass from V_{CC} to GND (Figure 9).

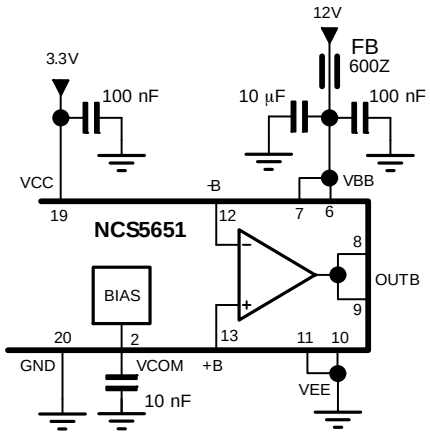


Figure 9. Decoupling Capacitors

Current Limit (R−Limit)

The maximal output current of the NCS5651 can be programmed by the simple addition of a resistor (R_{LIM}) from pin 15 to V_{EE} (Figure 7). Figure 8 shows the limiting value for given resistance, with a tolerance of ±50 mA. Unlike traditional power amplifiers, the NCS5651 current limit functions both when sourcing and sinking current. To calculate the resistance required to program a desired current limit the following equation can be used:

$$I_{LIM} = \frac{1.215}{R_{LIM}} \times 8197$$

If the load current reaches the set current limit, the ILIM flag will go logic high. As an example, the user may act on this by reducing the signal amplitude. When the current output recovers, the ILIM flag returns low.

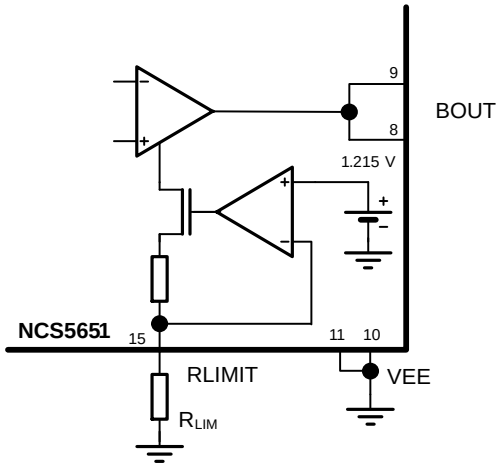


Figure 10. Programming the Current Limit

Figure 11 illustrates the required resistance to program the current limit.

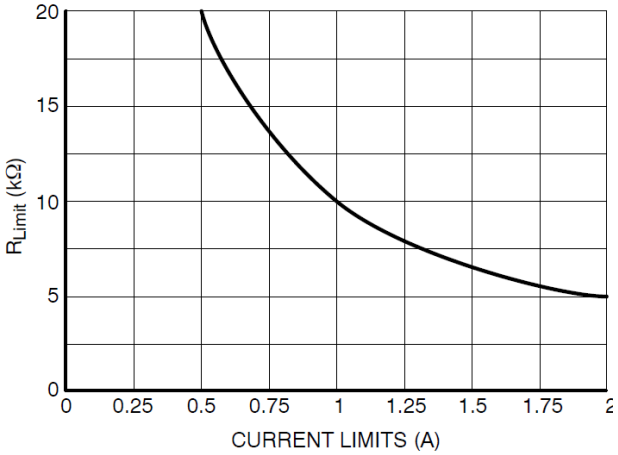


Figure 11. R_{LIM} in Function of the I_{LIM}

Thermal Shutdown and Thermal Warning Flag

Excessive dissipation inside the amplifier, for instance during overload conditions, can result in damaging junction temperatures. A thermal shutdown protection monitors the junction temperature to protect against this.

When the internal junction temperature reaches approximately 160°C, the amplifier is disabled and placed in a high−impedance state. The amplifier will be re−enabled − assuming the Enable input is still active − when the junction temperature cools back down to approximately 135°C.

During thermal shutdown the TSD flag (thermal shut down, pin 17) will go logic high.

The user has the option to avoid entering into the TSD mode by monitoring the junction temperature via the Thermal Warning feature.

Any junction temperature (T_{WARN}) from 105°C to 145°C can be programmed by applying the appropriate voltage to pin 14. Figure 11 shows how this may be realized with a voltage divider between VBB (pins 6,7) and VEE (the negative supply, pin 10 or 11). The voltage ratio required to program the thermal warning of the NCS5651 can be calculated using:

$$V_{TW} = 6.665 \times 10^{-3}\left(T_J\right) + 1.72 \qquad \text{(eq. 1)}$$

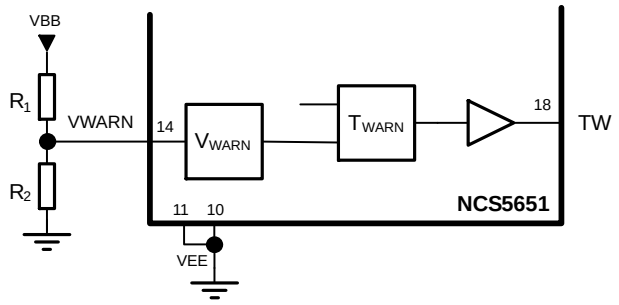


Figure 12. Setting the Thermal Warning Limit by Applying the Corresponding Threshold Voltage to Pin 14 (VWARN)

Figure 13 illustrates the linearity of the internal junction temperature to the required voltage on pin 14 (T_{warn}).

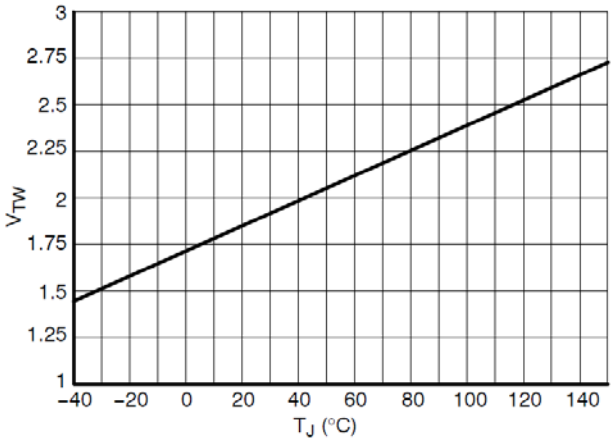


Figure 13. Thermal Warning Threshold in Function of Junction Temperature

Virtual Common (V_{COM})

The principal purpose of V_{COM} is to provide a convenient virtual common for implementing the 4th−order CENELEC filter when operating on single−sided power supply. When operating on balanced split supplies it is recommended to use the power supply common for the filter implementation and to leave V_{COM} floating.

The output impedance of V_{COM} is high, about 110 kΩ; thus, it is strongly recommended to use V_{COM} only for biasing the non−inverting inputs. In addition, it must be buffered with a ceramic capacitor for optimal supply noise rejection.

Safe Operating Area

The safe operating area (SOA) of an amplifier is the collection of output currents I_L and the output voltages V_L that will result in normal operation with risk of destruction due to overcurrent or overheating.

In a normal application only the output amplifier of the line driver must be considered; the load on the small−signal amplifier is usually negligible.

The output amplifier SOA depends on the thermal resistance from junction to ambient $R_{\theta JA}$, which in turn strongly depends on board design. $R_{\theta JA}$ = 50 K/W in free air is a typical value, which may be used even if the host printed circuit board (PCB) is mounted in a small closed box, provided the transmission of frames are infrequent and widely spread in time.

This typical value is also used in the generation of the curves plotted in Figures 14 and 15.

Figure 14 shows the SOA in function of output current I_L and output voltage V_L with the ambient temperature as independent parameter. The maximum allowed current is 800 mA RMS. For that reason it is recommended to limit the output current by using R_{LIM} = 5 kΩ. This current limitation is plotted as a horizontal line. The maximal output voltage is limited by $V_{CC,max}$, V_{OH} and V_{OL}. This results in the straight line on the right hand side of the V_L–I_L plot. The area below and left from these limitations is considered as safe. The relation between output voltage and current is the impedance as seen at the output of the power operational amplifier. Constant impedance lines are represented by canted lines.

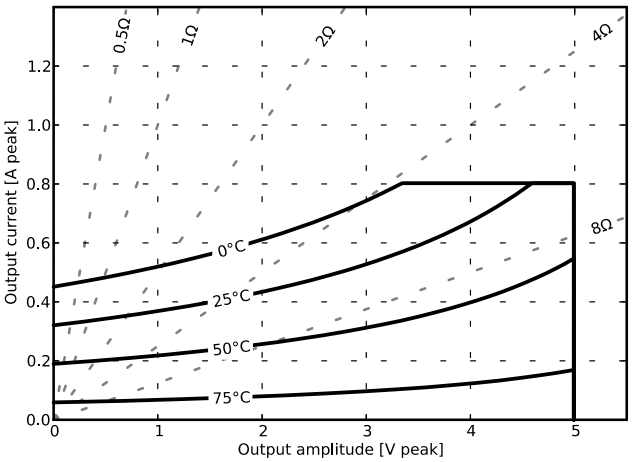


Figure 14. Example SOA in VL–IL Space (bottom left corner is safe) with Rthj−a = 50 K/W

Although voltage−versus−current is the normal representation of safe operating area, a PLC line driver can only control one of these variables: voltage and current are linked through the mains impedance. Figure 15 displays exactly the same information as Figure 14 but might be easier to work with. Constant current values are now represented as canted lines.

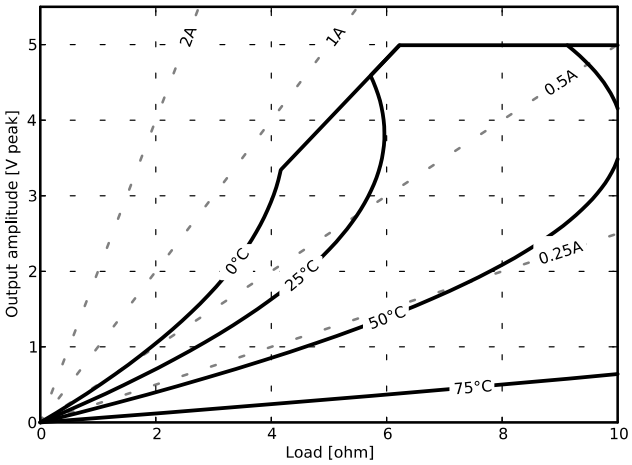


Figure 15. Example SOA in ZL–VL Space (bottom right corner is safe)

Again, the safe operating area depends on PCB layout. Thus, the designer must verify the performance of her particular design [1].

Digital Power Supply GND−Reference and Translators

In many mixed signal applications analog GND and digital GND are not at the same potential. To minimize GND loop issues, the NCS5651 has a separate GND pin (pin 20) which should be used to reference the digital supply and the warning flags (pins 16, 17, and 18). In most applications this would be the same GND reference used for the PLC modem. Please note that at some point in the application digital GND and analog GND must be tied together.

REFERENCES

In this document references are made to:

1. ON Semiconductor, Design Manual NCN49597/9, December 2014. The latest version is available from your sales representative.
2. ON Semiconductor. AND8402/D Thermal Considerations for the NCS5651 (application note). 2014−08−01. Online at http://www.onsemi.com/pub/Collateral/AND8402−D.PDF
3. ON Semiconductor. AND9165/D. Getting started with power line communication (application note). 2014−11−01. Online at http://www.onsemi.com/pub_link/Collateral/AND9165−D.PDF

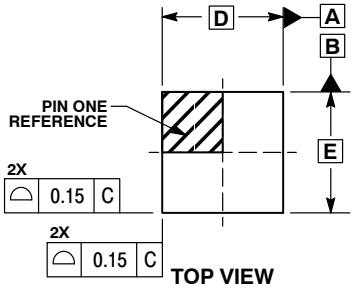
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

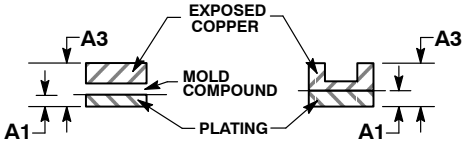
QFN20, 4x4, 0.5P
CASE 485E
ISSUE C

DATE 13 FEB 2018

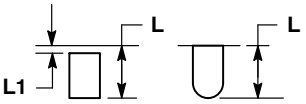


SCALE 2:1

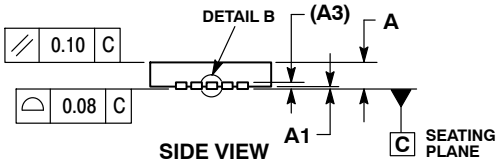




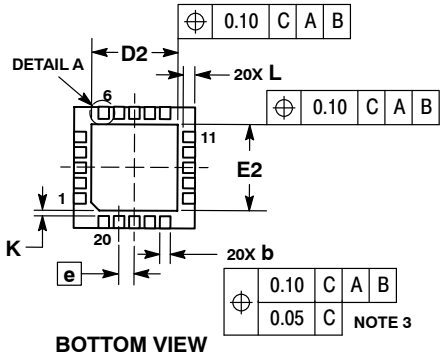
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS

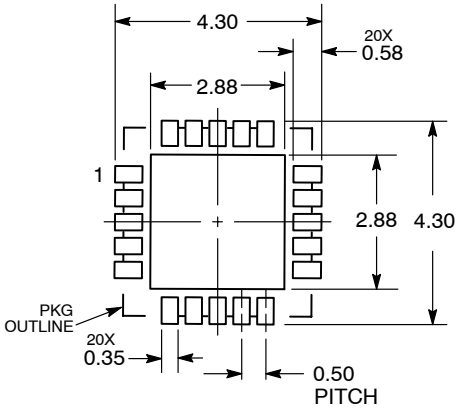


SIDE VIEW



BOTTOM VIEW

SOLDERING FOOTPRINT*



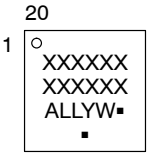
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15

GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
LL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN20, 4X4, 0.5P**	**PAGE 1 OF 1**

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