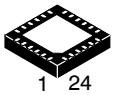
Single 6 A High-Speed, Low-Side SiC MOSFET Driver

NCV51705



QFN24
WETTABLE FLANK
CASE 484AE

MARKING DIAGRAM



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

The NCV51705 driver is designed to primarily drive SiC MOSFET transistors. To achieve the lowest possible conduction losses, the driver is capable to deliver the maximum allowable gate voltage to the SiC MOSFET device. By providing high peak current during turn−on and turn−off, switching losses are also minimized. For improved reliability, dV/dt immunity and even faster turn−off, the NCV51705 can utilize its on−board charge pump to generate a user selectable negative voltage rail.

For full compatibility and to minimize the complexity of the bias solution in isolated gate drive applications the NCV51705 also provides an externally accessible 5 V rail to power the secondary side of digital or high speed opto isolators.

The NCV51705 offers important protection functions such as under−voltage lockout monitoring for the bias power.

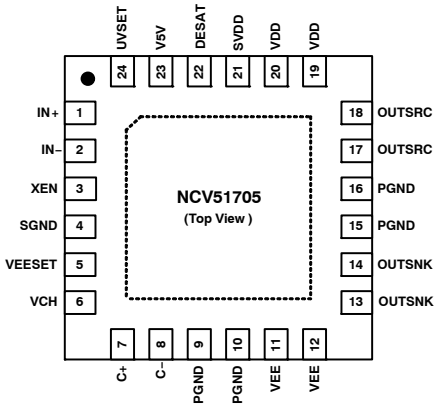
Features

- Automotive Qualified to AEC−Q100 with Grade 1 Temperature Range
- High Peak Output Current with Split Output Stages to Allow Independent Turn−ON/Turn−OFF Adjustment;
  - Source Capability: 6 A
  - Sink Capability: 6 A
- Extended Positive Voltage Rating for Efficient SiC MOSFET Operation during the Conduction Period
- Adjustable, On−board Regulated Charge Pump
- Negative Voltage Drive for Fast Turn−off
- Built−in Negative Charge Pump
- Accessible 5 V Reference / Bias Rail for Digital Oscillator Supply
- Adjustable Under−Voltage Lockout
- Desaturation Function
- Small & Low Parasitic Inductance QFN24 Package with Wettable Flank

Typical Applications

- Driving SiC MOSFET for Automotive Applications
- Automotive Inverters, Converter, and Motor Drivers
- PFC, AC to DC and DC to DC Converters

PIN CONNECTIONS

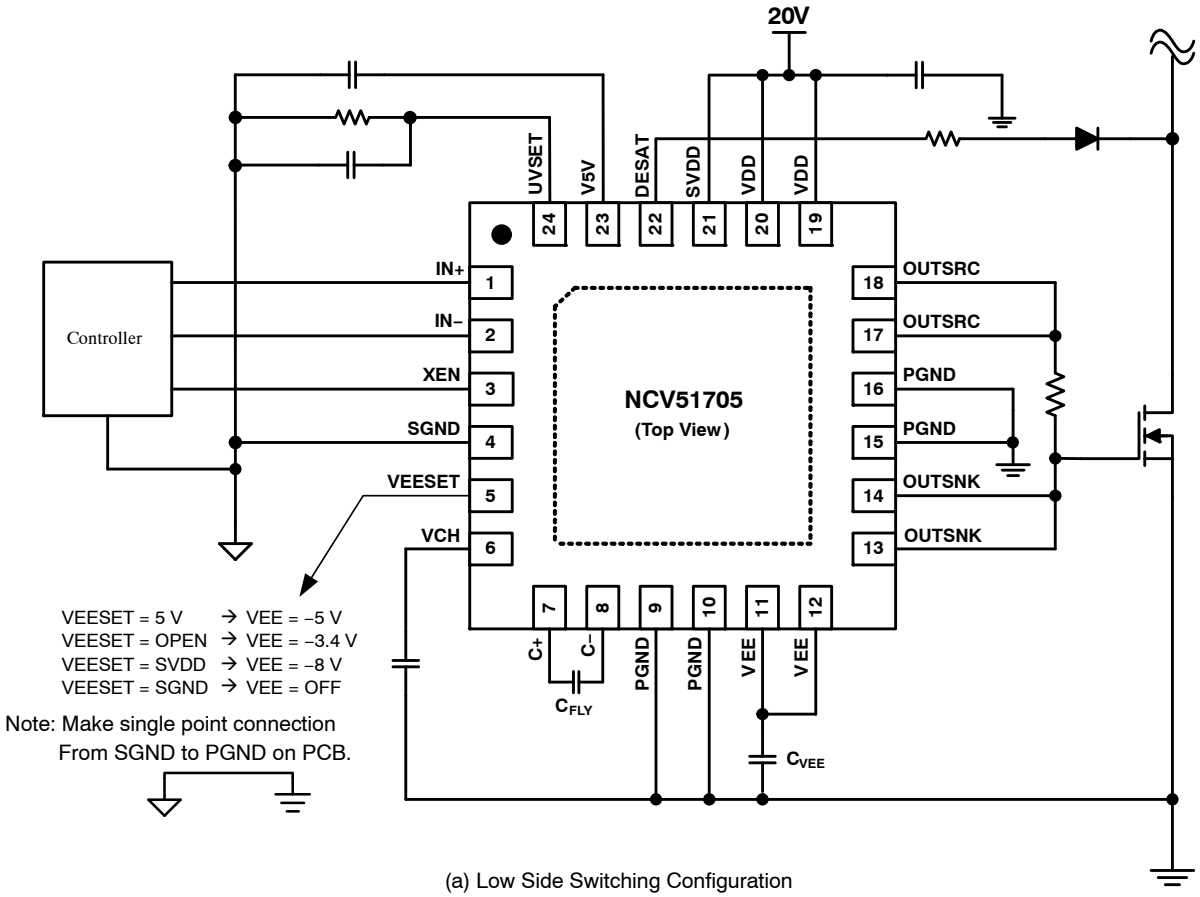


ORDERING INFORMATION

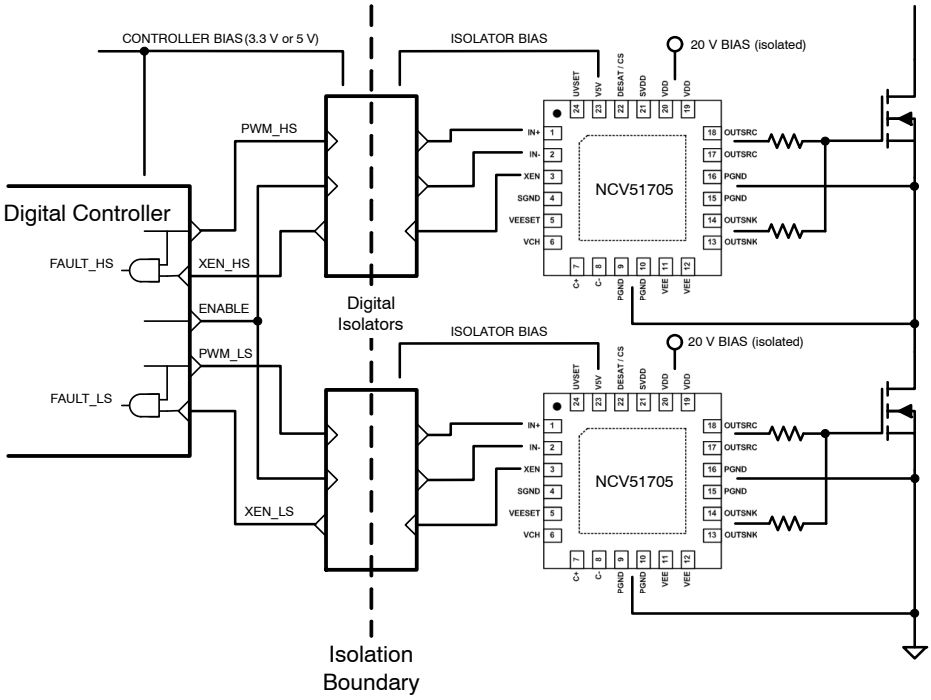
Device	Package	Shipping†
NCV51705MNTWG	QFN24 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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(a) Low Side Switching Configuration



(b) Half Bridge Switching Configuration

Figure 1. Typical Application Schematics

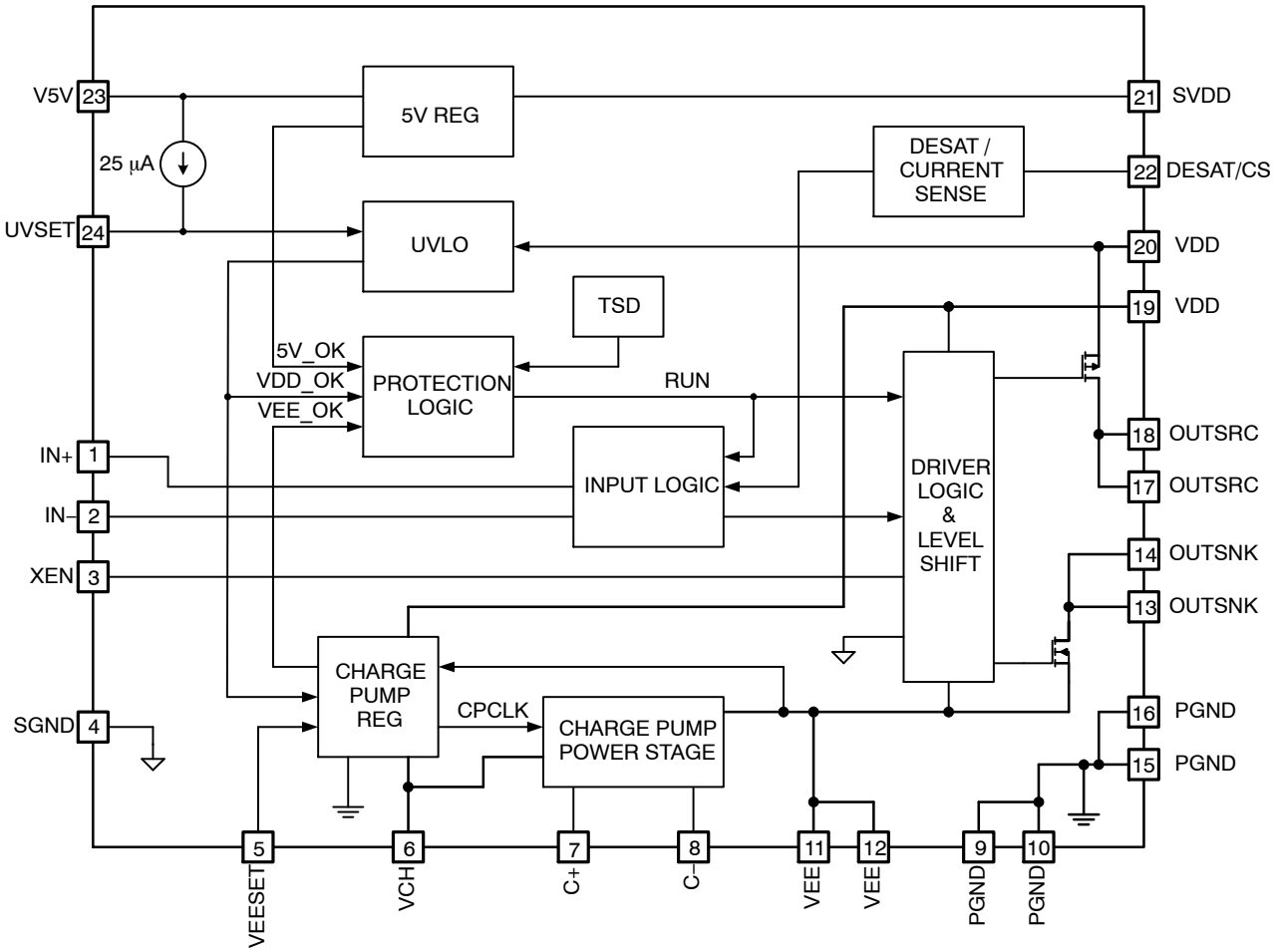


Figure 2. Internal Block Diagram

PIN CONNECTIONS

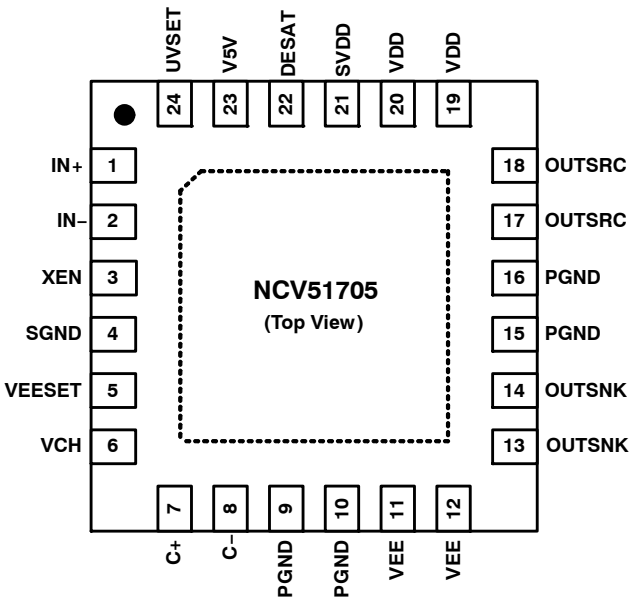


Figure 3. Pin Assignments – 24 Leads QFN (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Name	Description
1	IN+	Input for non−inverting, logic level PWM signal or ENABLE signal.
2	IN−	Input for inverting, logic level PWM signal or DISABLE signal.
3	XEN	Driver state flag. See the application description for details.
4	SGND	Signal ground.
5	VEESET	Negative bias voltage select pin.
6	VCH	Regulated bias voltage for the charge pump.
7	C+	Positive node of the flying charge pump capacitor.
8	C−	Negative node of the flying charge pump capacitor.
9,10,15,16	PGND	Power ground.
11,12	VEE	Negative drive voltage, the output of the charge pump
13,14	OUTSNK	Pull down drive.
17,18	OUTSRC	Pull up drive.
19,20	VDD	Positive bias voltage for the high current driver section.
21	SVDD	Positive bias voltage for the control section of the driver.
22	DESAT	Sense input for the desaturation / current limit input of the driver.
23	V5V	External bypass for 5 V controller bias – suitable to power digital isolators
24	UVSET	Input for setting the Under voltage lock out threshold. (minimum operating voltage level)

Table 2. OUTPUT LOGIC

IN+	IN−	OUTSRC
0 (Note 1)	0	0
0 (Note 1)	1 (Note 1)	0
1	0	1
1	1 (Note 1)	0

1. Default input signal if no external connection is made.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Power Supply Voltage	−0.3	28	V
V_{V5V}	Bias Rail	−0.3	5.5	V
V_{CH}	Charge Pump Supply Voltage	−0.3	10	V
V_{EE}	Charge Pump Output; Negative Gate Drive Voltage	−9	+0.3	V
V_{VEESET}	Charge Pump Output Voltage Select	−0.3	28	V
V_{IN+}; V_{IN-}	Logic Input Voltage Levels	−0.3	V5V+0.3	V
V_{XEN}	Logic Output Voltage	−0.3	V5V+0.3	V
V_{UVSET}	UVLO SET Voltage	−0.3	V5V+0.3	V
V_{DESAT}	Desaturation / Current sense voltage	−0.3	12	V
V_{C+}	Positive node of the flying charge pump capacitor	−0.3	VCH+0.3	V
V_{C-}	Negative node of the flying charge pump capacitor	+0.3	V_{EE} -0.3	V
V_{OUTSRC}	Gate Drive Source Output Voltage	V_{EE} -0.3	V_{DD} +0.3	V
V_{OUTSNK}	Gate Drive Sink Output Voltage	V_{EE} -0.3	V_{DD} +0.3	V
f_{MAX}	Maximum Operating Frequency (Note 2)		500	kHz
T_J	Junction Temperature	−55	150	°C
T_{STG}	Storage Temperature	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum operating frequency refers to ground reference applications and might be limited by power dissipation below the recommended value.

Table 4. THERMAL CHARACTERISTICS

Parameters		Symbol	Value	Unit
Thermal Characteristics, QFN 4x4 24 Leads Thermal Resistance Junction−Air (Notes 3 & 4)	1S0P with thermal vias	θ_{JA}	127	°C/W
	1S2P with thermal vias		43	
	1S0P with thermal vias	Ψ_{jt}	12	
	1S2P with thermal vias		3.7	
Power Dissipation (Note 4)	1S0P with thermal vias	P_D	0.98	W
	1S2P with thermal vias		2.9	

3. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
4. JEDEC standard: JESD51−2, JESD51−3. Mounted on 76.2×114.3×1.6mm PCB (FR−4 glass epoxy material).
   1S0P with thermal vias: one signal layer with zero power plane and thermal vias
   1S2P with thermal vias: one signal layer with two power plane and thermal vias.

Table 5. ESD CAPABILITY

Symbol	Parameter	Value	Unit
ESD	Human Body Model, JESD22−A114 (Note 5)	2000	V
	Charged Device Model, JESD22−C101 (Note 5)	1000	

5. Meets JEDEC standards JESD 22−A114 and JESD 22−C101.

Table 6. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive Power Supply Voltage	10	22	V
V_{EE}	Negative Power Supply Voltage	−8	0	V
V_{CH}	Charge Pump Power Supply Voltage	0	8	V
V_{V5V}	5 V internal/external bias output	0	5.5	V
V_{ENA}	Logic Enable Voltage	0	5.5	V
V_{IN}	Logic Input Voltage	0	5.5	V
V_{XEN}	Logic Output Voltage	0	5.5	V
V_{VEESET}	Charge Pump Output Voltage Setting	0	22	V
V_{UVSET}	UVLO Threshold Setting	2	3.5	V
V_{DESAT}	Desaturation Voltage	0	10	V
f_{SW}	Operating Frequency (Note 6)		500	kHz
T_A	Operating Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Maximum operating frequency refers to ground referenced applications and might be limited by power dissipation below the recommended value.

Table 7. ELECTRICAL CHARACTERISTICS (V_{DD} = 20 V, V_{EESET} = 0 V and C_{LOAD} = 1000 pF for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified.) (Note 7)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
VDD SECTION						
I_{DD}	Operating V_{DD} Supply Current	f_{IN} = 100 kHz, V_{EESET} = 5 V		12	18	mA
I_{QDD1}	Quiescent V_{DD} Supply Current 1	V_{IN+} = V_{IN-} = 0 V, V_{EESET} = 5 V		4.5	6.5	mA
I_{QDD2}	Quiescent V_{DD} Supply Current 2	V_{IN+} = 0 V, V_{IN-} = 5 V		0.85	1.1	mA
I_{UVSET}	Source Current for UV Voltage Set	V_{UVSET} = 3 V	20	25	30	μA
V_{DDUV+}	V_{DD} Supply Under−Voltage Positive−going Threshold	V_{UVSET} = 3 V	17	18	19	V
V_{DDUV-}	V_{DD} Supply Under−Voltage Negative−going Threshold	V_{UVSET} = 3 V	16	17	18	V
V_{DDHYS}	V_{DD} Supply UVLO Hysteresis Voltage	V_{DDUV+} − V_{DDUV-}		1		V
$V_{UVSET,MIN}$	UVSET pin short protection Threshold	V_{UVSET} rising		1.55		V
$V_{UVSET,HYS}$	UVSET pin short protection Hysteresis			0.2		V
5V REGULATOR SECTION						
V_{V5V}	External Bypass for 5 V (Note 8)	T_J = 25°C	4.9	5	5.1	V
		Total Variation	4.75	5	5.25	V
V_{V5V_Reg}	5 V Line Regulation	10 V < V_{DD} < 22 V, I_{OUT} = 10 mA			50	mV
	5 V Load Regulation	0 mA < I_{OUT} < 10 mA			50	mV
I_{5V_MAX}	Maximum Output Current (Note 9)	for external load	20	25		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C.
8. Exclude overshoot voltage at start−up.
9. This parameter is not tested in production, although derived by design/characterization.

Table 7. ELECTRICAL CHARACTERISTICS (V_{DD} = 20 V, V_{EESET} = 0 V and C_{LOAD} = 1000 pF for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified.) (Note 7)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units
CHARGE PUMP SECTION						
V_{EE}	Negative Bias Rail Voltage	V_{EESET} = 5 V	−5.7	−5	−4.3	V
		V_{EESET} = open	−4.0	−3.4	−2.8	V
		V_{EESET} = V_{DD}		−8		V
$I_{VEE, MAX}$	Maximum Output Current of V_{EE}	C_{FYL} = 0.47 μF, C_{VEE} = 1.5 μF C_{LOAD} = 1 nF, V_{EESET} = 5 V			40	mA
f_{OSC}	Oscillator Switching Frequency for Charge Pump		320	390	480	kHz
DESATURATION SECTION						
I_{DESAT}	DC Source Current	V_{DESAT} = 0 V	340	400	460	μA
$V_{TH,DESAT}$	V_{CE} Protection Threshold		6.7	7.5	8.1	V
$t_{DEL,DESAT}$	Protection Blanking Time after turn−on		300	500	700	ns
$R_{ON,DESAT}$	Active Pull Down Resistance			5	10	Ω
INPUT LOGIC SECTION; IN+; IN−						
V_{IH}	High Level Input Voltage			1.6	2.0	V
V_{IL}	Low Level Input Voltage		0.8	1.2		V
V_{INHYS}	Input Logic Hysteresis			0.4		V
I_{IN+}	High Level Logic Input Bias Current	V_{IN+} = 5 V		50		μA
$I_{IN−}$	Low Level Logic Input Bias Current	$V_{IN−}$ = 0 V		50		μA
R_{IN+}	Logic Input Pull−Down Resistance		75	100	125	kΩ
$R_{IN−}$	Logic Input Pull−Up Resistance		75	100	125	kΩ
OUTPUT LOGIC SECTION; XEN						
V_{OHX}	High Level Output Voltage (V5V−V_{OH})	I_{OUT} = 1 mA		0	0.5	V
V_{OLX}	Low Level Output Voltage	I_{OUT} = 1 mA		0	0.2	V
I_{XENH}	High Level Logic Output Source Current (Note 9)				5	mA
I_{XENL}	High Level Logic Output Sink Current (Note 9)				5	mA
GATE DRIVER OUTPUT SECTION						
I_{SOURCE}	OUTSRC Source Current (Note 9)	OUTSRC = 0 V, V_{EESET} = 5 V		6		A
I_{SINK}	OUTSNK Sink Current (Note 9)	OUTSNK = 20 V, V_{EESET} = 5 V		6		A
V_{OH}	High Level Output Voltage (V_{DD} − V_{OUT})	I_{OUT} = 100 mA			0.5	V
V_{OL}	Low Level Output Voltage	I_{OUT} = 100 mA			0.2	V
t_{ON}	Turn−On Propagation Delay	C_{LOAD} = 1 nF		25	50	ns
t_{OFF}	Turn−Off Propagation Delay	C_{LOAD} = 1 nF		25	50	ns
t_R	Turn−On Rise Time	C_{LOAD} = 1 nF		8	15	ns
t_F	Turn−Off Fall Time	C_{LOAD} = 1 nF		8	15	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C.
8. Exclude overshoot voltage at start−up.
9. This parameter is not tested in production, although derived by design/characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

Typical characteristics are provided at 25°C and V_{DD} = 20 V unless otherwise noted.

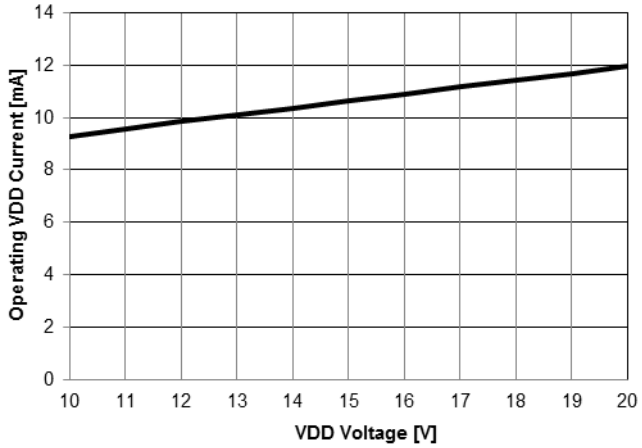


Figure 4. Operating Current (I_{DD}) vs. Operating Voltage (V_{DD})

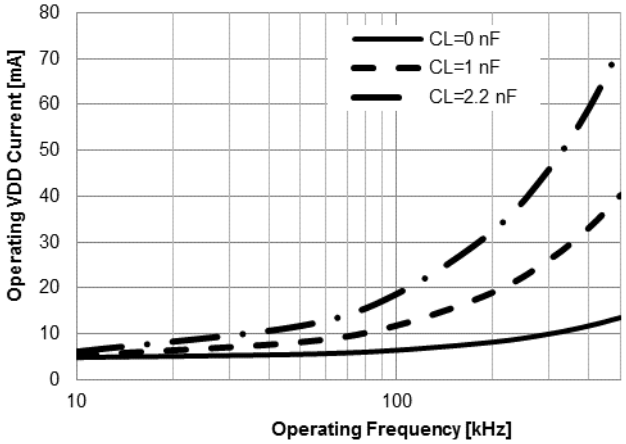


Figure 5. Operating Current (I_{DD}) vs. Operating Frequency

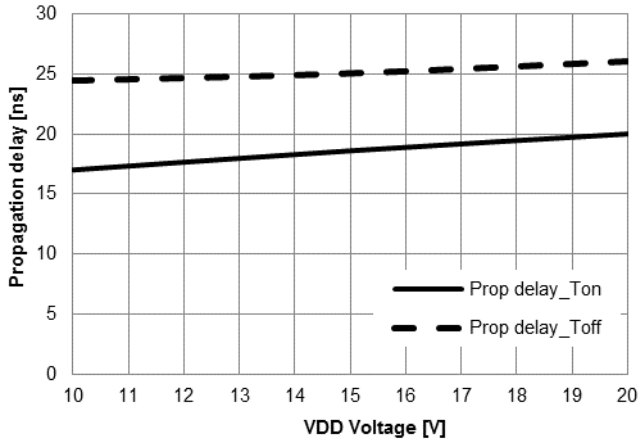


Figure 6. Propagation Delay Time vs. Operating Voltage (V_{DD})

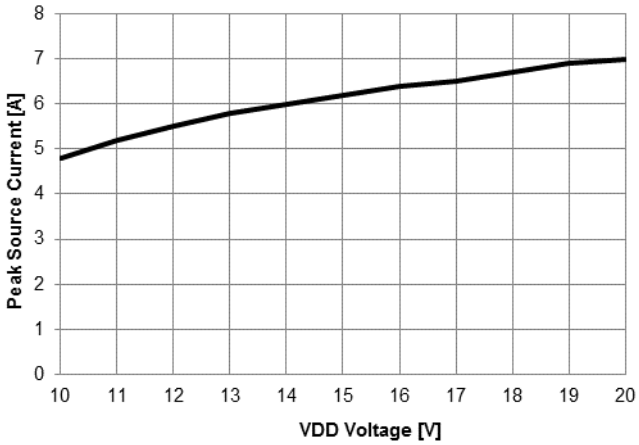


Figure 7. Sourcing Current vs. Operating Voltage (V_{DD})

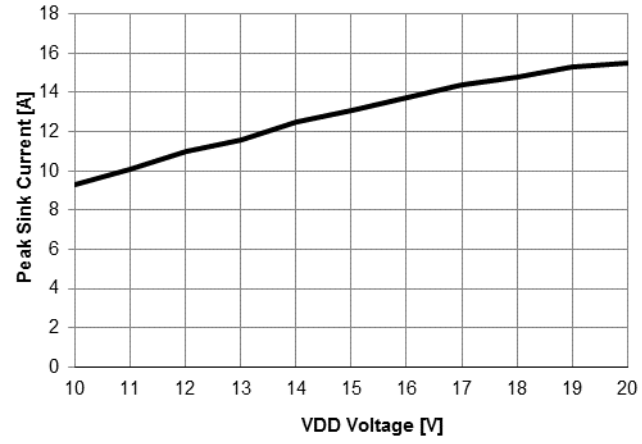


Figure 8. Sinking Current vs. Operating Voltage (V_{DD})

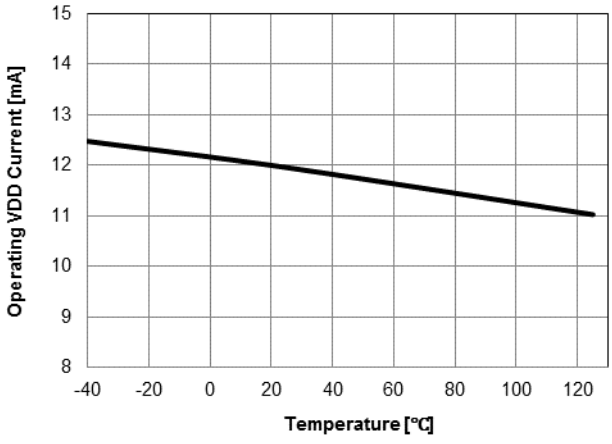


Figure 9. Operating Current (I_{DD}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

Typical characteristics are provided at 25°C and V_{DD} = 20 V unless otherwise noted.

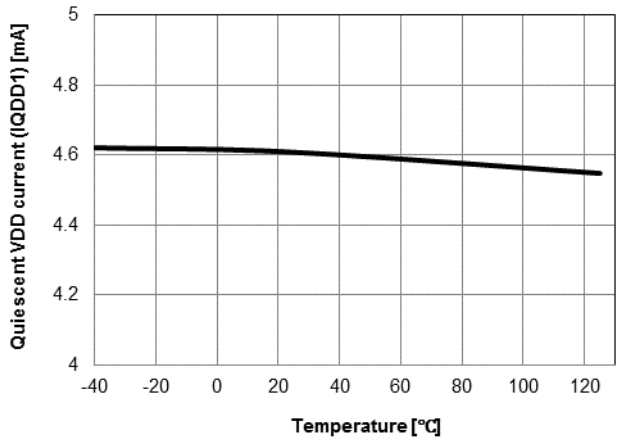


Figure 10. Quiescent Current 1 (I_{QDD1}) vs. Temperature

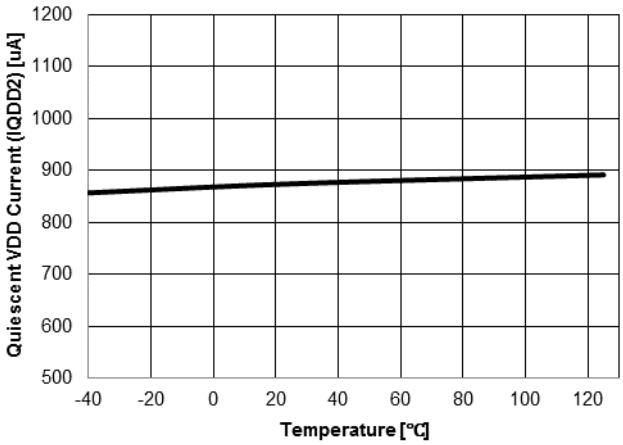


Figure 11. Quiescent Current 2 (I_{QDD2}) vs. Temperature

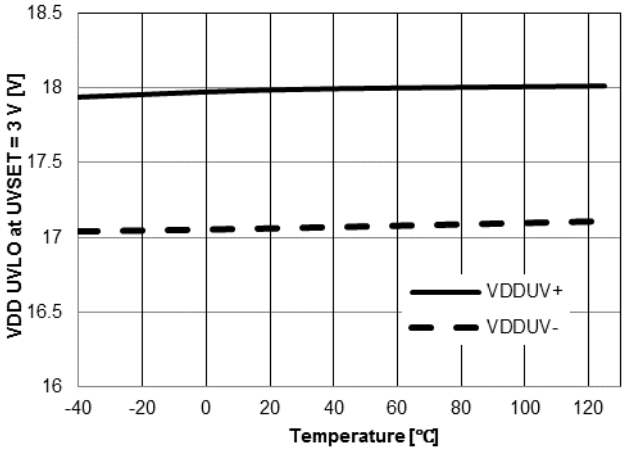


Figure 12. VDD UVLO vs. Temperature

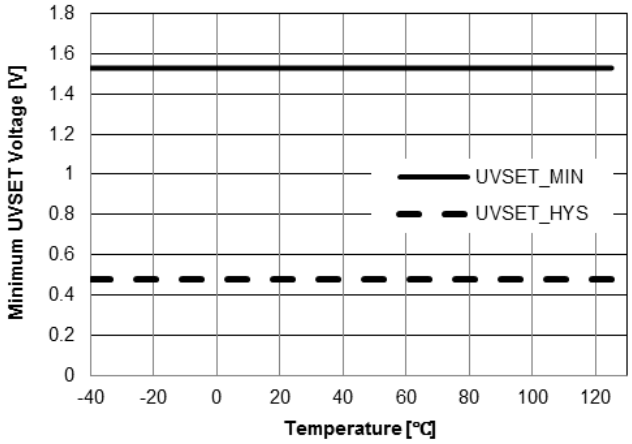


Figure 13. UVSET vs. Temperature

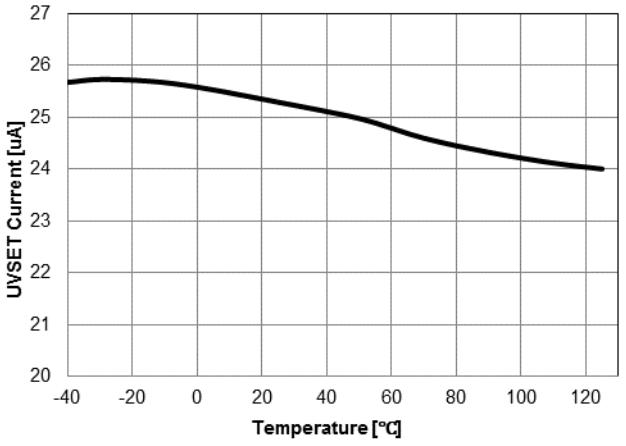


Figure 14. UVSET Current (I_{UVSET}) vs. Temperature

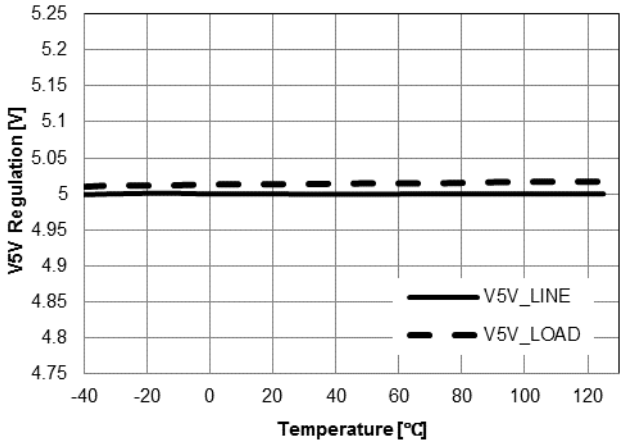


Figure 15. 5 V Regulated Output Voltage (V5V) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

Typical characteristics are provided at 25°C and V_{DD} = 20 V unless otherwise noted.

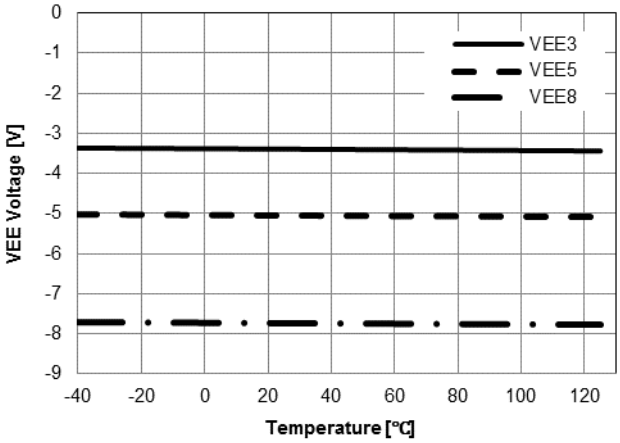


Figure 16. Negative Bias Voltage of Charge Pump vs. Temperature

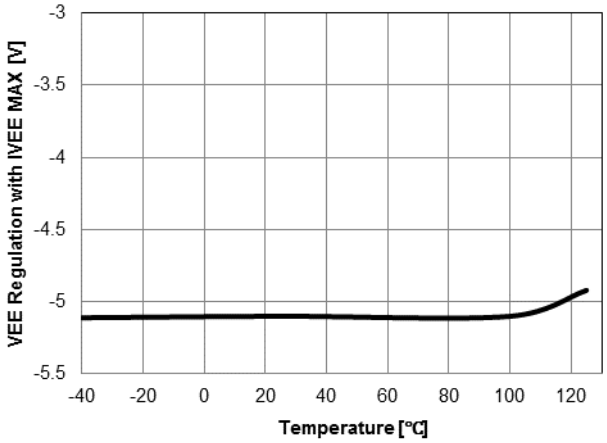


Figure 17. VEE5 Regulated Voltage with $I_{VEE,MAX}$ vs. Temperature

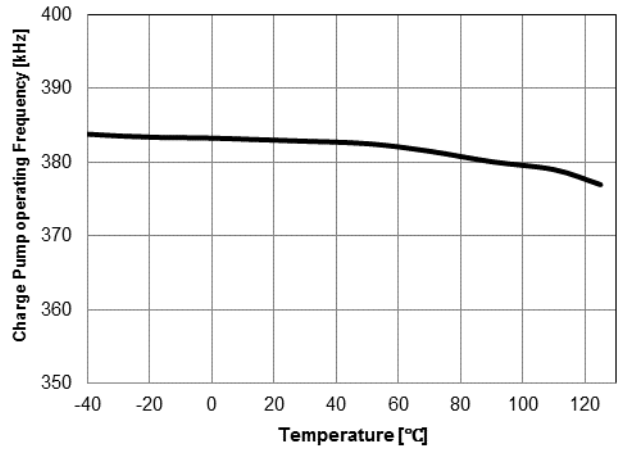


Figure 18. Charge Pump Operating Frequency (f_{OSC}) vs. Temperature

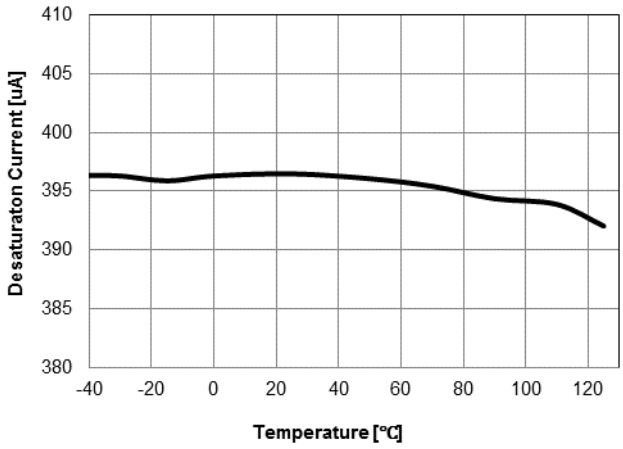


Figure 19. Desaturation Current (I_{DESAT}) vs. Temperature

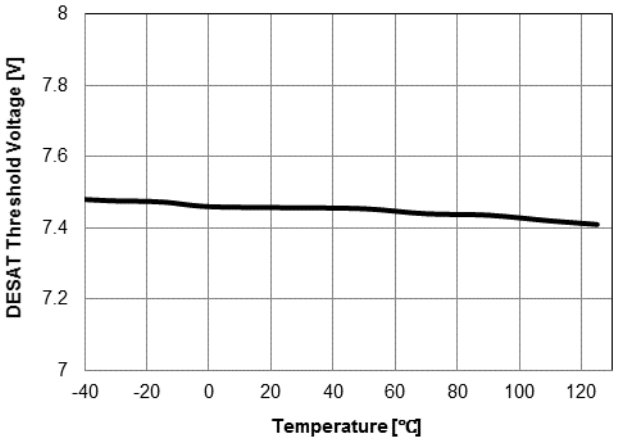


Figure 20. DESAT Threshold Voltage ($V_{TH,DESAT}$) vs. Temperature

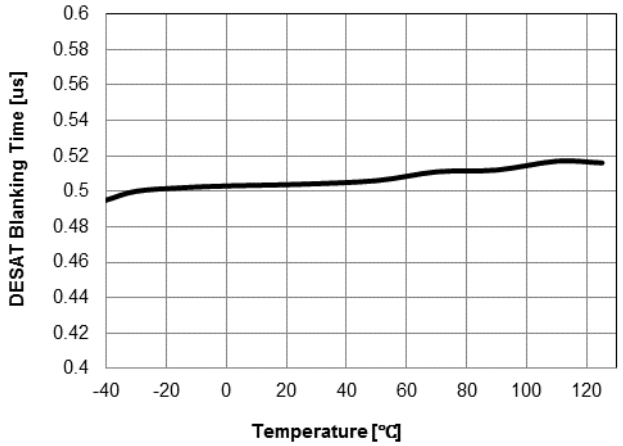


Figure 21. Desaturation Blanking Time ($t_{DEL,DESAT}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

Typical characteristics are provided at 25°C and V_{DD} = 20 V unless otherwise noted.

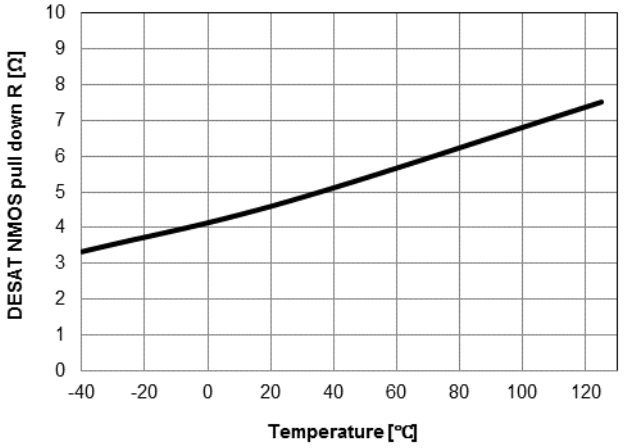


Figure 22. DESAT Pull Down Resistance ($R_{DON,DESAT}$) vs. Temperature

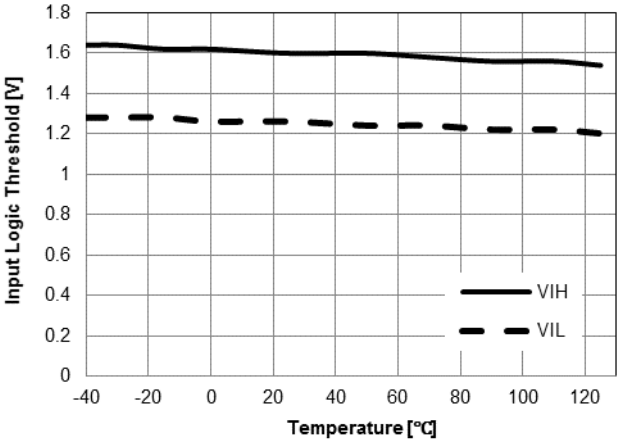


Figure 23. Input Logic Threshold Voltage vs. Temperature

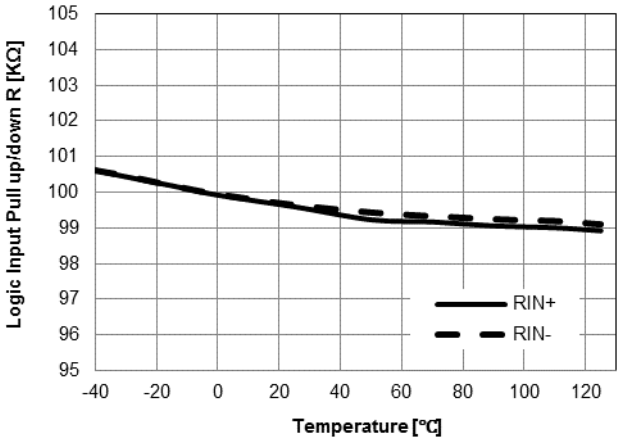


Figure 24. Logic Input Resistance vs. Temperature

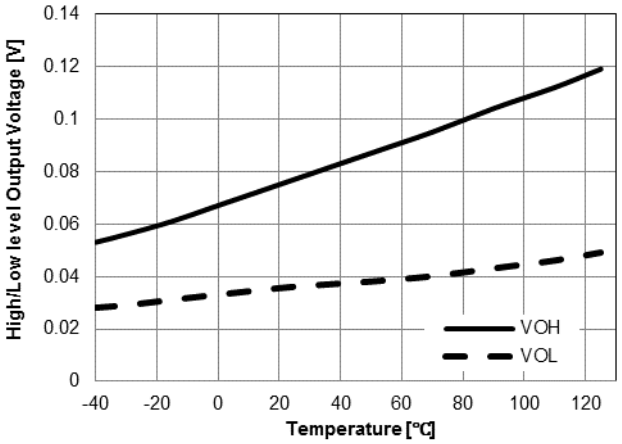


Figure 25. XEN Logic Output Voltage vs. Temperature

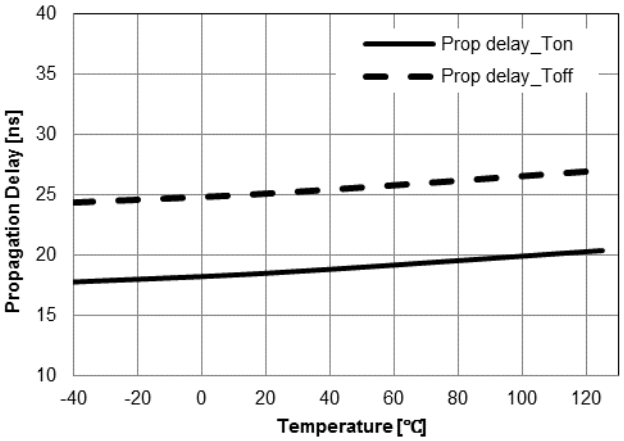


Figure 26. Propagation Delay Time vs. Temperature

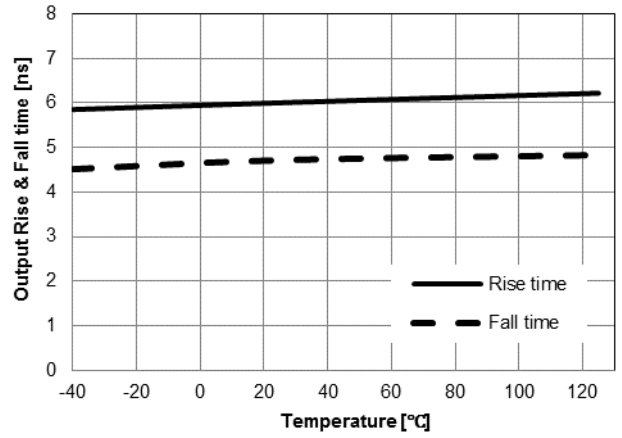


Figure 27. Turn On Rising and Turn Off Falling Time vs. Temperature

APPLICATIONS INFORMATION

The NCV51705 can be quickly configured by following the steps outlined in this section. The component references made throughout this section refer to the schematic diagram and reference designations shown in Figure 28.

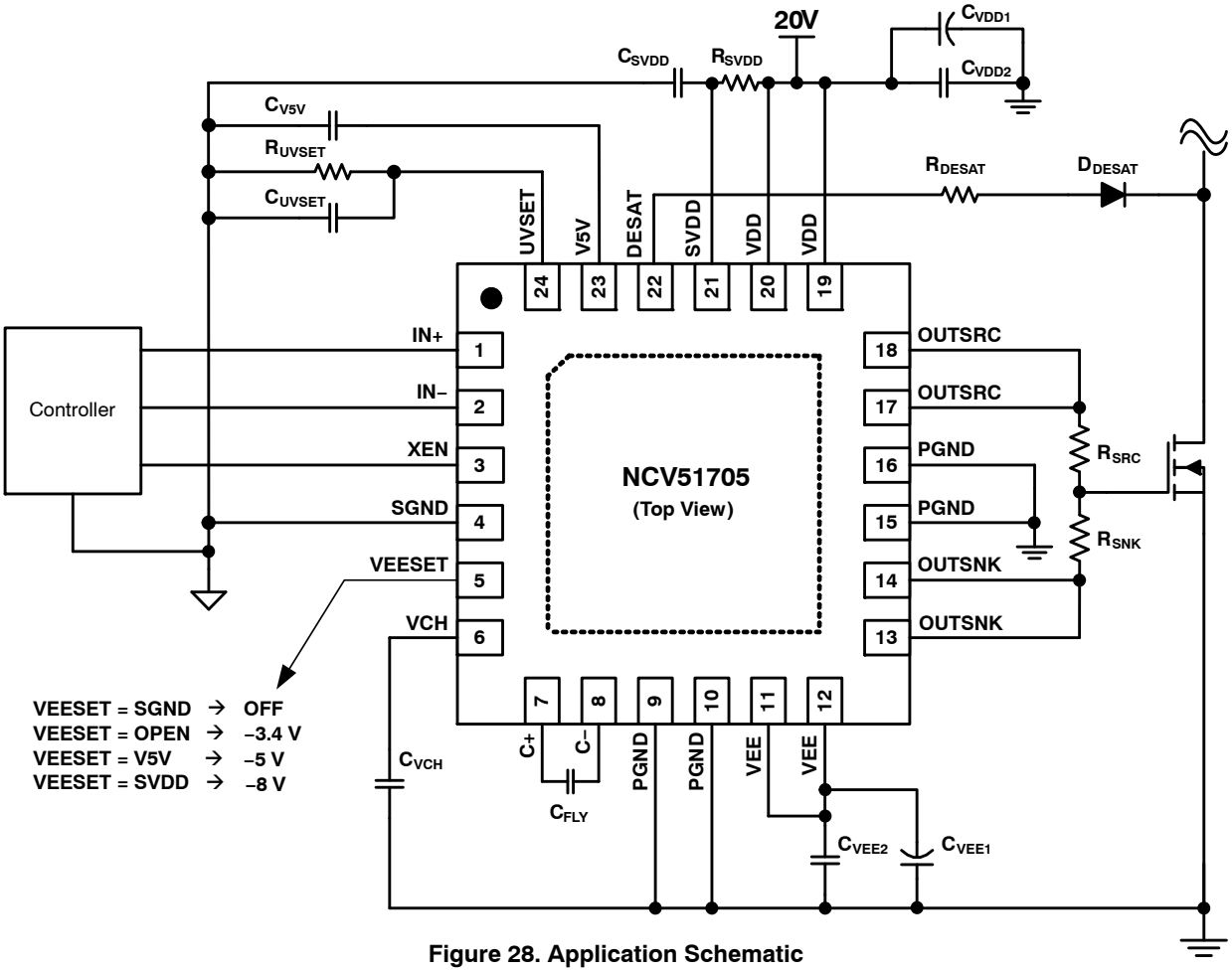


Figure 28. Application Schematic

Input (IN+, IN−)

Both independent PWM inputs are TTL compatible and are internally pulled to the correct states such that each corresponding driver input is defaulted to the inactive (disabled) state. The TTL input thresholds provide buffer and level translation functions from logic inputs. The input thresholds meet industry−standard TTL−logic thresholds, independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic high. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/μs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

For non−inverting input logic the PWM input signal is applied to IN+ while the IN− input can be used as an enable function. If IN− is pulled HIGH, the driver output remains LOW, regardless of the state of IN+. To enable the driver output, IN− should be tied to SGND through a 10 kΩ resistor, as shown in Figure 29, or can be used as an active LOW enable pull down. The start−up logic waveforms shown in Figure 30 illustrate the expected behavior when applying a PWM input signal to the IN+ input while the IN− input is pulled LOW to SGND. In this example, the PWM signal is applied prior to the application of VDD. When VDD is greater than ~7.5 V, the NCV51705 internal charge pump is enabled and begins switching. The output is only enabled when VDD is greater than the set UVLO ON level (VON) and VEE is less than 80% of the programmed voltage level. The output begins switching corresponding to the next PWM rising edge after both UVLO thresholds have been crossed. This method of edge detection, assures the output accurately represents the PWM input while preventing the output from possibly switching in the middle of an IN+, PWM pulse on−time.

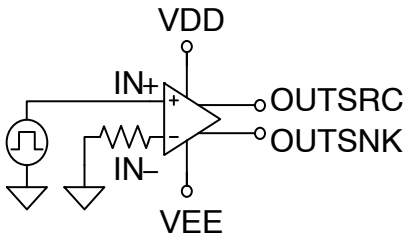


Figure 29. Non−inverting Input Configuration

Table 8. NON−INVERTING LOGIC, IN+, TRUTH TABLE

IN+ (PWM)	IN− (SGND)	OUTSRC	OUTSNK
0	0	0	1
1	0	1	0

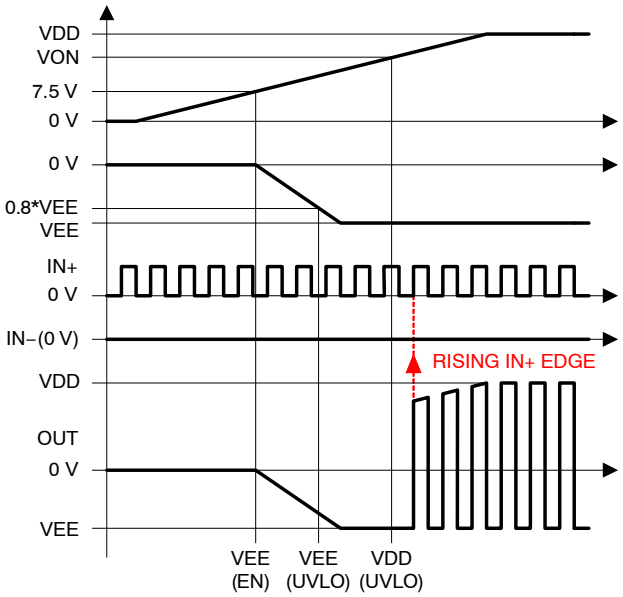


Figure 30. Non−inverting Start−up Logic

For inverting input logic the PWM input signal is applied to IN− while the IN+ input can be used as an enable function. If IN+ is pulled LOW, the driver output remains LOW, regardless of the state of IN−. To enable the driver output, IN+ should be tied to V5V (5 V) through a 10 kΩ resistor, as shown in Figure 31, or can be used as an active HIGH enable pull up. The start−up logic waveforms shown in Figure 32 illustrate the expected behavior when applying a PWM input signal to the IN− input while the IN+ input is pulled HIGH to V5V. In this example, the PWM signal is applied prior to the application of VDD. When VDD is greater than 7.5 V, the NCV51705 internal charge pump is enabled and begins switching. The output is only enabled when VDD is greater than the set UVLO ON level (VON) and VEE is less than 80% of the programmed voltage level. The output begins switching corresponding to the next PWM falling edge after both UVLO thresholds have been crossed. This method of edge detection, assures the output accurately represents the PWM input while preventing the output from possibly switching in the middle of an IN−, PWM pulse off−time.

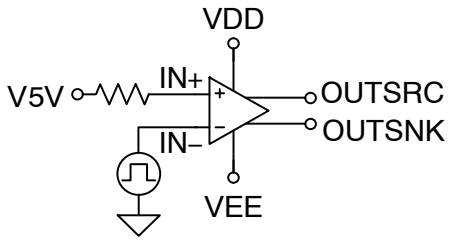


Figure 31. Inverting Input Configuration

Table 9. INVERTING LOGIC, IN−, TRUTH TABLE

IN+ (V5V)	IN− (PWM)	OUTSRC	OUTSNK
1	0	1	0
1	1	0	1

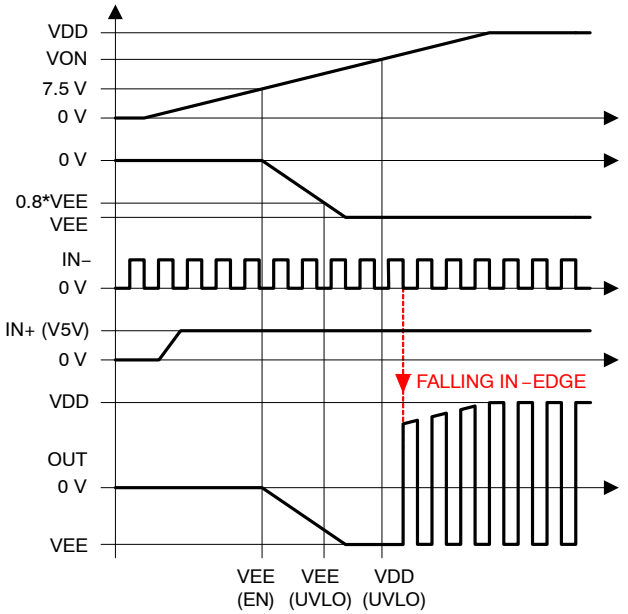


Figure 32. Inverting Start−up Logic

Driver State Reporting (XEN)

The XEN signal is a 5 V digital output representation of the output state of the NCV51705 driver. XEN is directly derived from the output of the driver and should not be considered as the inverse of the non−inverting logic input to the driver, IN+. The output of the NCV51705 driver can be commanded to its OFF state while the input signal is still HIGH by any of the protection functions of the driver. In such instances, XEN will accurately represent that the river is OFF, independent of the input signal to the device.

The propagation delay from IN to XEN is related with T_{ON} and T_{OFF} as shown in Table 10. T_{ON} and T_{OFF} are typical 25 ns with 1 nF load.

Table 10. XEN DELAY

Item	Timing Definition	Typical XEN Delay
ON Delay (IN to XEN)	IN+ rising (V_{IH}) to XEN falling (90%)	= T_{ON}
	IN− falling (V_{IL}) to XEN falling (90%)	= T_{ON}
OFF Delay (IN to XEN)	IN+ falling (V_{IL}) to XEN rising (10%)	= T_{OFF} + 40 ns
	IN− rising (V_{IH}) to XEN rising (10%)	= T_{OFF} + 40 ns

The intent of this signal is that it can be used as a fault flag and in half−bridge power topologies, can provide a synchronization signal for implementing cross−conduction (overlap) protection for the power transistors.

Whenever XEN is HIGH, V_{GS} is LOW and the SiC MOSFET is OFF. Therefore, if XEN and the PWM input signals are both HIGH, a fault condition is detected and can be digitally assigned to take whatever precautions might be desired. XEN can also be used as a control signal for cross−conduction prevention between a high−side and low−side switch used in a half or full−bridge configuration. The schematic diagram shown in Figure 33 illustrates a circuit example how to utilize the XEN signals for fault detection and cross−conduction prevention. As can be seen in this implementation, the functions are independent and it is up to the designer to decide whether any one or both functions are needed to be implemented in the system.

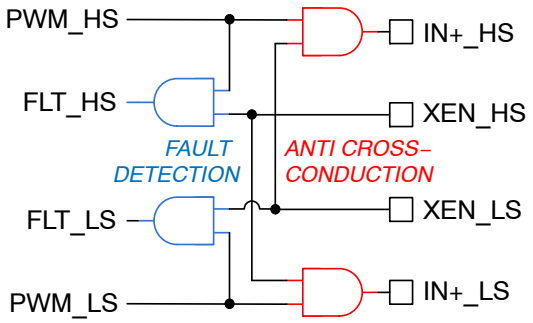


Figure 33. Examples of XEN Signal Usage

If XEN_HS transitions from LOW to HIGH while PWM_HS is HIGH, the PWM pulse width had been terminated early by one of the protection functions of the NCV51705. The protection function are; any of the Under Voltage Lock−Out (UVLO) protections, and Desaturation Detection (DESAT). As Figure 33 indicates a FAULT signal can be generated by a simple AND connection of the PWM input signal and the corresponding XEN output.

In case of cross−conduction prevention, the XEN signal of one driver is used to enable the operation of the other driver as depicted in a simplified manner in Figure 33. The isolation for the high side driver is not shown in the simplified schematic of Figure 33 but the operation of the system can be easily followed. While the high−side driver is ON, XEN_HS is LOW preventing any gate drive to be applied to the low−side driver. Once the high−side driver turns OFF its XEN_HS signal transitions to HIGH and the PWM_LS signal can pass through to the low−side driver. An identical sequence exists to ensure that the high−side driver cannot be turned ON until the low−side driver is OFF.

Signal Ground (SGND) and Power Ground (PGND)

Signal ground connection (SGND) is the GND for all control logic biased from the 5 V rail (V5V). Internally, the SGND and PGND pins are tied together by two anti−parallel diodes to limit ground bounce difference due to bond wire inductances during the switching actions of the high−current gate drive circuits. It is recommended to connect the SGND and PGND pins together with a short, low−impedance trace on the PCB.

PGND is the reference potential (0 V) for the high−current gate−drive circuit. Two bypass capacitors should be connected between the VDD pin and the PGND pin. One is the V_{DD} energy storage capacitor, which provides bias power during startup until the bootstrap power supply comes up. The value of the energy storage capacitor is a strong function of the gate charge requirement of the SiC MOSFET. It is recommended to use a minimum of 1 μF to ensure proper operation but the value is primarily dictated by the biasing scheme and startup time of the system. The second capacitor shall be a good−quality ceramic bypass capacitor, located as close as possible to the PGND and VDD pins to filter the high peak currents of the gate driver source circuit. A ceramic bypass capacitor in the range of 10 nF to 100 nF is recommended.

Similarly, two bypass capacitors should be connected between the VEE pin and the PGND pin. One is the V_{EE} energy storage capacitor, which smoothes the ripple voltage seen at output of the internal charge pump power stage. It is recommended to use a minimum of 470 nF to ensure accurate DC regulation. The second capacitor shall be a good−quality ceramic bypass capacitor, located as close as possible to the PGND and VEE pins to filter the high peak currents of the gate driver sink circuit. A ceramic bypass capacitor in the range of 10 nF to 100 nF is recommended.

Note that the exposed metal pad beneath the IC is thermally conductive but electrically not always connected to GND potential. ***Do not connect this pad to SGND or PGND***.

Programmable VEE Voltage (VEESET)

V_{EE} is regulated to the voltage set at V_{CH} which is determined by the internal low dropout regulator (LDO) voltage, programmable by the VEESET pin. The NCV51705 offers several convenient pin strapping options for VEESET. If VEESET is left floating (a 100 pF bypass capacitor from VEESET to SGND is recommended), then V_{EE} is set to regulate at −3 V. For a −5 V V_{EE} voltage, the VEESET pin should be connected directly to V5V (pin 23). If VEESET is connected to any voltage between 9 V and V_{DD}, then V_{EE} is clamped and set to regulate at the minimum charge pump voltage of −8 V. The charge pump

starts when V_{DD} > 7.5 V. Additionally, the V_{EE} voltage rail includes an internally fixed under−voltage lockout (UVLO) set to 80% of the programmed V_{EE} value. Since V_{DD} and V_{EE} are each monitored by independent UVLO circuits, the NCV51705 is smart enough to realize when both voltage rails are within limits deemed safe for switching a given SiC MOSFET.

Some SiC MOSFETs can operate between 0 V and VDD. For these applications, 0 V<OUT<V_{DD} switching can be achieved by disabling the charge pump entirely. When VEESET is connected to SGND and VEE is connected to PGND, the charge pump is disabled. With the charge pump disabled and V_{EE} tied directly to PGND, the output switches between 0 V<OUT<V_{DD}. During this mode of operation the internal V_{EE} UVLO function is also disabled accordingly.

Another configuration is to disable the charge pump but allow the use of an external negative V_{EE} voltage rail. This option permits −V_{EE}<OUT<V_{DD} switching with a slight savings in IC power dissipation, since the charge pump is not switching. With VEESET connected to SGND, an external negative voltage rail, $V_{EE(EXT)}$, can be connected directly between VEE and PGND as shown in (bold highlight) Figure 34. $V_{EE(EXT)}$ can be supplied from a dedicated bias winding, LDO or an external negative DC power converter. When using an external $V_{EE(EXT)}$ bias, be mindful that since VEESET is 0 V, the internal V_{EE} UVLO is disabled and therefore the NCV51705 is unaware if the V_{EE} voltage level is within or outside of the expected range.

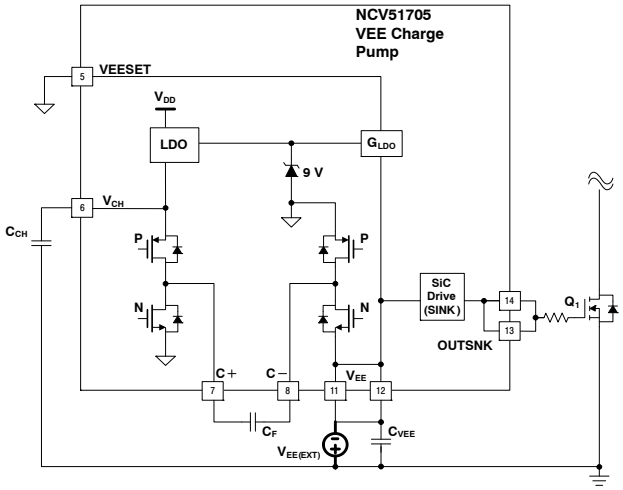


Figure 34. Supplying VEE with Negative External Voltage Bias

If none of the pin strapping options provide the desired V_{EE} negative bias voltage, the VEESET pin can be programmed using an external voltage bias. An external LDO from VDD or a simple resistive divider connected between VDD and SGND can be used as shown in (bold highlight) Figure 35.

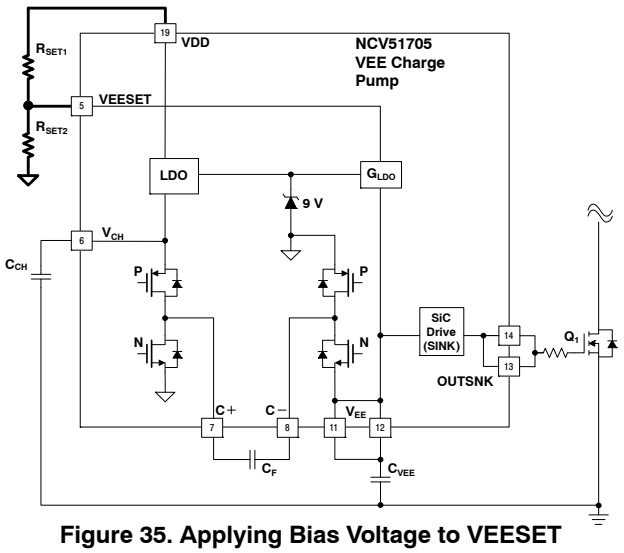


Figure 35. Applying Bias Voltage to VEESET

The VEE voltage can programmed from −3.4 V < VEE < −7.6 V for a range of VEESET bias voltage between 1.5 V < VEESET < 10.5 V. The absolute minimum programmable VEE voltage is −3 V and can be set by applying 1 V to VEESET, or by simply leaving the VEESET pin floating. For any VEESET voltage greater than 10.5 V, up to VDD, the VEE voltage rail is clamped to an absolute maximum programmable voltage of −7.6 V. The range of programmable VEE negative voltage versus VEESET bias voltage is shown graphically in Figure 36.

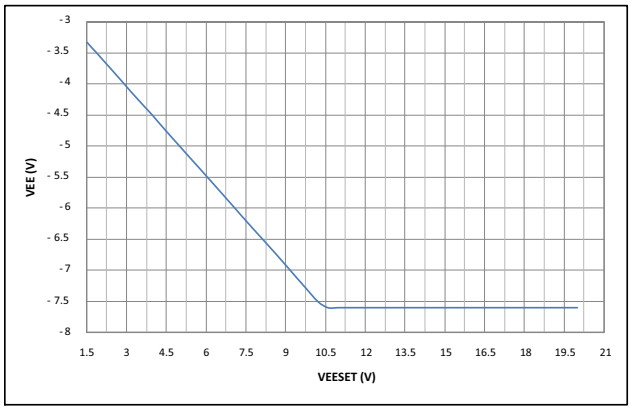


Figure 36. VEE vs. VEESET Bias Voltage

The configurability of the VEESET pin is summarized in Table 11.

Table 11. SUMMARY OF VEESET PIN CONFIGURATION

VEESET	COMMENT	V_{EE}	$V_{EE(UVLO)}$
V_{DD}	10.5 V<VEESET<V_{DD}	−8 V	−6.4 V
V5V		−5 V	−4 V
OPEN	Add C_{VEE}≤100 pF from VEESET to SGND	−3.4 V	−2.72 V
SGND	Remove C_{VEE} and connect V_{EE} to PGND	0 V	NA
SGND	Connect V_{EE} to external negative voltage supply	$-V_{EXT}$	NA
Resistor divider	Resistor divider from V_{DD} to SGND	Variable	NA

Charge Pump Configuration (VCH, C+, C− and VEE)

As can be seen from the charge pump functional block diagram shown in Figure 37, only three external capacitors (C_{CH}, C_F and C_{VEE}) are required to establish the negative V_{EE} voltage rail. The charge pump power stage essentially consists of two PMOS and two NMOS switches arranged in a bridge configuration.

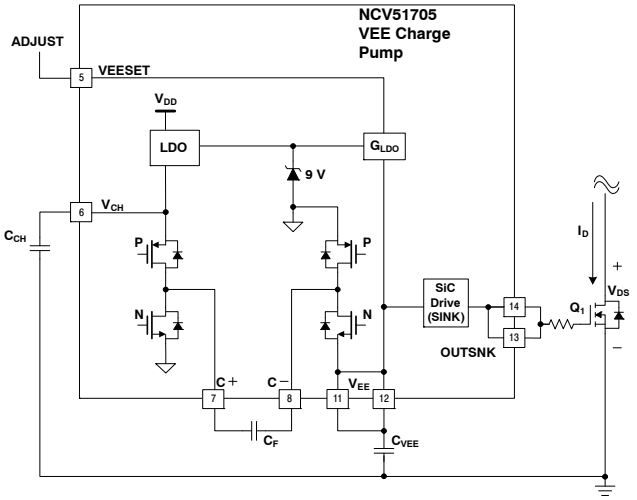


Figure 37. NCV51705 V_{EE} Charge Pump

An external flying capacitor, C_F, is connected between the midpoints of each leg of the bridge as shown. The switching frequency is internally set at 390 kHz. The V_{EE} output is seen at the VEE pin and is released after V_{DD}>7 V. Once V_{EE} exceeds 80% of the set amplitude, the VEE power rail is deemed sufficient and the VEE Under Voltage Lock Out no longer prevents switching.

Output (OUTSNK and OUTSRC)

The NCV51705 output is driven by a pure MOS, low−impedance totem pole output stage to ensure full VEE to VDD, rail−to−rail switching. The output slew rate is determined primarily by V_{DD}, V_{EE} and the C_{iss} of the SiC MOSFET. The turn−on (OUTSRC) and turn−off (OUTSNK) functions each have dual dedicated pins. This allows a single resistor between each pin and the SiC MOSFET gate to independently control gate ringing as well as fine tuning dV_{DS}/dT turn−on and turn−off transitions present on the SiC drain−source voltage. The driver provides the high peak currents necessary for high−speed switching, even at the higher Miller plateau voltage typical of SiC MOSFETs. The outputs of the NCV51705 (OUTSRC, OUTSNK) are rated to 6 A peak current capability.

Programmable Under−Voltage Lockout (UVSET)

UVLO for a gate driver IC is important for protecting the MOSFET by disabling the output until V_{DD} is above a known threshold. This not only protects the load but verifies to the controller that the applied V_{DD} voltage is above the turn−on threshold. Because the on−resistance of a SiC MOSFET has a strong dependency on V_{GS} (and therefore V_{DD}), allowing the driver output to switch at low V_{DD} can be detrimental for one SiC MOSFET but may be acceptable for another depending on heat−sinking, cooling and V_{DD} start−up time. The optimal UVLO turn−on threshold can also vary depending on how the V_{DD} voltage rail is derived. Some power systems may have a dedicated, housekeeping, bias supply while others might rely on a V_{DD} bootstrapping technique.

The NCV51705 addresses this need through a programmable UVLO turn−on threshold that can be set with a single resistor between UVSET and SGND. As shown in Figure 38, the UVSET pin is internally driven by a 25 μA current source. The UVSET resistor, R_{UVSET}, is chosen according to a desired UVLO turn−on voltage, V_{ON}, as defined by:

$$R_{UVSET} = \frac{V_{ON}}{6 \times 25\ \mu A} \qquad \text{(eq. 1)}$$

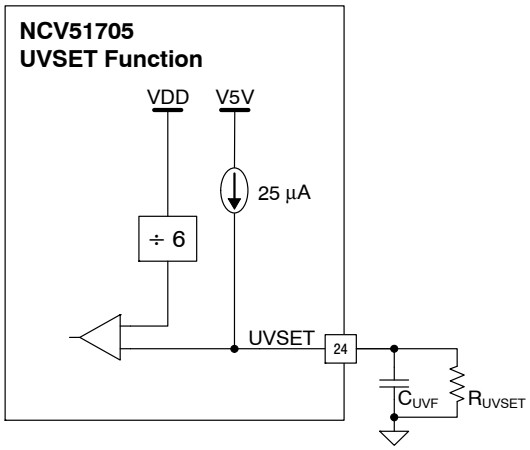


Figure 38. NCV51705 UVSET Programmable UVLO

The value for V_{ON} is typically determined by referencing the SiC MOSFET voltage versus current, output characteristic curves. Because the on−resistance of a SiC MOSFET dramatically increases even for a slight decrease

in V_{GS}, the allowable UVLO hysteresis must be small. For this reason, the NCV51705 has a fixed 1 V hysteresis so that the turn−off voltage, V_{OFF}, is always 1 V less than the set V_{ON}. Due to the narrow, 1 V hysteresis band, a small filter capacitor, C_{UVF}, is recommended to prevent any periodic or random noise disturbances on the UVSET pin. A ceramic capacitor in the range of 10 nF<C_{UVF}<100 nF should be placed between UVSET and SGND as close as possible to the IC.

Positive Bias Voltage (VDD and SVDD)

The positive bias voltage for the driver OUTSRC is provided through VDD. The input bias voltage to the internal 5 V regulator is provided through SVDD. VDD and SVDD should be the same value coming from the same voltage source but they are seperated to allow a small RC filter to be used at the input to SVDD. A small resistor (few Ω's) can be inserted between VDD and SVDD to help prevent any switching noise that might be present on VDD from coupling into the control logic biased by the internal 5 V regulator. In many cases this resistor may not be necessary and VDD can be connected directly to SVDD. However, it is recommended to allow a placeholder on the PCB design to accommodate this resistor until it can be determined if it is needed or not.

For V_{DD}>7 V, quiescent current ramps up linearly until the set UVLO threshold, V_{ON}, is crossed. After V_{DD}>V_{ON} and V_{EE}>$V_{EE(UVLO)}$, the IC is properly biased to allow output switching. Except for the case when VEESET=SGND (VEE=0 V), both VDD and VEE UVLO conditions must be met before output switching can ensue. Two bypass capacitors must be used between VDD and PGND as detailed in Signal Ground (SGND) and Power Ground (PGND) section.

Over−Current Protection (DESAT)

The implementation of the NCV51705 DESAT function can be realized using only two external components. As shown in Figure 39, the drain−source voltage of the SiC MOSFET, Q_1 is monitored via the DESAT pin through R_1 and D_1.

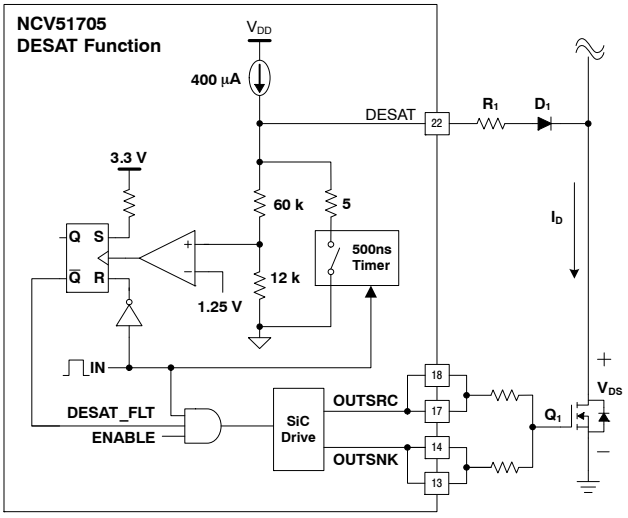


Figure 39. NCV51705 DESAT Function

During the time that Q_1 is off several hundred volts can appear across the drain−source terminals. Once Q_1 is turned on, the drain−source voltage rapidly falls and this transition from high−voltage to near zero voltage is expected to happen in less than a few hundred nano−seconds. During the turn−on transition, the leading edge of the DESAT signal is blanked by a 500 ns timer, consisting of a 5 Ω, low impedance pull−down resistance. This allows sufficient time for V_{DS} to fall while at the same time ensuring DESAT is not inadvertently activated. After 500 ns, the DESAT pin is released and the 400 μA current source provides a constant current through R_1, D_1 and the SiC MOSFET on−resistance. During the on−time, if the DESAT pin rises above 7.5 V, the DESAT comparator output goes HIGH which triggers the clock input of an RS latch. Such a fault will reduce the on−time of the Q_NOT output on a cycle−by−cycle basis.

The 400 μA current source is sufficient to ensure a predictable forward voltage drop across D_1 while also allowing the voltage drop across R_1 to be independent of V_{DS} during the on−time of the SiC MOSFET. If desired, DESAT protection can be disabled by connecting the DESAT pin to ground. Conversely, if the DESAT pin is left floating, or R_1 fails open, the 400 μA current source flowing through the 12 kΩ resistor, puts a constant 4.8 V on the non−inverting input of the DESAT comparator. This condition essentially disables the gate drive to the SiC MOSFET. The voltage on the DESAT pin, V_{DESAT}, is determined as:

$$V_{DESAT} = (400\ \mu A \times R_1) + V_{D1} + (I_D \times R_{DS}) \quad \text{(eq. 2)}$$

After assigning the maximum value for I_D (plus allowing any additional design margin) R_1 and I_D are selected such that V_{DESAT}<7.5 V. Solving for R_1 gives:

$$R_1 = \frac{V_{DESAT} - V_{D1} - (I_D \times R_{DS})}{400\ \mu A} \quad \text{(eq. 3)}$$

In addition to setting the maximum allowable V_{DS} voltage, R_1 also serves the dual purpose of limiting the instantaneous current through the junction capacitance of

D_1. Because the drain voltage on the SiC MOSFET sees extremely high dV/dt, the current through the p−n junction capacitance of D_1 can become very high if R_1 is not sized appropriately. Therefore, selecting a fast, high−voltage diode with lowest junction capacitance should be a priority. Typical values for R_1 will be near the range of 5 kΩ<R_1<10 kΩ but this can vary according to the I_D and R_{DS} parameters of the selected SiC MOSFET. If R_1 is much smaller than 5 kΩ, the instantaneous current into the DESAT pin can be hundreds of milliamps, which is problematic to the 400 μA internal DESAT current source. Conversely, if R_1 is much larger than 10 kΩ, a *RC* delay ensues as a product of R_1 and the junction capacitance of D_1. The delay can be on the order of few μs, resulting in an additional delay time responding to an over current condition.

5 V Bias (V5V)

This is the bypass capacitor pin for the internal 5 V bias rail powering the control circuitry. The recommended capacitor value is 2.2 μF. At least a 1 μF, good−quality, high−frequency, ceramic capacitor should be placed in close proximity to the pin. A smaller ceramic capacitor value such as 100 nF will assure stability but may result in a 500 mV overshoot on the 5 V rail during start−up. The 5 V rail starts to rise approximately 30 μs after V_{DD} is applied. Once the 7 V threshold is exceeded at the VDD pin, the 5 V rail is enabled. The V5V pin can source up to 10 mA making it suitable for use as a low power bias supply for housekeeping circuits such as open collector pull−up, optocoupler or digital isolator bias.

PCB Guideline

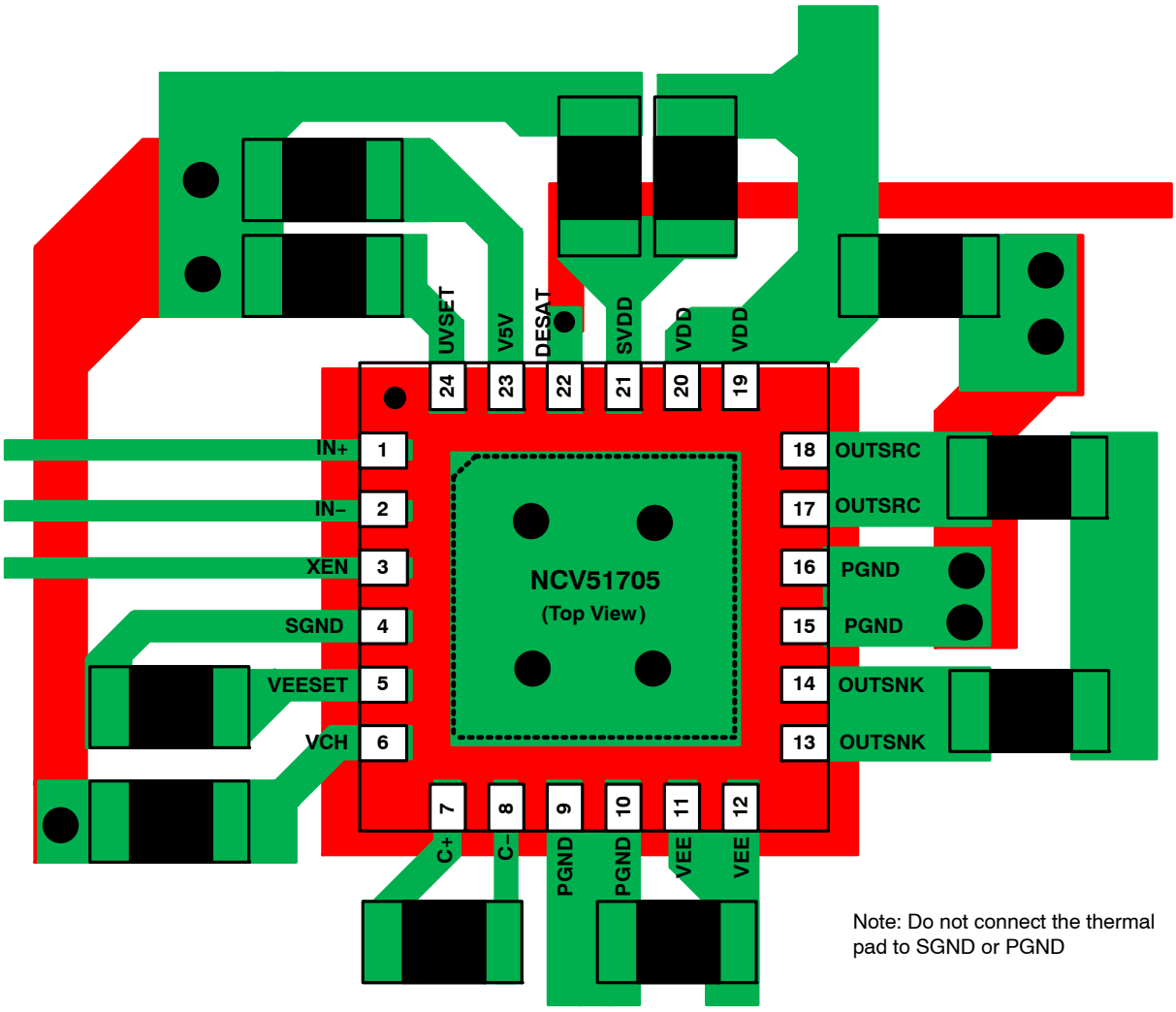


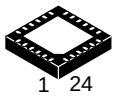
Figure 40. Recommend PCB Drawing

First of all, to optimize operation of SiC gate driving should be minimize influence of the parasitic inductance and capacitance on the layout. The following should be considered before beginning a PCB layout using the NCV51705.

- The SiC driver should be located as close as possible to the SiC MOSFET.
- VDD, SVDD, V5V, Charge Pump and VEE capacitor should be located as close as possible to the device.
- When the VEESET = GND, the VEE should be as close as possible to the PGND trace.
- Driver input and DESAT should not be close to the high dV/dT traces. It can cause abnormal operation with significant noise.
- If the device operates in the high temperature condition, use thermal via distribution from exposed pad to the other layer to make the thermal resistance as low as possible. In this case, do not connect the thermal pad to SGND or PGND.
- Use wide traces for OUTSRC, OUTSNK and VEE related with main gate driving path.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

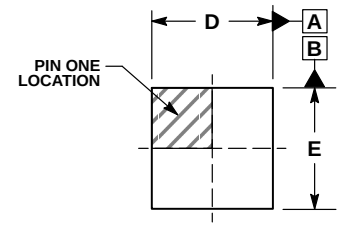
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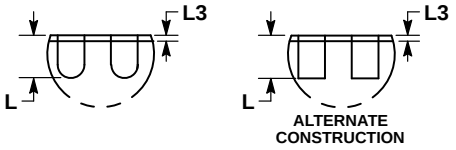
SCALE 2:1

QFNW24 4x4, 0.5P
CASE 484AE
ISSUE A

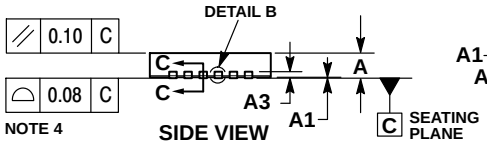
DATE 07 AUG 2018



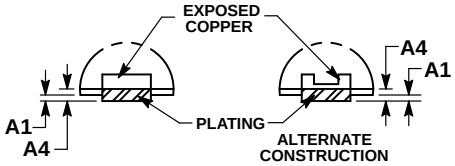
TOP VIEW



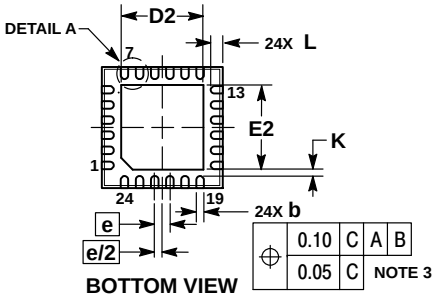
DETAIL A



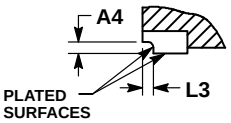
SIDE VIEW



DETAIL B



BOTTOM VIEW



SECTION C−C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	–––	–––	0.05
A3		0.20 REF	
A4	0.10	–––	–––
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e		0.50 BSC	
K	0.20	–––	–––
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

GENERIC MARKING DIAGRAM*

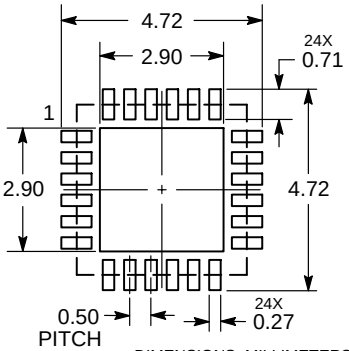


XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**QFNW24 4x4, 0.5P**		**PAGE 1 OF 1**

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