System Basis Chip with CAN FD, LDO Regulator and HS Driver

NCV7450

The system basis chip (SBC) NCV7450 integrates +5 V / 250 mA LDO regulator with a high−speed CAN FD transceiver and one high−side driver with diagnostics, directly controlled by dedicated pins.

Features

- 5 V ±2% / 250 mA LDO
  - Current Limitation with Fold−back
  - Output Voltage Monitoring
- One High−Speed CAN FD Transceiver
  - Current Limitation, Reverse Current Protected
  - Compliant to ISO11898−2:2016
  - CAN FD Timing Specified up to 5 Mbit/s
  - TxDC Timeout
- One High−Side Driver
  - Rdson = 300 mΩ @ 25°C
  - Current Limitation
  - Diagnostic Output
  - Overcurrent Protection
  - Underload Detection
- Direct Control
- Window Watchdog
- Two−level Thermal Shutdown Protection
- AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant

Typical Applications

- Automotive
- Industrial Networks

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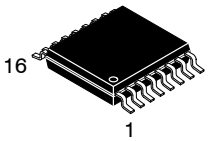
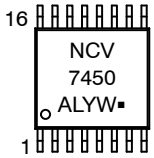


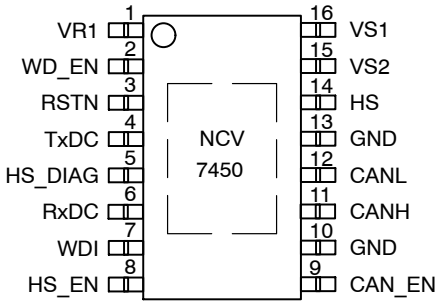
TSSOP16−EP
CASE 948BV

MARKING DIAGRAM



NCV7450	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV7450DB0R2G	TSSOP16−EP (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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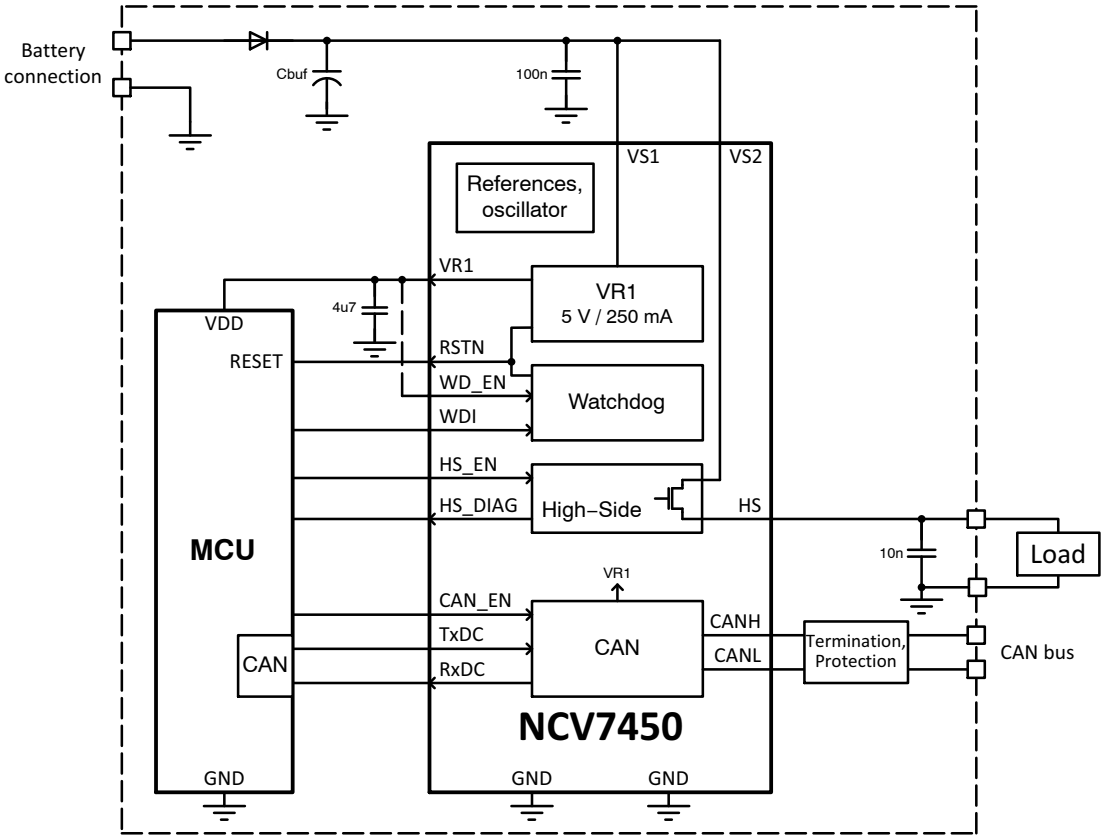

Figure 1. Simplified Application Diagram

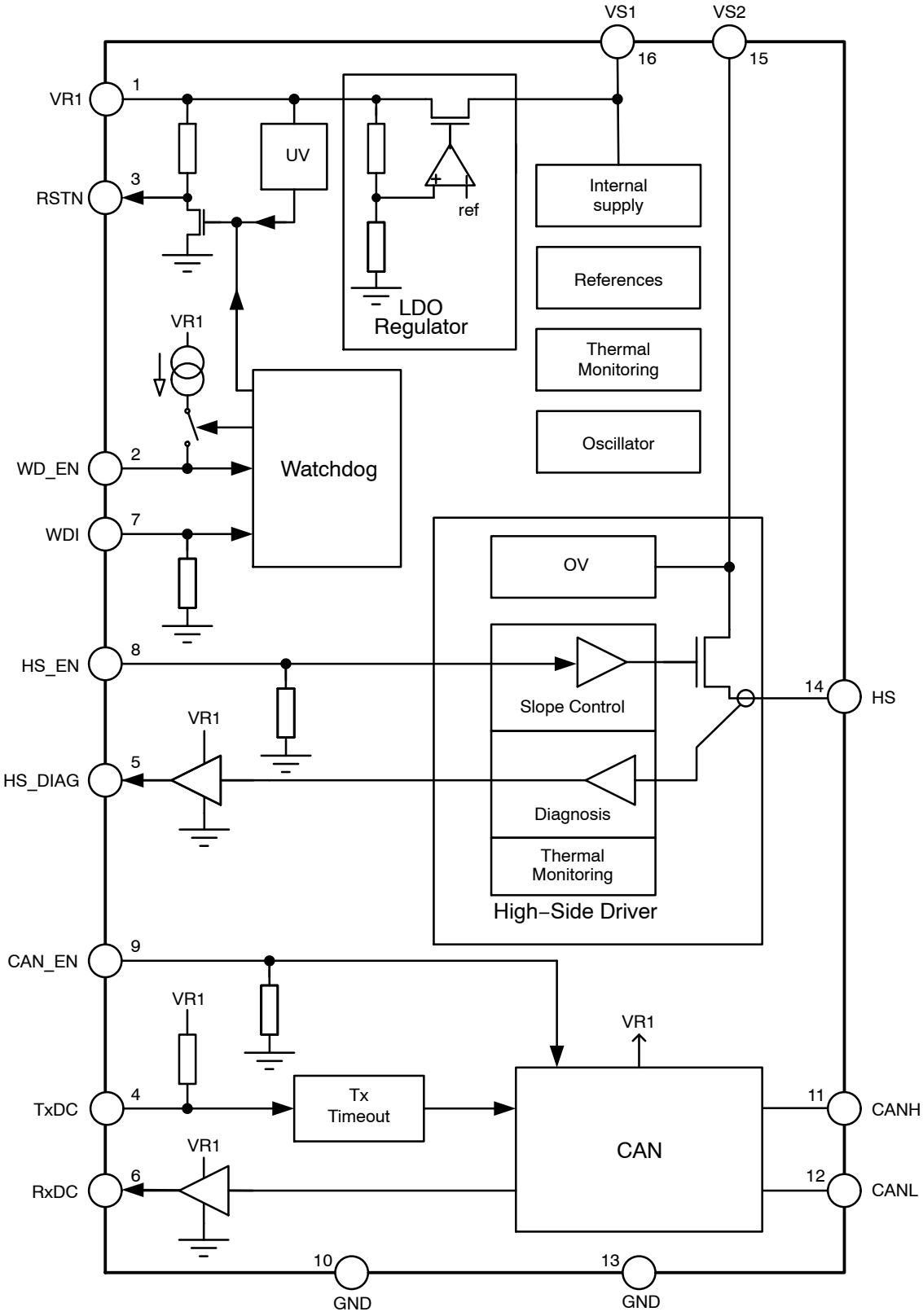

Figure 2. Block Diagram

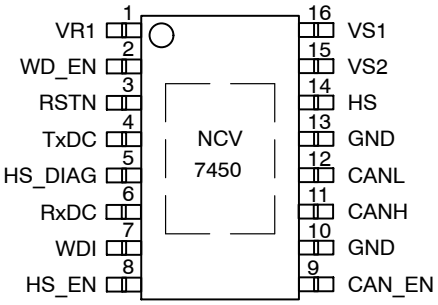

Table 1. PIN DESCRIPTION

Pin No.	Pin Name	Pin Type (LV = Low Voltage; HV = High Voltage)	Description
1	VR1	LV supply output	Output of the 5 V / 250 mA low−drop regulator
2	WD_EN	LV digital input; internal pull−up current	Watchdog enable input
3	RSTN	LV digital output; open drain; internal pull−up	Reset signal to the MCU
4	TxDC	LV digital input; internal pull−up	CAN transmitter data input
5	HS_DIAG	LV digital output; push−pull	HS driver diagnostic output (active Low)
6	RxDC	LV digital output; push−pull	CAN receiver data output
7	WDI	LV digital input; internal pull−down	Watchdog trigger input
8	HS_EN	LV digital input; internal pull−down	HS driver enable input
9	CAN_EN	LV digital input; internal pull−down	CAN transceiver enable input
10	GND	Ground connection	Ground supply (all GND pins have to be connected externally)
11	CANH	CAN bus interface	CANH line of the CAN bus
12	CANL	CAN bus interface	CANL line of the CAN bus
13	GND	Ground connection	Ground supply (all GND pins have to be connected externally)
14	HS	HV output; high−side	High−side driver output
15	VS2	HV supply input	Main supply input (HS Driver), keep floating if HS driver not used
16	VS1	HV supply input	Main supply input (VR1, logic)
	EP	Exposed pad	Substrate (has to be connected to all GND pins externally)

Table 2. MAXIMUM RATINGS

Symbol	Rating		Min	Max	Unit
Vmax_VS1	DC Power Supply Voltage (Note 1)		−0.3	40	V
Vmax_VS2	DC Power Supply Voltage (Note 1)		−0.3	40	V
Vmax_HS	DC High−side driver Voltage		−0.3	VS2+0.3	V
Vmax_digIO	DC voltage on digital pins (CAN_EN, WD_EN, WDI, RSTN, RxDC, TxDC, HS_EN, HS_DIAG)		−0.3	VR1+0.3	V
Vmax_CAN	DC voltage on pin CANH and CANL		−40	40	V
Vmax_diff	Differential DC voltage between any two pins (incl. CANH and CANL)		−40	40	V
Vmax_VR1	LDO Supply pin output voltage		−0.3	6 or VS1+0.3 (whichever is lower)	V
Tj	Junction Temperature Range		−40	150	°C
Tstg	Storage Temperature Range		−55	150	°C
Tsld	Peak Soldering Temperature (Note 3)			260	°C
V_ESDHBM	ESD Capability, Device HBM (Note 2)	Pins VS1/2, CANH, CANL, HS	−5	+5	kV
V_ESDHBM	ESD Capability, Device HBM (Note 2)	All other pins	−4	+4	kV
V_ESDMM	ESD Capability, Machine Model (Note 2)		−250	+250	V
V_ESDCDM	ESD Capability, Charged Device Model (Note 2)		−750	+750	V
V_ESDIEC	ESD Capability, System HBM (Note 2), pins VS1/2, CANH, CANL, HS		−6	+6	kV
V_SCHAF	Voltage transients per ISO7637 − 3, Class D, pins VS1/2, CANH and CANL	Test pulse 1	−100	–	V
		Test pulse 2a	–	+75	V
		Test pulse 3a	−150	–	V
		Test pulse 3b	–	+100	V
MSL	Moisture Sensitivity Level		2		–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   Device ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   Device ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Device ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   System ESD Human Body Model tested per IEC61000−4−2 (150 pF, 330 Ω)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
	Thermal Characteristics,		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Air (Note 4)	54	
$R_{\psi JA}$	Thermal Resistance, Junction−to−Air (Note 5)	81	
	Thermal Characteristics,		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	10.5	

4. Value based on test board according to JESD51−3 standard, signal layer with 10% trace coverage.
5. Value based on test board according to JESD51−7 standard, signal layers with 20% trace coverage, inner planes with 90% coverage.

Table 4. RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Max	Unit
VS1	Functional supply voltage	5	28	V
	Supply voltage for valid parameter specification	6	18	V
VS2	Functional supply voltage	4.3	24	V
	Supply voltage for valid parameter specification	6	18	V
VR1	VR1 LDO output voltage	4.9	5.1	V
VdigIO	Digital inputs/outputs voltage	0	VR1	V
HS	High−side driver voltage	0	VS2	V
CANH, CANL	CAN bus pins voltage	−40	40	V
T_J	Junction Temperature	−40	150	°C
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS (6 V ≤ Vs1 = Vs2 ≤ 18 V; −40°C ≤ Tj ≤ 150°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VS1, VS2 SUPPLY						
VS_PORH	VS1 POR threshold	VS1 rising	3.4	–	4.1	V
VS_PORL	VS1 POR threshold	VS1 falling	2.0	–	3.5	V
Is1_off	VS1 consumption, low−power	VS1 = VS2 = 14 V, VR1 on (not loaded), HS load to GND, CAN bus recessive, CAN_EN = Low, HS_EN = Low, WD_EN = Low, Tj ≤ 85°C	–	25	–	μA
Is2_off	VS2 consumption, low−power	VS1 = VS2 = 14 V, HS load to GND, HS_EN = Low, Tj ≤ 85°C	–	4	–	μA
Is_act	VS1+VS2 consumption, active	VS1 = VS2 = 14 V, VR1 on (loaded by 100 mA, not included in Is_act), HS floating, CAN bus recessive, CAN_EN = High, HS_EN = High, WD_EN = High, TxDC = High	–	10	20	mA
VS2_OV	VS2 overvoltage	HS_EN = High	28	–	–	V
VS2_OV_hyst	VS2 overvoltage hysteresis	HS_EN = High	–	1	–	V
tfilt_VS2_OV	VS2 overvoltage filter time	VS2 rising	60	–	105	μs
VR1 VOLTAGE REGULATOR						
V_VR1	Regulator output voltage	0 mA ≤ I(VR1) ≤ 250 mA, 6 V ≤ VS1 ≤ 28 V	4.9	5.0	5.1	V
Iout_VR1	Regulator output current	Maximum VR1 load current	–	–	250	mA
Ilim_VR1	Regulator current limitation	Maximum VR1 overload current, VR1 > RES_VR1	400	–	1000	mA
Ishort_VR1	Regulator short current	Maximum VR1 short current, VR1 < RES_VR1	133	1/3 x Ilim_VR1	333	mA
Vdrop_VR1	Dropout Voltage	I(VR1) = 100 mA, VS1 = 5 V				V
		·Tj ≤ 150°C	–	–	0.4	
		·Tj ≤ 40°C (Note 6)	–	0.2	–	
		·Tj = −40°C	–	–	0.2	
		I(VR1) = 100 mA, VS1 = 4.5 V	–	–	0.5	
		I(VR1) = 50 mA, VS1 = 4.5 V	–	–	0.4	
Loadreg_VR1	Load Regulation	1 mA ≤ I(VR1) ≤ 100 mA	−50	–	50	mV
Linereg_VR1	Line Regulation	I(VR1) ≤ 100 mA	−30	–	30	mV
Cload_VR1	VR1 load capacity	ESR < 200 mΩ, ceramic capacitor recommended	1	4.7	–	μF

Table 5. ELECTRICAL CHARACTERISTICS (6 V ≤ Vs1 = Vs2 ≤ 18 V; −40°C ≤ Tj ≤ 150°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VR1 VOLTAGE REGULATOR						
RES_VR1	VR1 Reset threshold	VR1 voltage decreasing	4.3	4.5	4.7	V
RES_hyst_VR1	VR1 Reset threshold hysteresis		0.05	0.1	0.2	V
tfilt_RES_VR1	VR1 undervoltage filter time		–	15	–	μs
toff_VR1	VR1 off time after TSD		–	1.0	–	s
Is_add_VR1	VS consumption adder of VR1	(Note 6)	–	0.02 x I(VR1)	–	A
HS DRIVER						
Ron_HS	On−resistance	Tj = 25°C (Note 6)	–	0.3	–	Ω
		Tj = 125°C	–	–	0.6	
		Tj = 125°C, Vs2 = 4.3 V (Note 6)	–	–	0.8	
		Tj = 150°C	–	–	0.7	
Ilim_HS	Current Limitation		−3.7	−3	−2.5	A
Ioc_HS	Overcurrent threshold		−3.7	−2.7	−1.7	A
Iuld_HS	Underload detection threshold		−40	–	−6.0	mA
Ileak_HS	Output leakage current	HS off ; V(HS) = 0 V				μA
		Tj = 25°C (Note 6)	−1	–	–	
		Tj = 150°C	−5	–	–	
td_on_HS	Output delay time	HS_EN = Low −> High; V(HS) = 0.1 x Vs2				μs
		·HS_EN was Low for more than 30 ms	–	140	–	
		·HS_EN was Low for less than 20 ms	–	40	–	
td_off_HS	Output delay time	HS_EN = High −> Low; V(HS) = 0.9 x Vs2	–	40	–	μs
td_oc_HS	Overcurrent detection filter time		–	–	65	μs
tdb_uld_HS	Underload detection blanking delay	Timer started after driver activation and V(HS) = Vs2 − 2 V	–	–	130	μs
td_uld_HS	Underload detection filter time	HS Driver active, tdb_uld_HS elapsed	–	–	70	μs
dVout_HS	Slew rate	HS load = 16 Ω to GND	–	0.2	–	V/μs
Is_add_HS	HS consumption from VS2	HS_EN = High; HS pin floating	2.0	4.4	8.0	mA
WATCHDOG TIMING (see Figure 3)						
twd_acc	Watchdog timing accuracy		−15	–	+15	%
t_wd_TO	Timeout watchdog period	After WD_EN low −> high transition or RSTN pulse	–	65	–	ms
t_wd_CW	Window watchdog closed window		–	6	–	ms
t_wd_OW	Window watchdog open window		–	100	–	ms
t_RSTN	Reset pulse length after VR1 undervoltage or watchdog failure		–	8	–	ms
t_WDI	Minimum WDI pulse width accepted as a watchdog service		6.0	–	–	μs
DIGITAL OUTPUTS, RxDC, HS_DIAG						
IoutL_pinx	Low−level output driving current	pinx is logical Low, forced V(pinx) = 0.4 V	1.0	6	12	mA
IoutH_pinx	High−level output driving current	pinx is logical High, forced V(pinx) = VR1 − 0.4 V	−8.0	−3	−1.0	mA
DIGITAL OUTPUT RSTN						
IoutL_RSTN	Low−level output driving current	RSTN is active (logical Low), forced V(RSTN) = 0.4 V	2.0	5	12	mA

Table 5. ELECTRICAL CHARACTERISTICS (6 V ≤ Vs1 = Vs2 ≤ 18 V; −40°C ≤ Tj ≤ 150°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUT RSTN						
VoutL_RSTN	Low−level output voltage, low VR1/VS1	VR1 > 4.7 V, I(RSTN) = 0.7 mA	−	−	0.4	V
		VR1 > 2 V, VS1 < VR1, I(RSTN) = 0.1 mA	−	−	0.4	
		VS1 > 2 V, I(RSTN) = 0.3 mA	−	−	0.4	
Rpullup_RSTN	Internal pull−up resistor to VR1		5.0	10	19	kΩ
DIGITAL INPUTS TxDC, CAN_EN, WD_EN, HS_EN, WDI						
VinL_pinx	Low−level input voltage (logical “Low”)		0	−	0.8	V
VinH_pinx	High−level input voltage (logical “High”)		2.0	−	VR1	V
Vin_hys_pinx	Input voltage hysteresis		100	−	500	mV
Rpullup_pinx	Internal pull−up resistor to VR1; pin TxDC		55	100	185	kΩ
Rpulldown_pinx	Internal pull−down resistor to ground; pins CAN_EN, HS_EN, WDI		55	100	185	kΩ
Ipullup_WD_EN	Internal pull−up current to VR1, pin WD_EN	V(WD_EN) = 0 V, pull−up current source active	50	100	200	μA
tper_pullup_WDEN	WD_EN pull−up current source activation period	WD_EN = CAN_EN = HS_EN = Low	−	610	−	μs
ton_pullup_WDEN	WD_EN pull−up current source activation on−time	WD_EN = CAN_EN = HS_EN = Low	−	5.0	−	μs
THERMAL PROTECTION						
Tsd1	Thermal shutdown level 1	Temperature increasing; HS switched off consequently	145	155	165	°C
Tsd2	Thermal shutdown level 2	Temperature increasing; VR1 and CAN switched off consequently	165	175	185	°C
Tsd1_off	Thermal shutdown recovery temperature	Temperature decreasing; HS switched on	135	145	155	°C

6. Not tested in production, guaranteed by design.

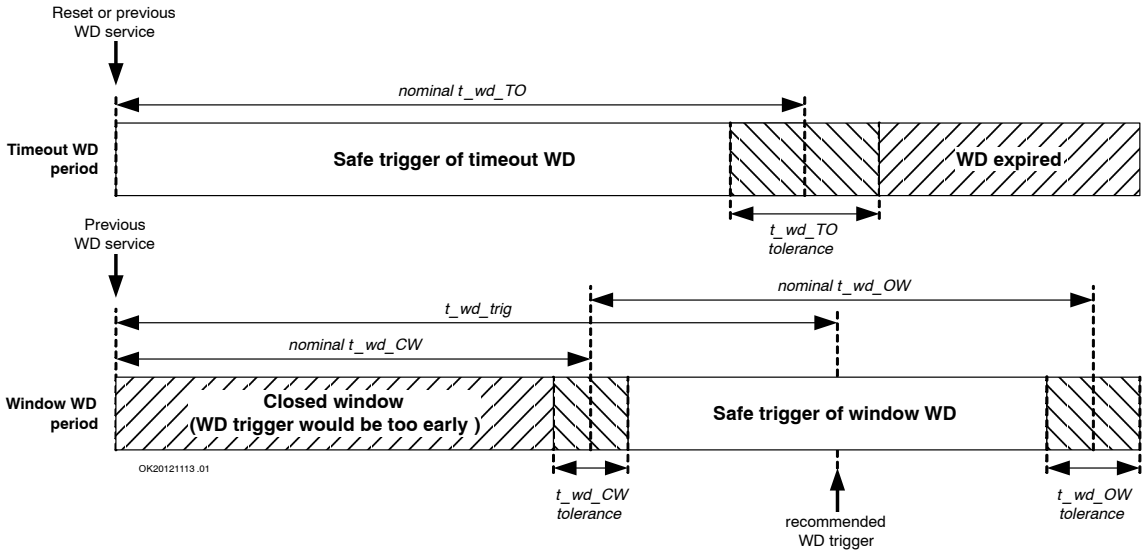

Figure 3. Watchdog modes timing

Table 6. ELECTRICAL CHARACTERISTICS (CONTINUED)

(VR1 = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used unless specified otherwise.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN BUS LINES (Pins CANH and CANL)						
$I_{o(rec)}$	Recessive output current at pins CANH and CANL	CAN enabled; −27 V < $V_{CANH/L}$ < +32 V	−5.0	–	+5.0	mA
I_{LI}	Input leakage current	0 < R(VR1 to GND) < 1 MΩ V_{CANH} = V_{CANH} = 5 V	−5.0	0	+5.0	μA
$V_{o(rec)\ (CANH)}$	Recessive output voltage at pin CANH	CAN enabled; V_{TxDC} = VR1	2.0	2.5	3.0	V
$V_{o(rec)\ (CANL)}$	Recessive output voltage at pin CANL	CAN enabled; V_{TxDC} = VR1	2.0	2.5	3.0	V
$V_{o(off)\ (CANH)}$	Recessive output voltage at pin CANH	CAN disabled	−0.1	0	0.1	V
$V_{o(off)\ (CANL)}$	Recessive output voltage at pin CANL	CAN disabled	−0.1	0	0.1	V
$V_{o(off)\ (diff)}$	Differential bus output voltage in off mode (V_{CANH} − V_{CANL})	CAN disabled	−0.2	0	0.2	V
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	50 Ω < R_{LT} < 65 Ω; V_{TxDC} = 0 V; t < $t_{dom(TxDC)}$	2.75	3.5	4.5	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	50 Ω < R_{LT} < 65 Ω; V_{TxDC} = 0 V; t < $t_{dom(TxDC)}$	0.5	1.5	2.25	V
$V_{o(dom)(sym)}$	Dominant output CANH/CANL drivers symmetry (V_{CANH} + V_{CANL})	R_{LT} = 60 Ω; C_1 = 4.7 nF; TxDC driven by square wave up to 1 MHz	0.9		1.1	VR1
$V_{o(dom)\ (diff)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxDC} = 0 V; dominant; 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(dom)\ (diff)_arb}$	Differential bus output voltage during arbitration (V_{CANH} − V_{CANL})	V_{TxDC} = 0 V; dominant; R_{LT} = 2240 Ω; (Note 7)	1.5		5.0	V
$V_{o(rec)\ (diff)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxDC} = VR1; recessive; no load	−50	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} = −3 V; V_{TxDC} = 0 V −3 V ≤ V_{CANH} ≤ +18 V	−100 −100	−70	−40 1.0	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} = 36 V; V_{TxDC} = 0 V −3 V ≤ V_{CANL} ≤ +18 V	40 −1.0	70	100 100	mA
$V_{i(th)(diff)_NORM}$	Differential receiver threshold voltage in normal mode	CAN enabled; −12 V ≤ V_{CANH} ≤ +12 V; −12 V ≤ V_{CANL} ≤ +12 V	0.5	–	0.9	V
$V_{i(rec)(diff)_NORM}$	Differential receiver input voltage for recessive state in normal mode	CAN enabled; −12 V ≤ V_{CANH} ≤ +12 V; −12 V ≤ V_{CANL} ≤ +12 V	−3.0	–	0.5	V
$V_{i(dom)(diff)_NORM}$	Differential receiver input voltage for dominant state in normal mode	CAN enabled; −12 V ≤ V_{CANH} ≤ +12 V; −12 V ≤ V_{CANL} ≤ +12 V	0.9	–	8.0	V
$V_{i(th)(diff)_WU}$	Differential receiver threshold voltage in wakeup−detection mode	CAN in wakeup−detection mode; −12 V ≤ V_{CANH} ≤ +12 V; −12 V ≤ V_{CANL} ≤ +12 V	0.4	–	1.05	V
$V_{i(rec)(diff)\ _WU}$	Differential receiver input voltage for recessive state in wakeup−detection mode	CAN in wakeup−detection mode; −12 V ≤ V_{CANH} ≤ +12 V; −12 V ≤ V_{CANL} ≤ +12 V	−3.0	–	0.4	V
$V_{i(dom)(diff)_WU}$	Differential receiver input voltage for dominant state in wakeup−detection mode	CAN in wakeup−detection mode; −12 V ≤ V_{CANH} ≤ +12 V; −12 V ≤ V_{CANL} ≤ +12 V	1.05	–	8.0	V
$R_{i(cm)\ (CANH)}$	Common−mode input resistance at pin CANH	−2 V ≤ V_{CANH} ≤ +7 V; −2 V ≤ V_{CANL} ≤ +7 V	15	25	37	kΩ

Table 6. ELECTRICAL CHARACTERISTICS (CONTINUED)

(VR1 = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω, C_{LT} = 100 pF, C_1 not used unless specified otherwise.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN BUS LINES (Pins CANH and CANL)						
$R_{i(cm)\ (CANL)}$	Common−mode input resistance at pin CANL	−2 V ≤ V_{CANH} ≤ +7 V; −2 V ≤ V_{CANL} ≤ +7 V	15	25	37	kΩ
$R_{i(cm)\ (m)}$	Matching between pin CANH and pin CANL common mode input resistance	V_{CANH} = V_{CANL} = 5 V	−1.0	0	+1.0	%
$R_{i(diff)}$	Differential input resistance	−2 V ≤ V_{CANH} ≤ +7 V; −2 V ≤ V_{CANL} ≤ +7 V	25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TxDC} = VR1; (Note 7)	–	7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TxDC} = VR1; (Note 7)	–	7.5	20	pF
$C_{i(diff)}$	Differential input capacitance	V_{TxDC} = VR1; (Note 7)	–	3.75	10	pF
TIMING CHARACTERISTICS (see Figure 4 and Figure 5)						
$t_{d(TxDC-BUSon)}$	Delay TxDC to bus dominant		–	65	–	ns
$t_{d(TxDC-BUSoff)}$	Delay TxDC to bus recessive		–	90	–	ns
$t_{d(BUSon-RxDC)}$	Delay bus dominant to RxDC		–	60	–	ns
$t_{d(BUSoff-RxDC)}$	Delay bus recessive to RxDC		–	65	–	ns
t_{pd_dr}	Propagation delay TxDC to RxDC dominant to recessive transition		50	100	210	ns
t_{pd_rd}	Propagation delay TxDC to RxDC recessive to dominant transition		50	120	210	ns
$t_{d(stb-nm)}$	Delay wake−up detection mode to normal mode		7.0	25	47	μs
t_{wake_filt}	Dominant time for wake−up via bus	CAN_EN = low	0.15	–	1.8	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions)	Valid bus wake−up event	0.5	–	10	μs
$t_{dwakedr}$	Delay to flag wake event (dominant to recessive transitions)	Valid bus wake−up event	0.5	–	10	μs
t_{wake_to}	Bus time for wake−up timeout	CAN_EN = low	1.0	–	10	ms
$t_{dom(TxDC)}$	TxDC dominant time for timeout	CAN_EN = high; V_{TxDC} = 0 V	1.0	–	10	ms
$t_{Bit(RxDC)}$	Bit time on RxDC pin	$t_{Bit(TxDC)}$ = 500 ns	400	–	550	ns
		$t_{Bit(TxDC)}$ = 200 ns	120	–	220	ns
$t_{Bit(Vi(diff))}$	Bit time on bus (CANH − CANL pin)	$t_{Bit(TxDC)}$ = 500 ns	435	–	530	ns
		$t_{Bit(TxDC)}$ = 200 ns	155	–	210	ns
Δt_{Rec}	Receiver timing symmetry $\Delta t_{Rec} = t_{Bit(RxDC)} - t_{Bit(Vi(diff))}$	$t_{Bit(TxDC)}$ = 500 ns	−65	–	40	ns
		$t_{Bit(TxDC)}$ = 200 ns	−45	–	15	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Not tested in production, guaranteed by design.

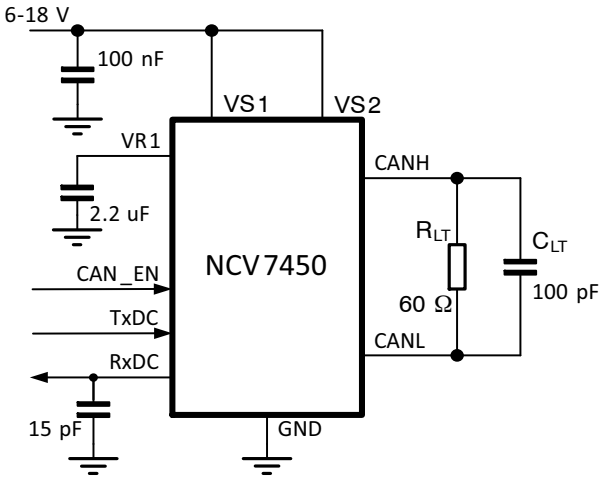

Figure 4. Test Circuit for Timing Characteristics

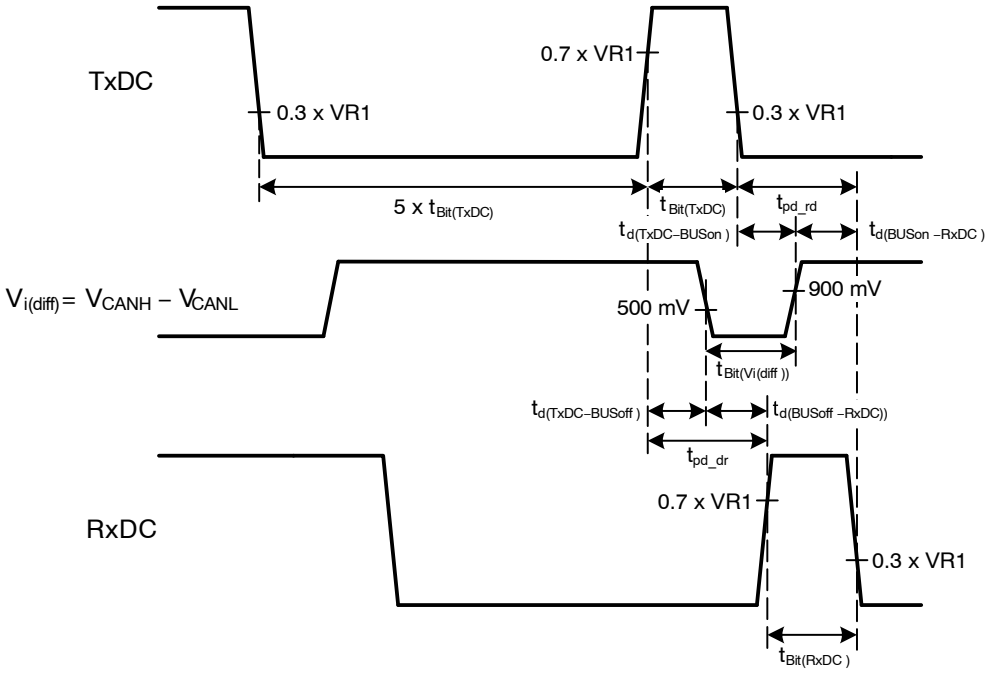

Figure 5. CAN Transceiver Timing Diagram

FUNCTIONAL DESCRIPTION

Supply Concept

The device has two independent supply pins VS1 and VS2. While VR1 regulator and logic control are supplied from VS1, High−side driver is supplied from VS2. Both supply lines have to be properly decoupled by filtration capacitors close to the device pins.

As long as VS1 < VS_POR level, all the blocks are in power−down mode.

VR1 Low−drop Regulator

VR1 is a low−drop output regulator providing 5 V voltage derived from the VS1 main supply. It is able to deliver up to 250 mA and is primarily intended to supply the on−chip CAN transceiver, the application microcontroller unit (MCU) and related 5 V loads (e.g. its own MCU−related digital inputs/outputs). An external capacitor needs to be connected on VR1 pin in order to ensure the regulator's stability and to filter the disturbances caused by the connected loads.

VR1 voltage is supplying all the digital low−voltage input/output pins.

The protection and monitoring of the VR1 regulator consist of the following features:

- VR1 Current Limitation – the two−level current limitation controlled by VR1 reset comparator to reduce the power dissipation in case of shorts to ground by the current fold−back (see Figure 7)
- VR1 Reset Comparator – the VR1 regulator output is compared with a reset level *RES_VR1*. If the VR1 level drops below this level for longer than *tflt_RES_VR1*, a reset towards the MCU is generated through the RSTN pin and peripherals (CAN transceiver and HS driver) disabled.
- Temperature (see Figure 14)

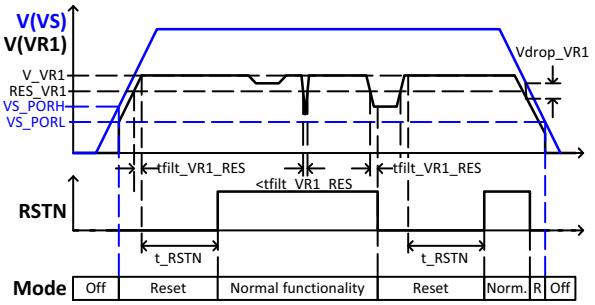

Figure 6. VR1 monitoring

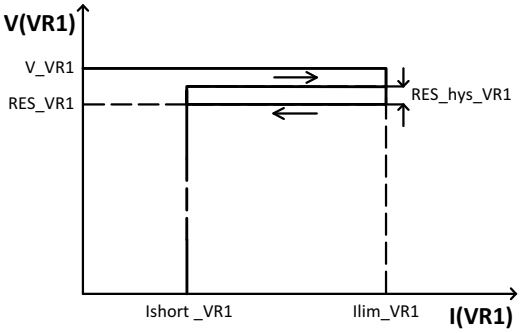

Figure 7. VR1 current fold−back

CAN Transceiver

The SBC contains one high−speed CAN transceiver compliant with ISO11898−2:2016, supporting bit rates up to 5 Mbit/s. The transceiver consists of the following sub−blocks: transmitter, receiver, and wakeup detector.

If enabled (CAN_EN = High), the CAN transceiver is ready to provide the full−speed interface between the bus and a CAN controller connected on pins RxDC (received data) and TxDC (data to transmit). The bus lines are biased to VR1 / 2.

In order to prevent a faulty node from blocking the bus traffic, the maximum length of the transmitted dominant symbol is limited by a timeout counter to *tdom(TxDC)*. In case the TxDC Low signal exceeds the timeout value, the transmitter returns automatically to the recessive state. The transmission is again de−blocked when TxDC pin returns to high (recessive) state.

If the CAN block is disabled (CAN_EN = Low) or RSTN pin active (Low) due to failed watchdog service or VR1 undervoltage, the CAN transceiver is in its wake−up detection state. The bus lines are biased to ground. Logical level on TxDC is ignored and pin RxDC is kept high until a CAN bus wake−up is detected. The CAN bus wake−up corresponds to a pattern consisting of dominant – recessive – dominant symbols of at least t_{wake_filt} each. The RxDC starts following the CAN bus afterwards. The pattern must be received within t_{wake_to} to be recognized as a valid wake−up event, otherwise internal wake−up logic is reset.

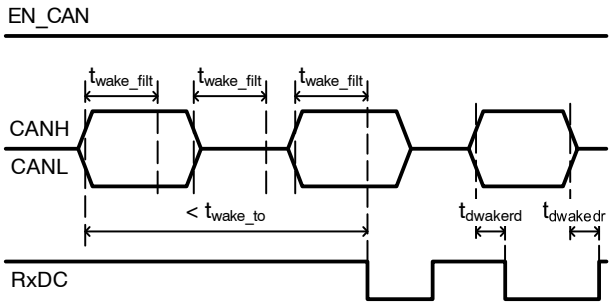

Figure 8. CAN wakeup pattern

HS Driver

HS high−side driver is intended to drive an external load. Its state is directly controlled via HS_EN pin and diagnostics are flagged on HS_DIAG pin (see Table 7).

When the driver is enabled (HS_EN = High), it is protected against an excessive current and temperature and diagnosed on Underload condition.

In case the HS driver is controlled by a PWM signal through HS_EN with very low duty−cycle, the diagnostic features are limited by *td_oc_HS* in case of an overcurrent and (VS2 / *dVout_HS)* + *td_uld_HS* in case of an underload.

The HS driver is designed to drive resistive loads. Therefore only a limited clamping energy (W < 1 mJ) can be dissipated by the device. For inductive loads (L > 100 μH) an external freewheeling diode connected between GND and the HS pin is required.

Table 7. HS Driver Diagnostics

Event	HS_EN	Failure condition	HS status	HS_DIAG	Recovery condition
Normal operation (no failure)	Low	–	Off	High	–
	High	–	On	High	–
Overcurrent	High	I(HS) > *Ioc_HS*	Off	Low	HS_EN = Low
Underload	High	I(HS) < *Iuld_HS*	On	Low	I(HS) > *Iuld_HS*
Short−to−battery					
Over−temperature	High	Tj > *Tsd1*	Off	Low	Tj < *Tsd1_off*
VS2 Overvoltage	High	VS2 > *VS2_OV*	Off	Low	VS2 < *VS2_OV*
RSTN active	High	RSTN = Low	Off	Low	RSTN = High

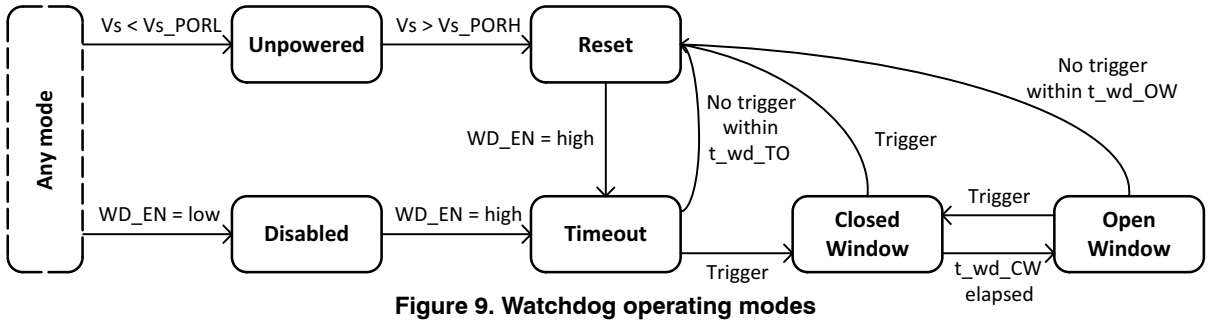

Figure 9. Watchdog operating modes

Watchdog

The on−chip watchdog requires that the MCU software “triggers” or “services” the watchdog in a specified time frame. A correct watchdog service consists of high−to−low transition on the WDI input. The watchdog timer restarts immediately after a successful trigger is received.

After any Reset event (power−up, watchdog failure, VR1 undervoltage, thermal shutdown 2) or watchdog enable (WD_EN = Low −> High), the watchdog always starts in a timeout mode. The MCU software must serve the watchdog any time before the timeout expiration. After the watchdog is triggered for the first time, it starts working in a window mode operation: the watchdog time is split to two distinct parts – a closed window, where the watchdog may not be triggered, is followed by an open window where the MCU must send a valid watchdog trigger (see Figure 10).

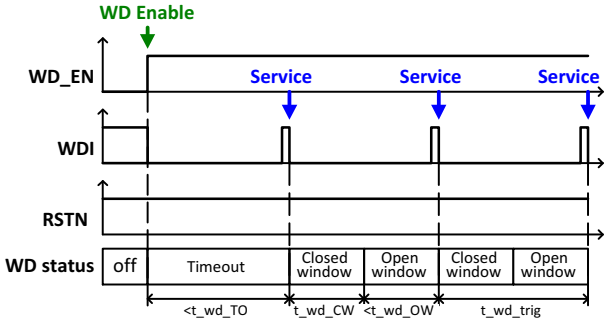

Figure 10. Correct watchdog services

In case the watchdog is not triggered before the timeout or open window elapses (Figure 11, Figure 12), or trigger is sent within the closed window (Figure 13), RSTN signal is generated and then watchdog restarted in the timeout mode again.

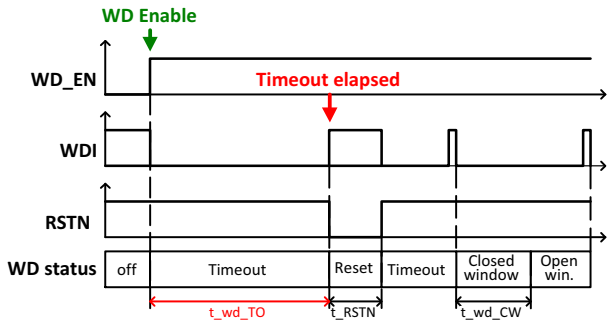

Figure 11. Missed watchdog in Timeout mode

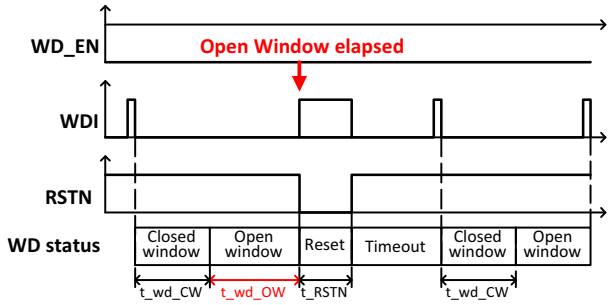

Figure 12. Missed watchdog in Window mode

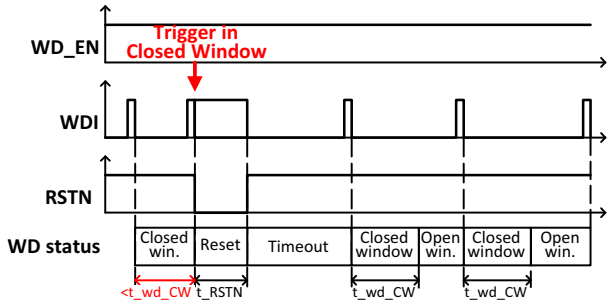

Figure 13. Watchdog service during closed window

The WD_EN pin has an integrated pull−up source to enable the watchdog in case the pin is disconnected from the application. To reduce the power consumption in the low−power mode (watchdog, CAN and HS driver disabled), the WD_EN pull−up current source is switched on for *ton_pullup_WDEN* time with period of *tper_pullup_WDEN*. The pin state is sampled in the end of the current source activation. Once High level is detected on the WD_EN pin, the current source is activated permanently.

To ensure the High level is correctly detected if the pin becomes floating, external WD_EN capacity should stay below 50 pF.

After the rising edge on WD_EN pin, the MCU should wait *tper_pullup_WDEN* before the first watchdog service.

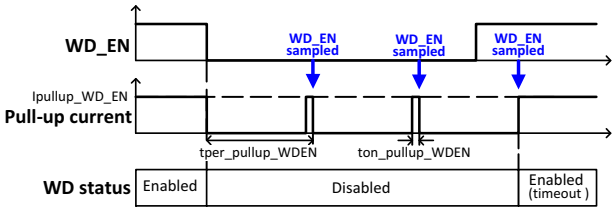

Figure 14. WD_EN pull−up current source activation

Thermal Protection

The device junction temperature is monitored in order to avoid permanent degradation or damage. Two distinct junction temperature levels are provided − thermal shutdown level 1 *Tsd1* (typ. 155°C) and thermal shutdown level 2 *Tsd2* (typ. 175°C).

When the junction temperature exceeds the first thermal shutdown level, the high−side driver is disabled while VR1 and CAN transceiver keeps running so that the MCU can still take appropriate actions. The junction temperature above the second shutdown level leads to complete device de−activation, VR1 included; the device recovers automatically after the junction temperature drops below *Tsd1* level and *toff_VR1* (typ. 1 second) elapses. HS driver functionality is recovered when the junction temperature drops below *Tsd1_off*.

The details of the thermal protection handling are shown in Figure 15.

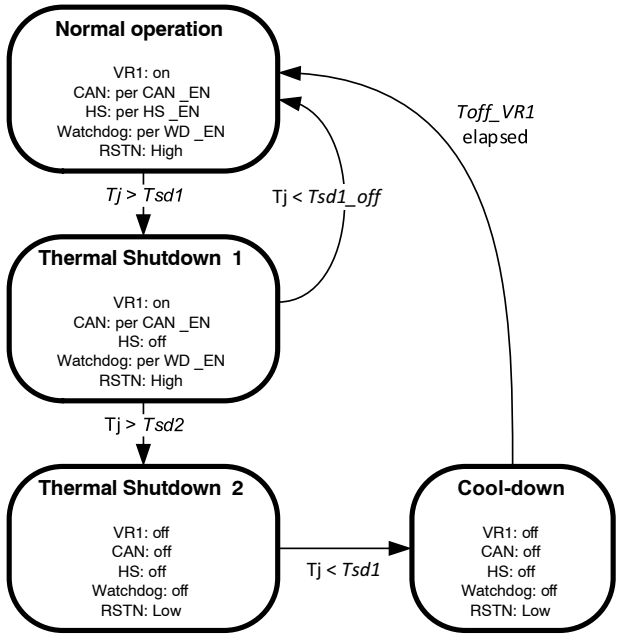

Figure 15. Thermal monitoring flow chart

Table 8. ISO11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7450 Datasheet
Parameter	**Notation**	**Symbol**
DOMINANT OUTPUT CHARACTERISTICS		
Single ended voltage on CAN_H	V_{CAN_H}	$V_{o(dom)(CANH)}$
Single ended voltage on CAN_L	V_{CAN_L}	$V_{o(dom)(CANL)}$
Differential voltage on normal bus load	V_{Diff}	$V_{o(dom)(diff)}$
Differential voltage on effective resistance during arbitration	V_{Diff}	$V_{o(dom)(diff)_arb}$
Optional: Differential voltage on extended bus load range	V_{Diff}	$V_{o(dom)(diff)}$
DRIVER SYMMETRY		
Driver symmetry	V_{SYM}	$V_{o(dom)(sym)}$
DRIVER OUTPUT CURRENT		
Absolute current on CAN_H	I_{CAN_H}	$I_{o(SC)(CANH)}$
Absolute current on CAN_L	I_{CAN_L}	$I_{o(SC)(CANL)}$
RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING ACTIVE		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(rec)(CANH)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(rec)(CANL)}$
Differential output voltage	V_{Diff}	$V_{o(rec)(diff)}$
RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING INACTIVE		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(off)(CANH)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(off)(CANL)}$
Differential output voltage	V_{Diff}	$V_{o(off)(dif)}$
OPTIONAL TRANSMIT DOMINANT TIMEOUT		
Transmit dominant timeout, long	t_{dom}	$t_{dom(TxDC)}$
Transmit dominant timeout, short	t_{dom}	NA
STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING ACTIVE		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)_NORM}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)_NORM}$
STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING INACTIVE		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)_WU}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)_WU}$
RECEIVER INPUT RESISTANCE		
Differential internal resistance	R_{Diff}	$R_{i(diff)}$
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	$R_{i(cm)(CANH)}$ $R_{i(cm)(CANL)}$
RECEIVER INPUT RESISTANCE MATCHING		
Matching a of internal resistance	m_R	$R_{i(cm)(m)}$
IMPLEMENTATION LOOP DELAY REQUIREMENT		
Loop delay	t_{Loop}	t_{pd_rd} t_{pd_dr}
OPTIONAL IMPLEMENTATION DATA SIGNAL TIMING REQUIREMENTS for use with bit rates above 1 Mbit/s and up to 2 Mbit/s		
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Received recessive bit width @ 2 Mbit/s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$
Receiver timing symmetry @ 2 Mbit/s	Δt_{Rec}	Δt_{Rec}

Table 8. ISO11898−2:2016 PARAMETER CROSS−REFERENCE TABLE

ISO 11898−2:2016 Specification		NCV7450 Datasheet
Parameter	**Notation**	**Symbol**
OPTIONAL IMPLEMENTATION DATA SIGNAL TIMING REQUIREMENTS for use with bit rates above 2 Mbit/s and up to 5 Mbit/s		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{Bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit / s	$t_{Bit(RXD)}$	$t_{Bit(RxD)}$
Received recessive bit width @ 5 Mbit / s	Δt_{Rec}	Δt_{Rec}
MAXIMUM RATINGS OF V_{CAN_H}, V_{CAN_L} AND V_{DIFF}		
Maximum rating V_{Diff}	V_{Diff}	Vmax_diff
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CANH} V_{CANL}
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA
MAXIMUM LEAKAGE CURRENTS ON CAN_H AND CAN_L, UNPOWERED		
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	I_{LI}
BUS BIASING CONTROL TIMINGS		
CAN activity filter time, long	t_{Filter}	NA
CAN activity filter time, short	t_{Filter}	t_{wake_filt}
Optional: Wake−up timeout, short	t_{Wake}	t_{wake_to}
Optional: Wake−up timeout, long	t_{Wake}	t_{wake_to}
Timeout for bus inactivity (Required for selective wake−up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake−up implementation only)	t_{Bias}	NA

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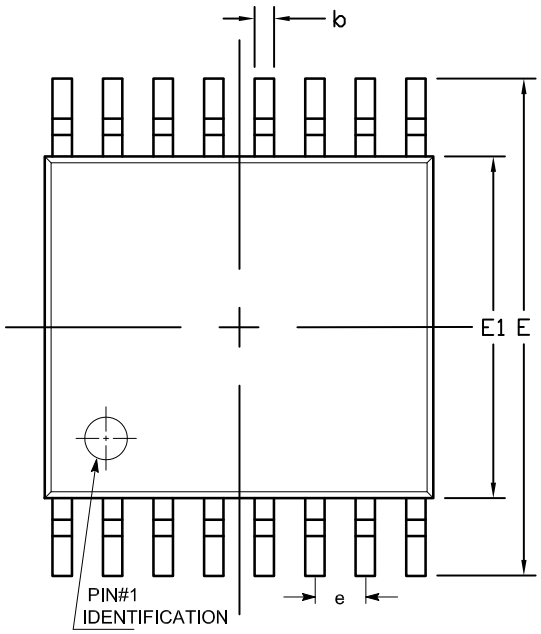
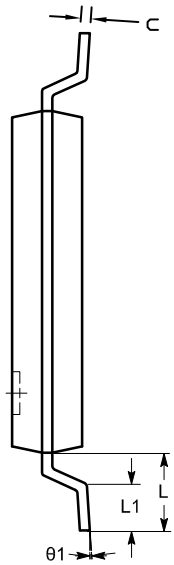


TOP VIEW



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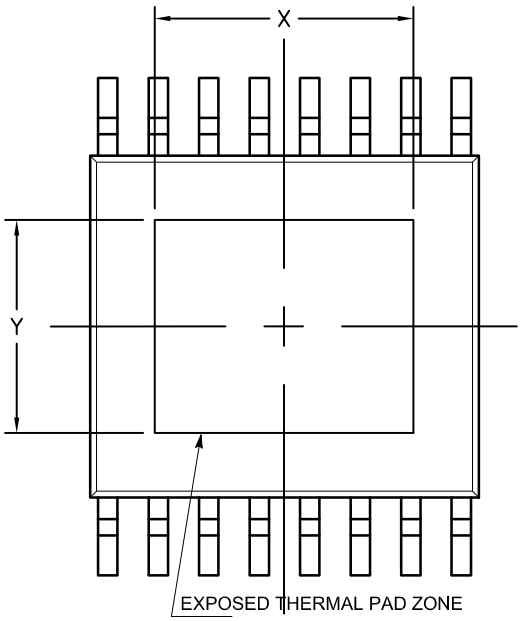
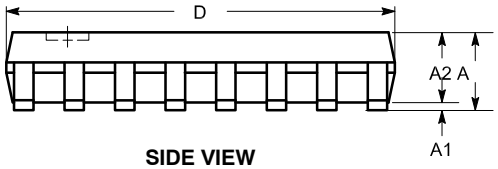
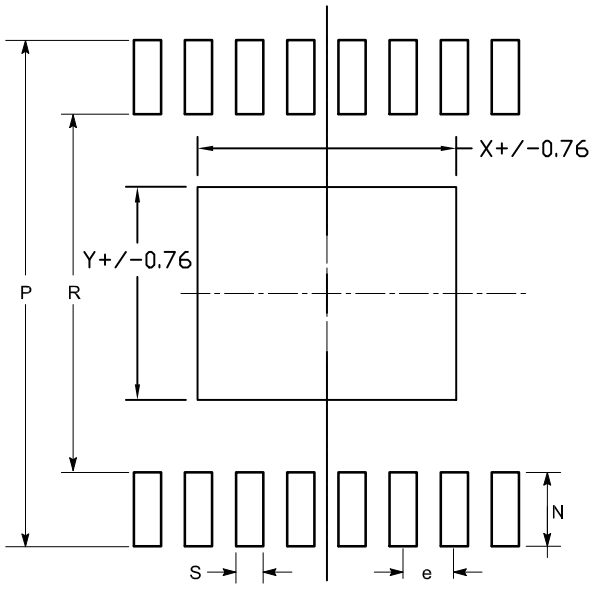


BOTTOM VIEW



SIDE VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.45		0.75
N	0.90		1.00
P	6.50		6.70
R	4.60		4.80
S	0.37		0.47
θ	0º		8º
X		3.33 REF	
Y		2.76 REF	



LAND PATTERN

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153 variations ABT.

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