NCV7703B

Triple Half-Bridge Driver with SPI Control

The NCV7703B is a fully protected Triple Half−Bridge Driver designed specifically for automotive and industrial motion control applications. The three half−bridge drivers have independent control. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states. The drivers are controlled via a standard Serial Peripheral Interface (SPI). This device is fully compatible with ON Semiconductor's NCV7708 Double Hex Driver.

Features

- Ultra Low Quiescent Current in Sleep Mode, 1 μA for V_S and V_{CC}
- Power Supply Voltage Operation down to 5 V
- 3 High−Side and 3 Low−Side Drivers Connected as Half−Bridges
- Internal Free−Wheeling Diodes
- Configurable as H−Bridge Drivers
- 0.5 A Continuous (1 A peak) Current
- $R_{DS(on)}$ = 0.8 Ω (typ)
- 5 MHz SPI Control with Daisy Chain Capability
- Compliance with 5 V and 3.3 V Systems
- Overvoltage and Undervoltage Lockout
- Fault Reporting
- 1.4 A Overcurrent Threshold Detection with Optional Shutdown
- 3 A Current Limit with Auto Shutdown
- Overtemperature Warning and Protection Levels
- Internally Fused Leads in SOIC−14 Package for Better Thermal Performance
- ESD Protection up to 6 kV
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management

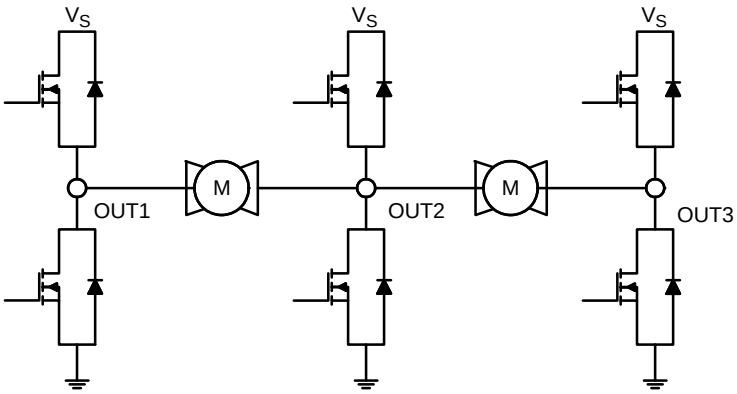
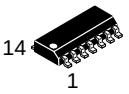


Figure 1. Cascaded Application

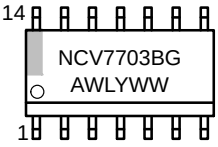
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MARKING DIAGRAM

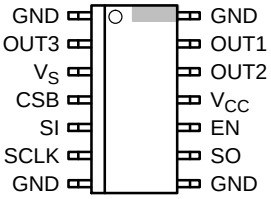


SOIC−14
D2 SUFFIX
CASE 751A



NCV7703B = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV7703BD2G	SOIC−14 (Pb−Free)	55 Units / Rail
NCV7703BD2R2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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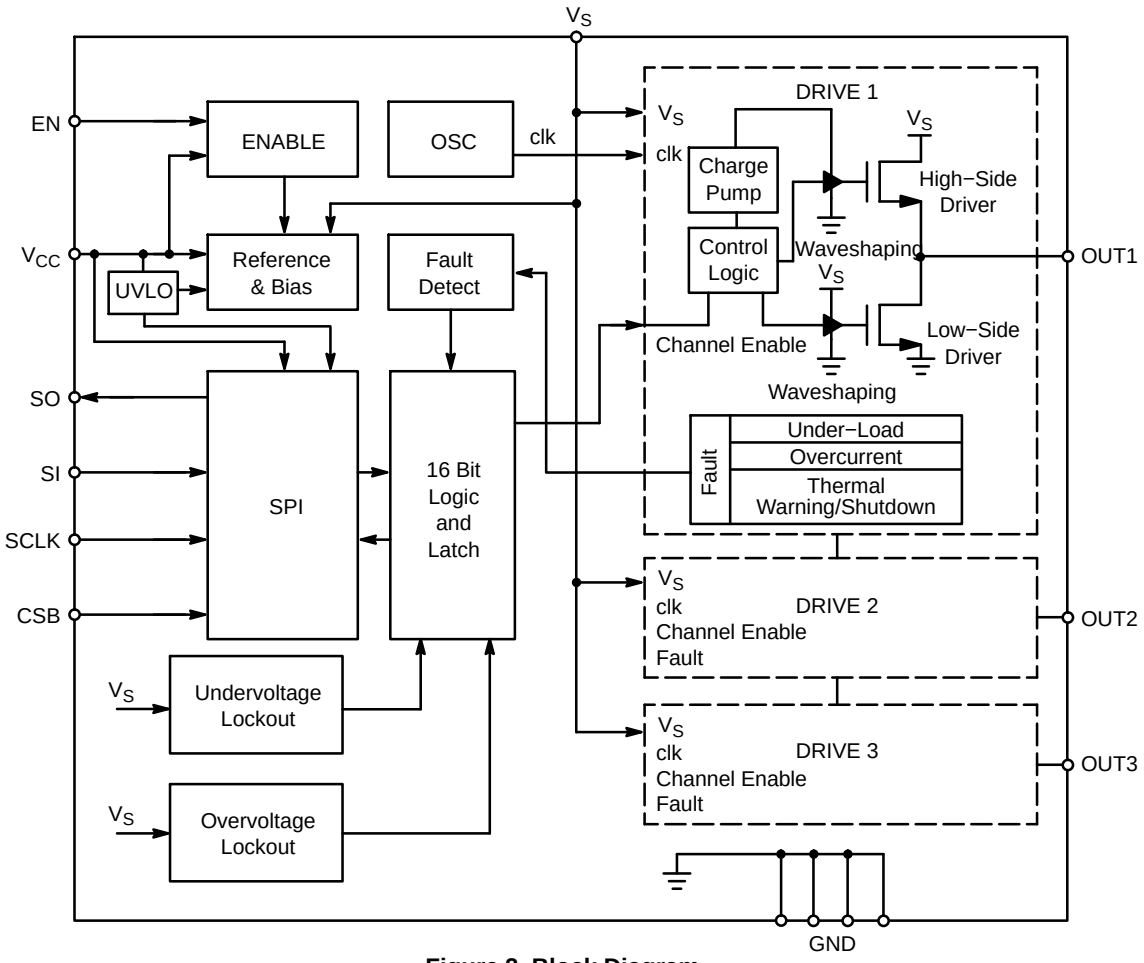
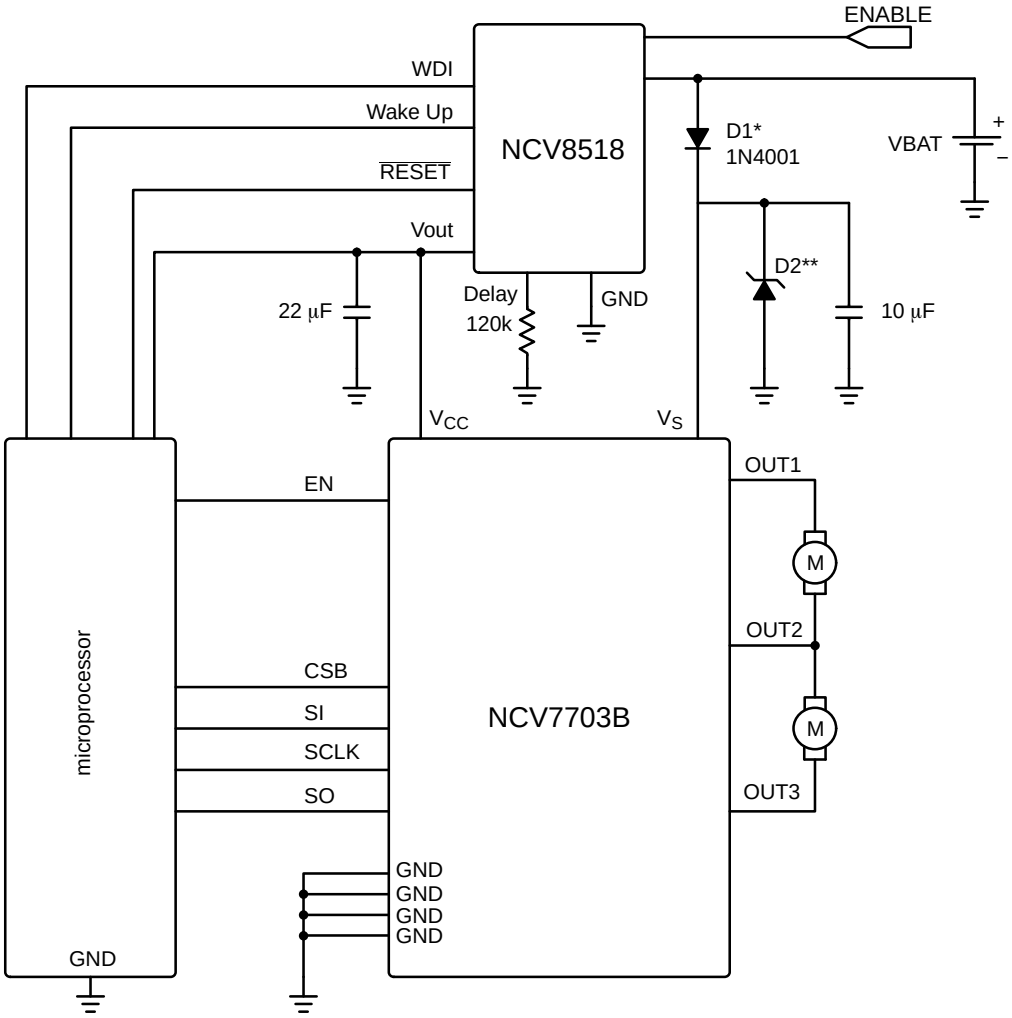


Figure 2. Block Diagram

PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	GND*	Ground. Connect all grounds together.
2	OUT3	Half Bridge Output 3.
3	V_S	Power Supply input for the output drivers and internal supply voltage.
4	CSB	Chip Select Bar. Active low serial port operation.
5	SI	Serial Input
6	SCLK	Serial Clock
7	GND*	Ground. Connect all grounds together.
8	GND*	Ground. Connect all grounds together.
9	SO	Serial Output
10	EN	Enable. Logic high wakes the IC up from a sleep mode.
11	V_{CC}	Power supply input for internal logic.
12	OUT2	Half Bridge Output 2.
13	OUT1	Half Bridge Output 1.
14	GND*	Ground. Connect all grounds together.

*Pins 1, 7, 8, and 14 are internally shorted together. It is recommended to also short these pins externally.



* D1 optional. For use where reverse battery protection is required.
** D2 optional. For use where load dump exceeds 40V.

Figure 3. Application Circuit

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage (V_S) (DC) (AC), t < 500 ms, Ivs > −2 A	 −0.3 to 40 −1	V
Output Pin OUTx (DC) (AC), t < 500 ms, IOUTx > −2 A	 −0.3 to 40 −1	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	−0.3 to 7	V
Output Current (OUTx) (DC) (AC) (50 ms pulse, 1 s period)	 −1.8 to 1.8 Internally Limited	A
Electrostatic Discharge, Human Body Model, V_S, OUT1, OUT2, OUT3 (Note 3)	6	kV
Electrostatic Discharge, Human Body Model, all other pins (Note 3)	2	kV
Electrostatic Discharge, Machine Model, V_S, OUT1, OUT2, OUT3 (Note 3)	300	V
Electrostatic Discharge, Machine Model, all other pins (Note 3)	200	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−55 to 150	°C
Moisture Sensitivity Level (MAX 260°C Processing)	MSL3	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Thermal Parameters	Test Conditions (Typical Value)		Unit
14 Pin Fused SOIC Package	min−pad board (Note 1)	1″ pad board (Note 2)	
Junction−to−Lead (psi−JL8, Ψ_{JL8}) or Pins 1, 7, 8, 14	23	22	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	122	83	°C/W

1. 1−oz copper, 67 mm^2 copper area, 0.062″ thick FR4.
2. 1−oz copper, 645 mm^2 copper area, 0.062″ thick FR4.
3. This device series incorporates ESD protection and is characterized by the following methods:
   ESD HBM according to AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM according to AEC−Q100−003 (EIA/JESD22−A115)

ELECTRICAL CHARACTERISTICS

($-40°C \le T_J \le 150°C$, $5.5\ V \le V_S \le 40\ V$, $3\ V \le V_{CC} \le 5.25\ V$, $EN = V_{CC}$, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
GENERAL					
Supply Current (V_S) Sleep Mode (Note 5)	V_S = 13.2 V, OUTx = 0 V EN = SI = SCLK = 0 V, CSB = V_{CC} 0 V < V_{CC} < 5.25 V (T_J = −40°C to 85°C)	−	1.0	5.0	μA
	V_S = 13.2 V, OUTx = 0 V EN = SI = SCLK = 0 V, CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C	−	−	2.0	
Supply Current (V_S) Active Mode	EN = V_{CC}, 5.5 V < V_S < 35 V No Load	−	2.0	4.0	mA
Supply Current (V_{CC}) Sleep Mode (Note 6)	V_{CC} = CSB, EN = SI = SCLK = 0 V (T_J = −40°C to 85°C)	−	0	2.5	μA
Supply Current (V_{CC}) Active Mode	EN = V_{CC}	−	1.5	3.0	mA
V_{CC} Power−On−Reset Threshold		2.60	2.80	3.00	V
V_S Undervoltage Detection Threshold Hysteresis	V_S decreasing	4.3 100	4.7 −	5.1 400	V mV
V_S Overvoltage Detection Threshold Hysteresis	V_S increasing	34.0 1.5	37.5 3.5	40.0 5.5	V
Thermal Warning (Note 4) Threshold Hysteresis		120 −	145 30	170 −	°C
Thermal Shutdown (Note 4) Threshold Hysteresis		155 −	175 30	195 −	°C
Ratio of Thermal Shutdown to Thermal Warning temperature (Note 4)		1.05	1.20	−	°C/°C
OUTPUTS					
Output $R_{DS(on)}$ (Source)	I_{out} = −500 mA				
	V_S = 13.2 V, T_J = 25°C	−	0.8	0.95	Ω
	V_S = 13.2 V	−	−	1.5	Ω
	8 V ≤ V_S ≤ 40 V	−	−	1.7	Ω
	5.5 V ≤ V_S ≤ 8 V, T_J = 25°C	−	1.3	−	Ω
	5.5 V ≤ V_S ≤ 8 V	−	−	2.0	Ω
Output $R_{DS(on)}$ (Sink)	I_{out} = 500 mA				
	V_S = 13.2 V, T_J = 25°C	−	0.8	0.95	Ω
	V_S = 13.2 V	−	−	1.5	Ω
	8 V ≤ V_S ≤ 40 V	−	−	1.7	Ω
	5.5 V ≤ V_S ≤ 8 V, T_J = 25°C	−	1.3	−	Ω
	5.5 V ≤ V_S ≤ 8 V	−	−	2.0	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Thermal characteristics are not subject to production test
5. For temperatures above 85°C, refer to Figure 4.
6. For temperatures above 85°C, refer to Figure 5.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
OUTPUTS					
Source Leakage Current Sum of I(OUTx) x = 1, 2, 3	OUTx = 0 V, V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V Sum(I(OUTx) OUTx = 0 V, V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C Sum(I(OUTx)	−5.0 −1.0	− −	− −	μA
Sink Leakage Current	OUTx = V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V OUTx = V_S = 13.2 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C	− −	− −	300 10	μA
Over Current Shutdown Threshold Source Sink		−1.8 1.0	−1.4 1.4	−1.0 1.8	A
Current Limit Source Sink		−5.0 2.0	−3.0 3.0	−2.0 5.0	A
Under Load Detection Threshold Source Sink		−15 3.0	−7.0 7.0	−2.0 15	mA
Power Transistor Body Diode Forward Voltage	I_f = 500 mA	−	0.9	1.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Thermal characteristics are not subject to production test
5. For temperatures above 85°C, refer to Figure 4.
6. For temperatures above 85°C, refer to Figure 5.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS (EN, SI, SCLK, CSB)					
Input Threshold High Low		 – 30	 – –	 70 –	%V_{CC}
Input Hysteresis		100	350	600	mV
Input Pulldown Current (EN, SI, SCLK)	EN = SI = SCLK = V_{CC}	5.0	25	50	μA
Input Pullup Current (CSB)	CSB = 0 V	−50	−25	−5	μA
Input Capacitance (Note 7)		–	10	15	pF
LOGIC OUTPUT (SO)					
Output High	I_{out} = 1 mA	V_{CC} – 1.0	V_{CC} – 0.7	–	V
Output Low	I_{out} = −1.6 mA	–	0.2	0.4	V
Tri−state Leakage	CSB = V_{CC}, 0 V ≤ SO ≤ V_{CC}	−10	–	10	μA
Tri−state Input Capacitance (Note 7)	CSB = V_{CC}	–	10	15	pF
TIMING SPECIFICATIONS					
Overcurrent Shutdown Delay Time Source Sink		 10 10	 25 25	 50 50	μs
Current Limit Fault Delay	V_S > 8 V	–	200	–	μs
Under Load Detection Delay Time		200	350	600	μs
High Side Turn On Time	V_S = 13.2 V, R_{load} = 25 Ω	–	7.5	15	μs
High Side Turn Off Time	V_S = 13.2 V, R_{load} = 25 Ω	–	3.0	6.0	μs
Low Side Turn On Time	V_S = 13.2 V, R_{load} = 25 Ω	–	6.5	15	μs
Low Side Turn Off Time	V_S = 13.2 V, R_{load} = 25 Ω	–	3.0	6.0	μs
High Side Rise Time	V_S = 13.2 V, R_{load} = 25 Ω	–	5.0	10	μs
High Side Fall Time	V_S = 13.2 V, R_{load} = 25 Ω	–	2.0	5.0	μs
Low Side Rise Time	V_S = 13.2 V, R_{load} = 25 Ω	–	1.0	3.0	μs
Low Side Fall Time	V_S = 13.2 V, R_{load} = 25 Ω	–	1.0	3.0	μs
NonOverlap Time	High Side Turn Off to Low Side Turn On	1.0	–	–	μs
NonOverlap Time	Low Side Turn Off to High Side Turn On	1.0	–	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Not production tested.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

SERIAL PERIPHERAL INTERFACE

Characteristic	Conditions	Timing Chart # (See Figure 8)	Min	Typ	Max	Unit
SCLK Frequency	V_{CC} = 5 V	−	−	−	5	MHz
SCLK Clock Period	V_{CC} = 5 V V_{CC} = 3.3 V	− −	200 500	− −	− −	ns
Maximum Input Capacitance (Note 8)	SI, SCLK	−	−	−	15	pF
SCLK High Time		1	85	−	−	ns
SCLK Low Time		2	85	−	−	ns
SCLK Setup Time		3 4	85 85	− −	− −	ns
SI Setup Time		11	50	−	−	ns
SI Hold Time		12	50	−	−	ns
CSB Setup Time		5 6	100 100	− −	− −	ns
CSB High Time (Note 9)		7	200	−	−	ns
SO enable after CSB falling edge (Note 8)		8	−	−	50	ns
SO disable after CSB rising edge (Note 8)		9	−	−	50	ns
SO Rise Time	V_{CC} = 5 V, C_{load} = 40 pF	−	−	10	25	ns
SO Fall Time	V_{CC} = 5 V, C_{load} = 40 pF	−	−	10	25	ns
SO Valid Time (Note 8)	SCLK ↑ to SO 50%	10	−	20	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Not tested in production.
9. Minimum high time of CSB between two successive SPI commands.

TYPICAL CHARACTERISTICS

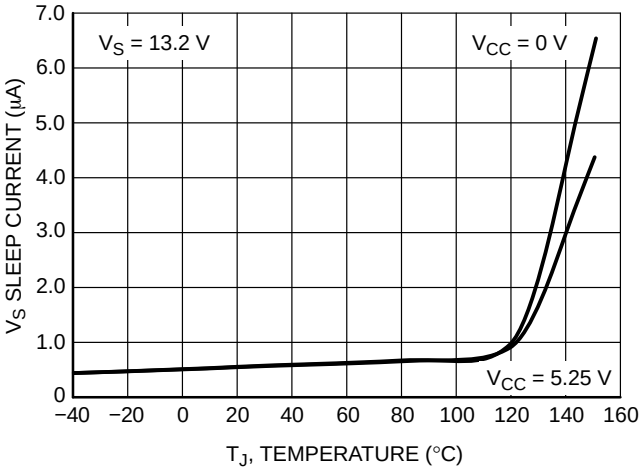


Figure 4. V_S Sleep Supply Current vs. Temperature

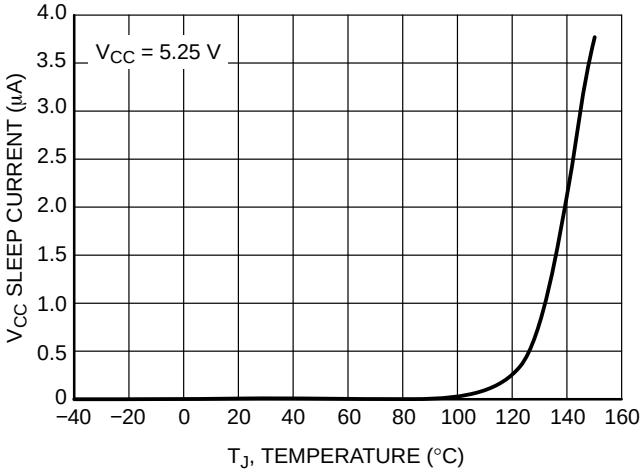


Figure 5. V_{CC} Sleep Supply Current vs. Temperature

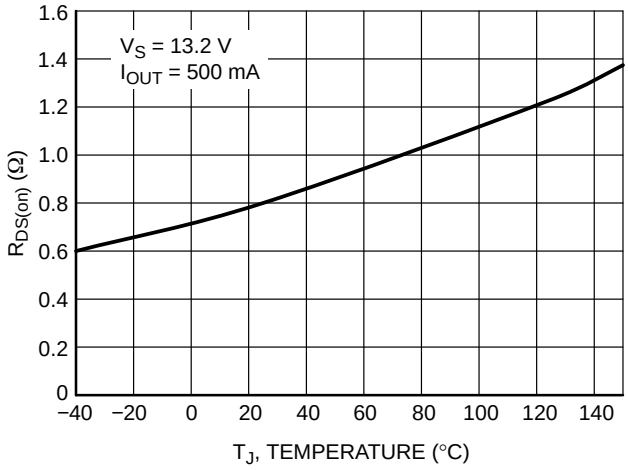


Figure 6. (Source / Sink) $R_{DS(on)}$ vs. Temperature

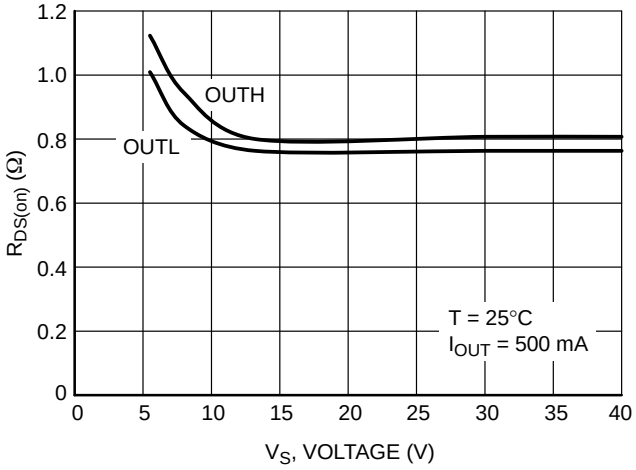


Figure 7. $R_{DS(on)}$ vs. V_S

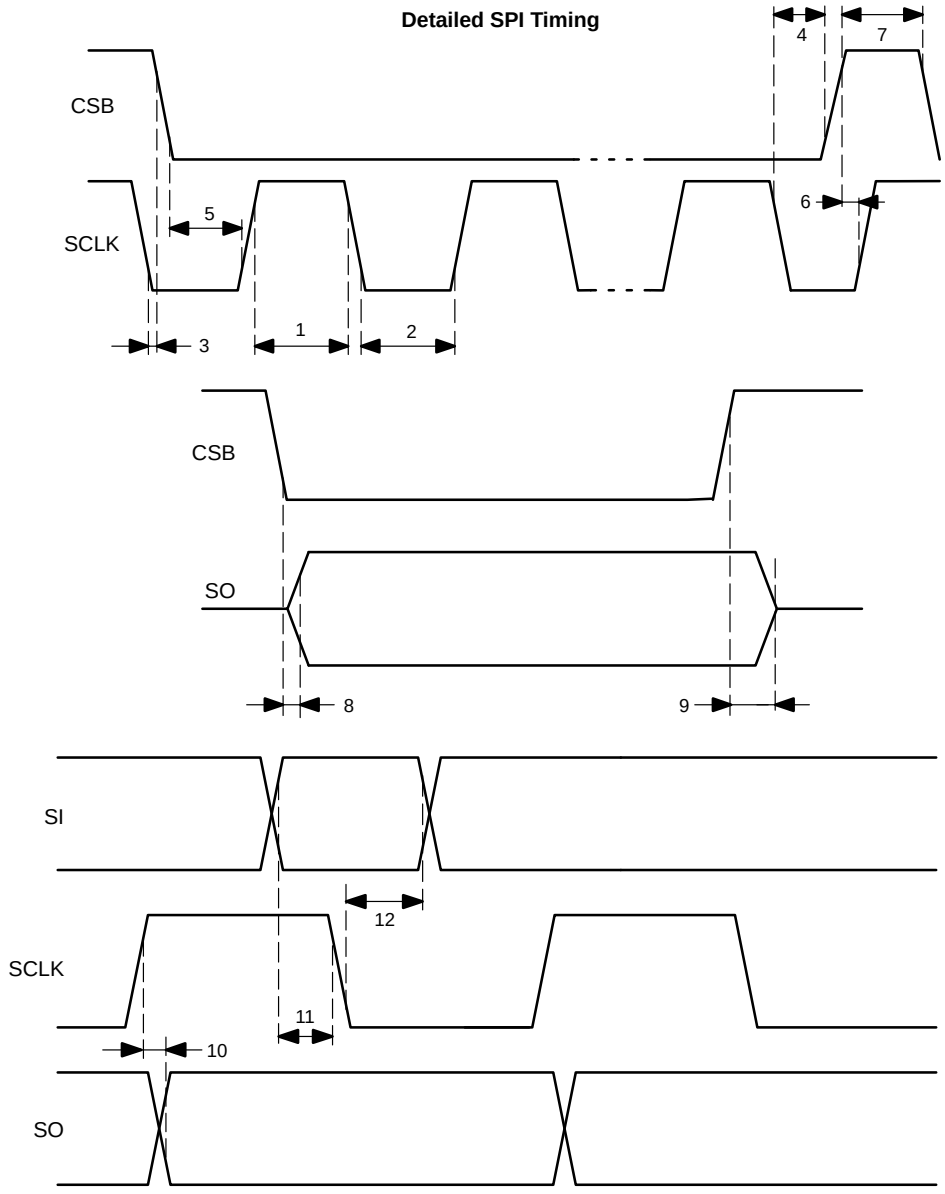


Figure 8. SPI Timing Waveforms

TYPICAL CHARACTERISTICS

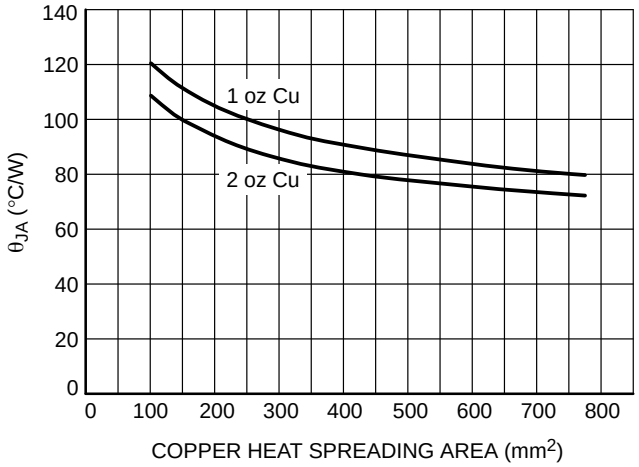


Figure 9. θ_{JA} vs. Copper Spreader Area, 14 Lead SON (fused leads)

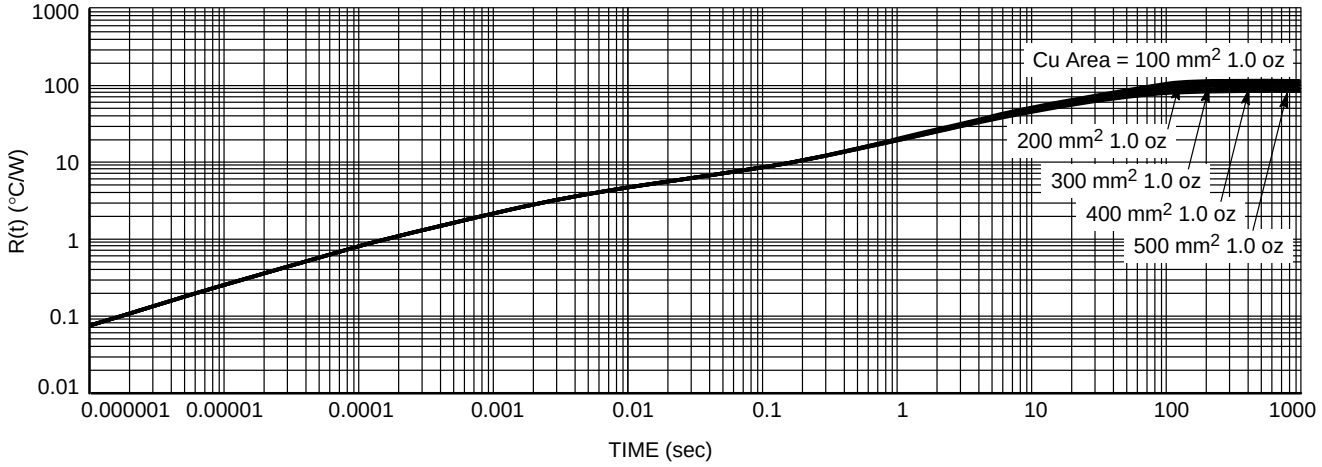


Figure 10. Transient Thermal Response to a Single Pulse 1 oz Copper (Log−Log)

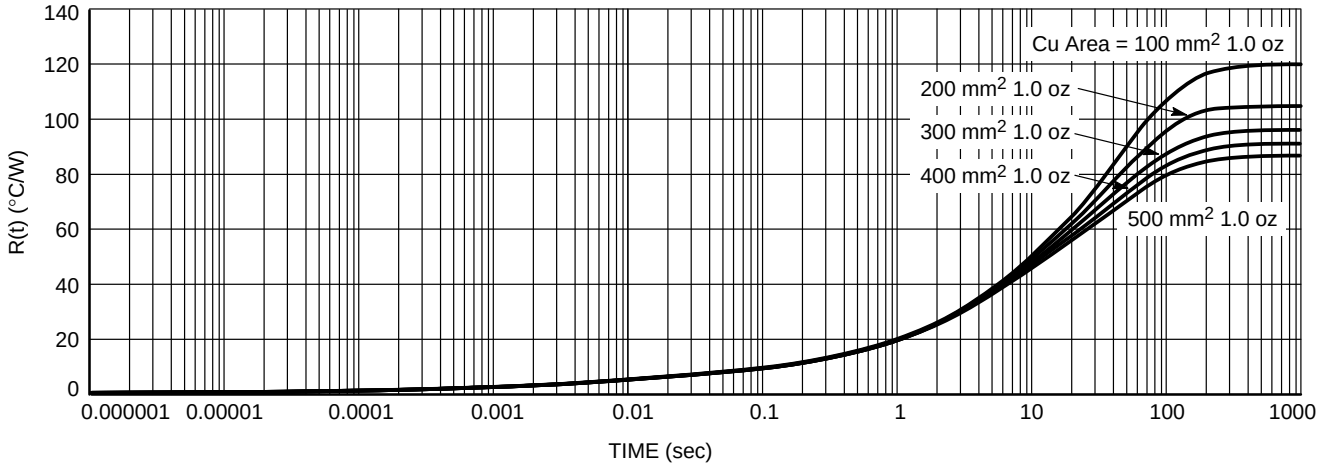


Figure 11. Transient Thermal Response to a Single Pulse 1 oz Copper (Semi−Log)

SPI Communication

Standard 16−bit communication has been implemented to this IC to turn drivers on/off, and to report faults. (See Figure 13). The LSB (Least Significant Bit) is clocked in first.

Communication is Implemented as Follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (Serial Input) pin.
3. CSB goes high to transfer the clocked in information to the data registers.

NOTE: SO is tristate when CSB is high.

Frame Detection

Input word integrity (SI) is evaluated by the use of a frame consistency check. The word frame length is compared to an η x 16 bit acceptable word length before the data is latched into the input register. This guarantees the proper word length has been imported and allows for daisy chain operation applications.

The frame length detector is enabled with the CSB falling edge and the SCLK rising edge.

SCLK must be low during the CSB rising edge. The fault register is cleared with a valid frame detection. Existing faults are re−latched after the fault filter time.

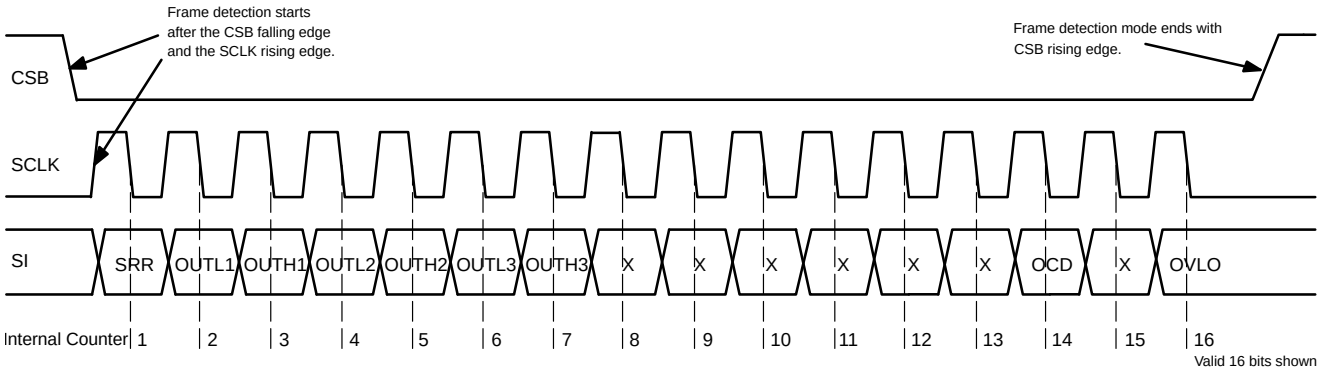


Figure 12. Frame Detection

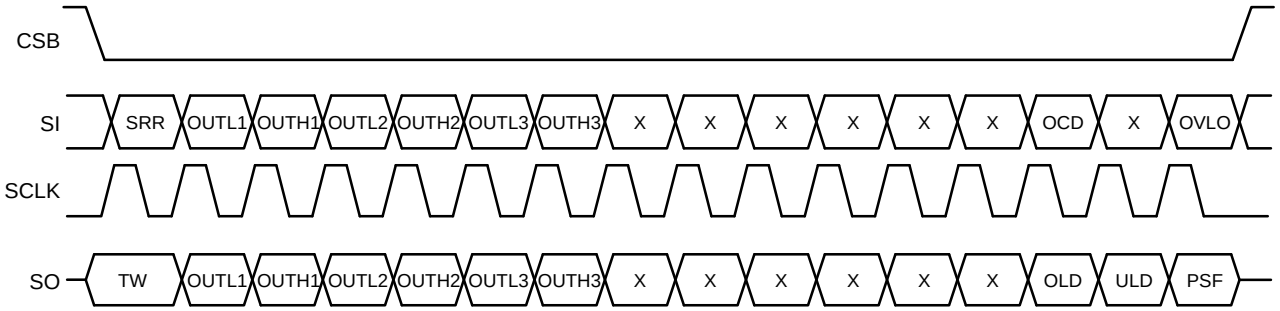


Figure 13. SPI Communication Frame Format

Table 1 defines the programming bits and diagnostic bits. Figure 13 displays the timing diagram associated with Table 1. Fault information is sequentially clocked out the SO pin of the NCV7703B as programming information is clocked into the SI pin of the device. Daisy chain communication between SPI compatible IC's is possible by connection of the Serial Output pin (SO) to the input of the sequential IC (SI) (Reference the Daisy Chain Section).

Table 1. SPI BIT DESCRIPTION

Input Data			Output Data		
Bit Number	**Bit Description**	**Bit Status**	**Bit Number**	**Bit Description**	**Bit Status**
15	Over Voltage Lock Out Control (OVLO)	0 = Disable	15	Power Supply Fail Signal (PSF for OVLO or UVLO)	0 = No Fault
		1 = Enable			1 = Fault
14	Not Used		14	Under Load Detect Signal (ULD)	0 = No Fault
					1 = Fault
13	Over Current Detection Shut Down Control (OCD)	0 = Disable	13	Over Load Detect Signal (OLD)	0 = No Fault
		1 = Enable			1 = Fault
12	Not Used		12	Not Used	
11	Not Used		11	Not Used	
10	Not Used		10	Not Used	
9	Not Used		9	Not Used	
8	Not Used		8	Not Used	
7	Not Used		7	Not Used	
6	OUTH3	0 = Off	6	OUTH3	0 = Off
		1 = On			1 = On
5	OUTL3	0 = Off	5	OUTL3	0 = Off
		1 = On			1 = On
4	OUTH2	0 = Off	4	OUTH2	0 = Off
		1 = On			1 = On
3	OUTL2	0 = Off	3	OUTL2	0 = Off
		1 = On			1 = On
2	OUTH1	0 = Off	2	OUTH1	0 = Off
		1 = On			1 = On
1	OUTL1	0 = Off	1	OUTL1	0 = Off
		1 = On			1 = On
0	Status Register Reset (SRR)	0 = No Reset	0	Thermal Warning (TW)	0 = Not in TW
		1 = Reset			1 = In TW

DETAILED OPERATING DESCRIPTION

General

The NCV7703B Triple Half Bridge Driver provides drive capability for 3 Half−Bridge configurations. Each output drive is characterized for a 500 mA load and has a typical 1.4 A surge capability. Strict adherence to integrated circuit die temperature is necessary, with a maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the EN, SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Power Up/Down Control

A feature incorporated in the IC is an under voltage lockout circuit that prevents the output drivers from turning on unintentionally. V_{CC} and V_S are monitored for undervoltage conditions supporting a smooth turn−on transition. All drivers are initialized in the off (high impedance) condition, and will remain off during a V_{CC} or V_S undervoltage condition. This allows power up sequencing of V_{CC}, and V_S up to the user. Once V_{CC} is out of UVLO, SPI communication can begin regardless of the voltage on V_S. However, drivers will remain off if V_S is in an undervoltage condition. Hysteresis in the UVLO circuits results in glitch free operation during power up/down.

H−Bridge Driver Configuration

The NCV7703B has the flexibility of controlling each half bridge driver independently. This allows for high side, low side and H−bridge control. H−bridge control provides forward, reverse, brake and high impedance states.

Overvoltage Clamping − Driving Inductive Loads

Each output is internally clamped to ground and Vs by internal free wheeling diodes. The diodes have ratings that complement the FETs they protect.

Overcurrent Shutdown Threshold Detection (Table 2)

The state of input bit 13 (OCD) selects driver reaction when reaching overcurrent shutdown threshold. With a “0” for input bit 13, the OLD status bit will be set to “1” when the level exceeds the overcurrent shutdown shut−down threshold and the driver will remain on. With a “1” for input bit 13, the output driver shuts off when the overcurrent shutdown threshold is exceeded and can only be turned back on via the SPI port with a SPI command that includes an SRR = 1. Note: high currents could cause a high rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

Current Limit Fault

The current limit fault circuit will shut down the offending output driver when the Current Limit (Source or Sink) has been exceeded for a duration greater than 200 μs, regardless of the OLD input bit status. The OUTx output bit will report a “0” indicating which driver encountered the hard short. The OLD status bit will be set and will remain set until a new SRR input SPI command is executed.

Under−Load Detection (Table 3)

The under−load detection circuit monitors the current from each output driver. A minimum load current (this is the maximum open circuit detection threshold) is required when the drivers are turned on. If the under−load detection threshold has been detected for more than the under−load delay time, the ULD bit (output bit #14) will be set to a “1”. The under load bit is reset with SRR.

Overvoltage Shutdown (Table 4)

Overvoltage lockout circuitry monitors the voltage on the V_S pin. The response to an overvoltage condition is selected by SPI input bit 15. PSF output bit 15 is set when a V_S overvoltage condition exists. If input bit 15 (OVLO) is set to “1”, all outputs will turn off during this overvoltage condition. Turn On/Off status is maintained in the logic circuitry, so that when proper input voltage level is reestablished, the programmed outputs will turn back on. The PSF output bit is reset with SRR.

Table 2. INPUT BIT 13, OVERCURRENT DETECTION SHUT DOWN CONTROL AND RESPONSE

OLD Input Bit 13 Set	Typical Load Current Condition	Output Bit 13 OLD Status	OUTx Status
0	$I_L \le 1.4$ A	0	Unchanged
0	1.4 A < $I_L \le 3$ A	1 (Need SRR to reset)	Unchanged
0	$I_L \ge 3$ A, for 200 μs (typ)	1 (Need SRR to reset)	OUTx Latched Off (Need SRR to reset)
1	$I_L \le 1.4$ A	0	Unchanged
1	I_L > 1.4 A, for 25 μs (typ)	1 (Need SRR to reset)	OUTx Latched Off (Need SRR to reset)

Table 3. OUTPUT BIT 14, UNDER LOAD DETECTION SHUT DOWN

OUTx ULD Set	Output Data Bit 14, Under Load Detect (ULD) Status	OUTx Status
0	0	Unchanged
1	1 (Need SRR to reset)	Unchanged

Table 4. INPUT BIT 15, OVERVOLTAGE LOCK OUT (OVLO) SHUT DOWN

OVLO Input Bit 15	V_S OVLO Condition	Output Data Bit 15 Power Supply Fail (PSF) Status	OUTx Status
0	0	0	Unchanged
0	1	1 (Need SRR to reset)	Unchanged
1	0	0	Unchanged
1	1	1 (Need SRR to reset)	All Outputs Shut Off (Remain off until V_S is out of OVLO)

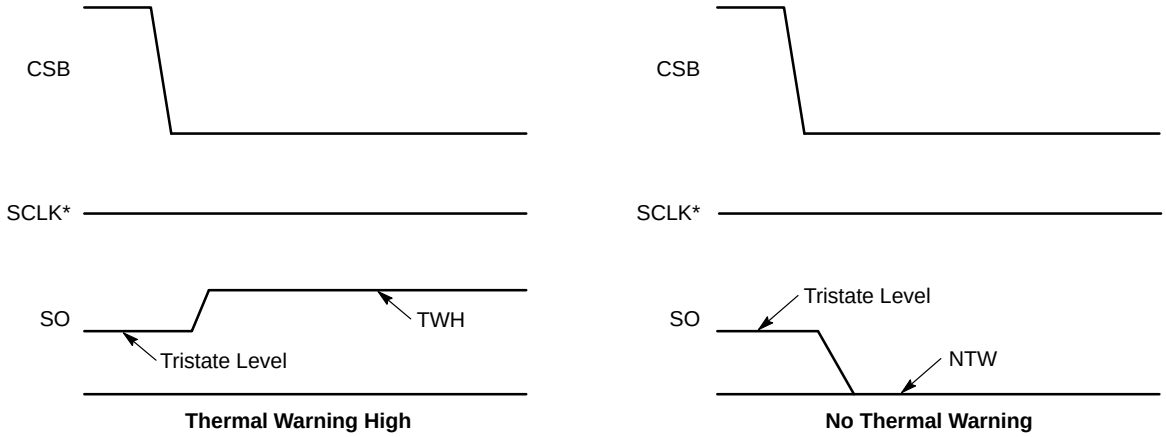
Thermal Shutdown

Three independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two temperature levels; Level 1, Thermal Warning sets the “TW” status bit to a 1 and would have to be reset with a command that includes the SRR after the IC cools to a temperature below Level 1. The output will remain on in this condition.

If the IC temperature reaches Level 2, Over Temperature Shutdown, all drivers are latched off. It can be reset only after the part cools below the shutdown temperature, (including thermal hysteresis) with a turn−on command that includes the SRR set bit.

The output data bit 0, Thermal Warning, will latch and remain set, even after cooling, and is reset by sending a SPI command to reset the status register (SRR, input 0 set to “1”). Since thermal warning precedes a thermal shutdown, software polling of this bit will allow for load control and possible prevention of thermal shutdown conditions.

Thermal warning information can be retrieved immediately without performing a complete SPI access cycle. Figure 14 below displays how this is accomplished. Bringing the CSB pin from a high to low condition immediately displays the information on the Output Data Bit 0, thermal warning, even in the absence of an SCLK signal. As the temperature of the NCV7703B changes from a condition from below the thermal warning threshold to above the thermal warning threshold, the state of the SO pin changes and this level is available immediately when the CSB goes low. A low on SO indicates there is no thermal warning, while a high indicates the IC is above the thermal warning threshold. This warning bit is reset by setting SRR to “1”.



*SCLK can be high or low in order to maintain the thermal information on SO. Toggling SCLK will cause other output bits to shift out.
TWH = Thermal Warning High
NTW = No Thermal Warning

Figure 14. Access to Temperature Warning Information

Applications Drawing

Daisy Chain

The NCV7703B is capable of being setup in a daisy chain configuration with other similar devices which include additional NCV7703B devices as well as the NCV7708 Double Hex Driver. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be the Diagnostic Output Data. These are the bits representing the status of the IC and are detailed in the SPI Bit Description Table. Additional programming bits should be clocked in which follow the Diagnostic Output bits. Word length must be η x 16 due to the use of frame detection.

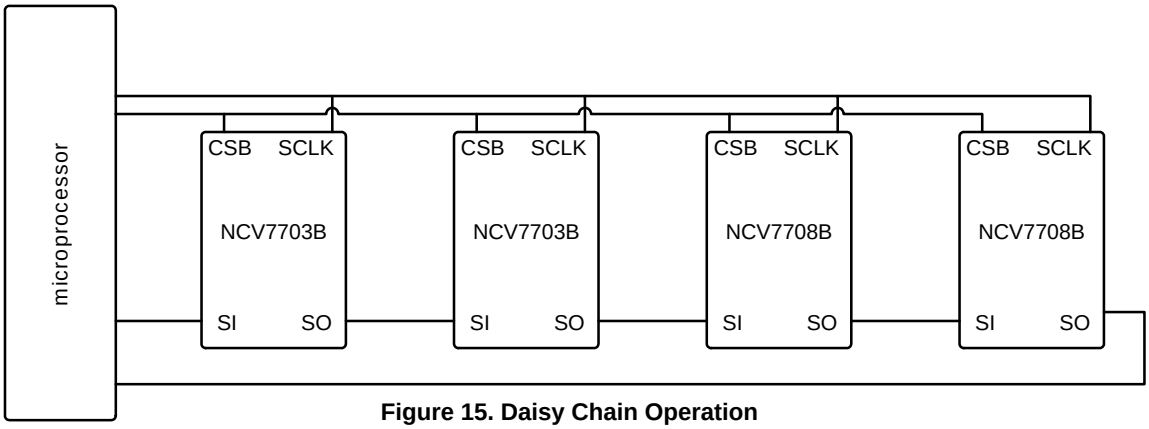


Figure 15. Daisy Chain Operation

Parallel Control

A more efficient way to control multiple SPI compatible devices is to connect them in a parallel fashion and allow each device to be controlled in a multiplex mode. The diagram below shows a typical connection between the microprocessor or microcontroller and multiple SPI compatible devices. In a daisy chain configuration, the programming information for the last device in the serial string must first pass through all the previous devices. The parallel control setup eliminates that requirement, but at the cost of additional control pins from the microprocessor for each individual CSB pin for each controllable device. Serial data is only recognized by the device that is activated through its respective CSB pin.

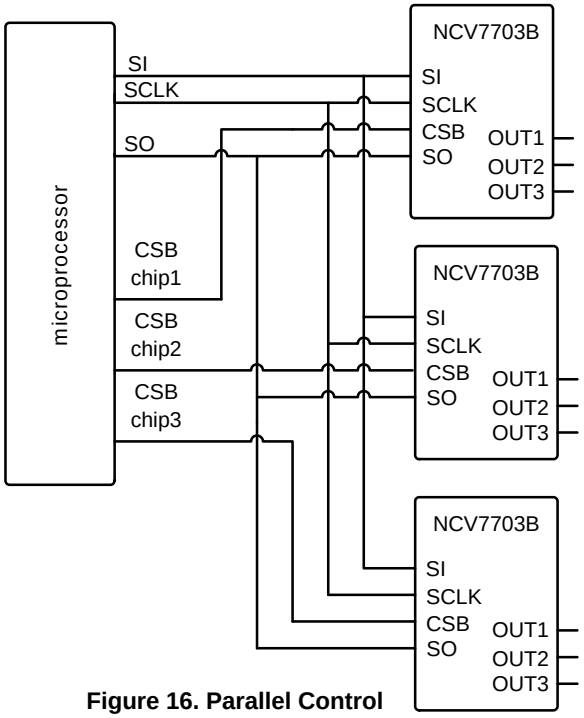


Figure 16. Parallel Control

Additional Application Setup

In addition to the cascaded H−Bridge application shown in Figure 1, the NCV7703B can also be used as a high−side driver or low−side driver (Figure 17).

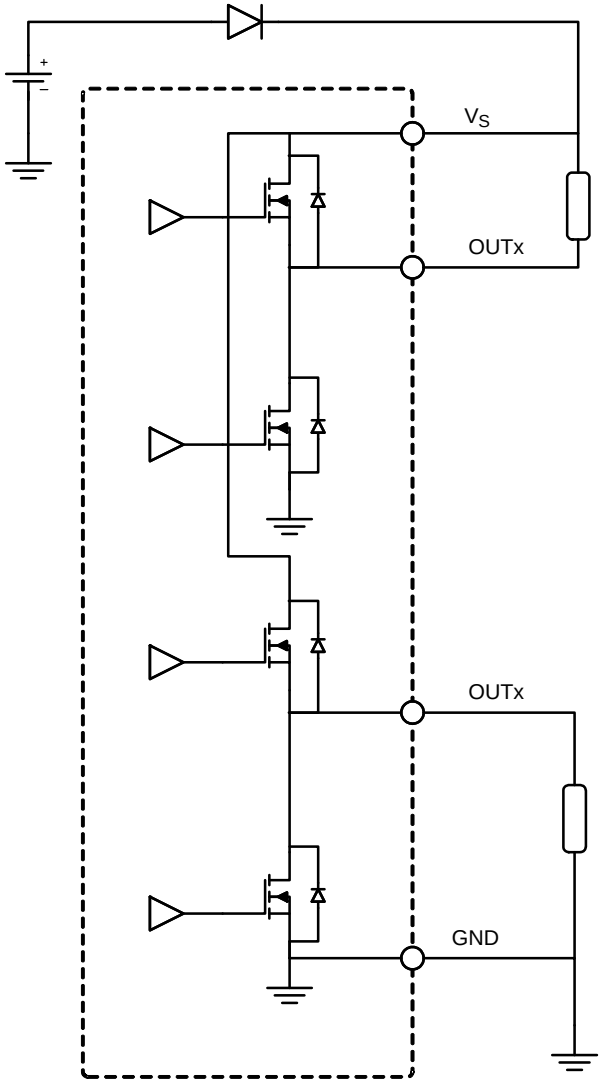
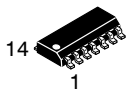


Figure 17. High−Side / Low−Side Application Drawing

Any combination of H−bridge and high or low−side drivers can be designed in. This allows for flexibility in many systems.

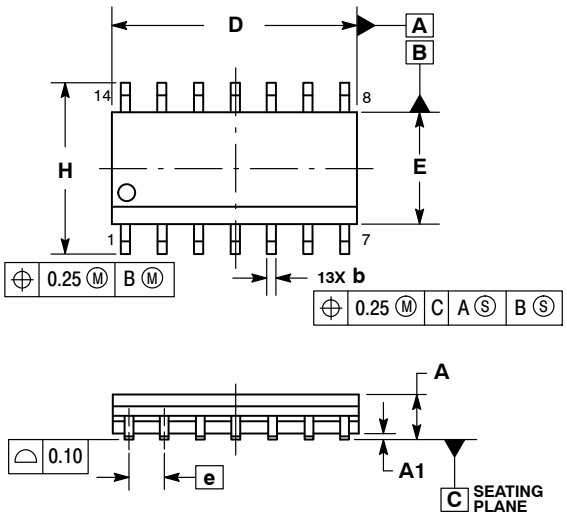
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

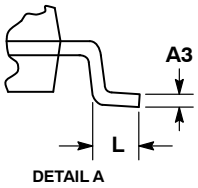


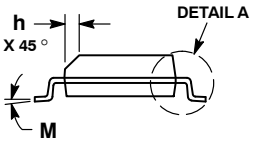
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

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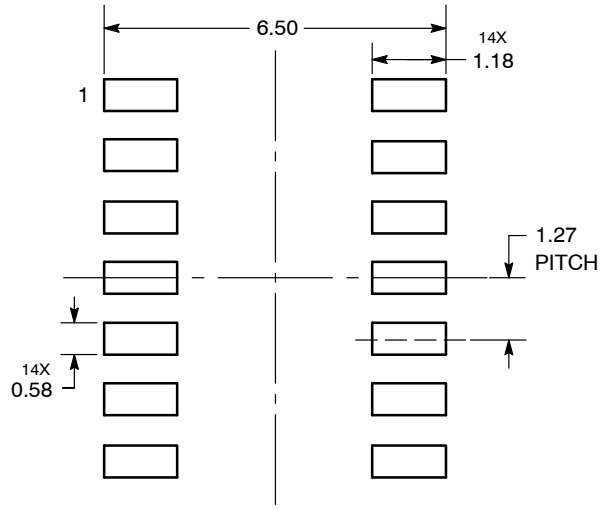




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

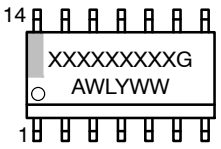
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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