Triple Half-Bridge Driver with SPI Control

NCV7703C

The NCV7703C is a fully protected Triple Half−Bridge Driver designed specifically for automotive and industrial motion control applications. The three half−bridge drivers have independent control. This allows for high side, low side, and H−Bridge control. H−Bridge control provides forward, reverse, brake, and high impedance states (with EN = 0). The drivers are controlled via a standard Serial Peripheral Interface (SPI).

Features

- Ultra Low Quiescent Current in Sleep Mode, 1 μA for V_S and V_{CC}
- 3 High−Side and 3 Low−Side Drivers Connected as Half−Bridges
- Internal Free−Wheeling Diodes
- Configurable as H−Bridge Drivers
- 500 mA (typ), 1.1 A (max) Drivers
- $R_{DS(on)}$ = 0.8 Ω (typ), 1.7 Ω (max)
- 5 MHz SPI Control with Daisy Chain Capability
- Compliance with 5 V and 3.3 V Systems
- Overvoltage and Undervoltage Lockout
- Fault Reporting
- 1.45 A Overcurrent Threshold Detection
- 3 A Current Limit
- Shoot−Through Attempt Detection
- Overtemperature Warning and Protection Levels
- Internally Fused Leads in SOIC−14 for Better Thermal Performance
- ESD Protection up to 6 kV
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial
- DC Motor Management

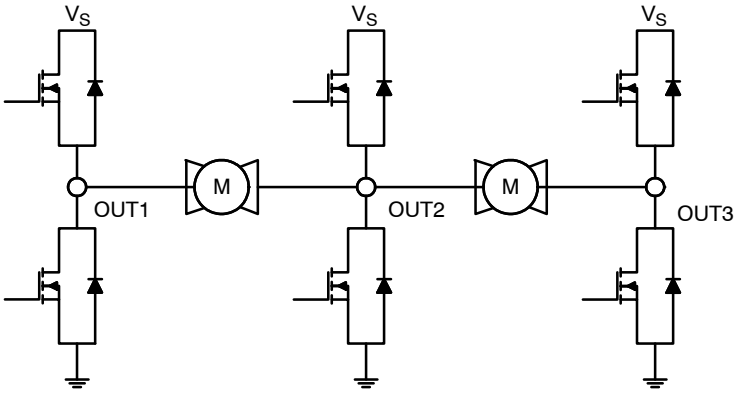
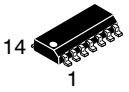


Figure 1. Cascaded Application

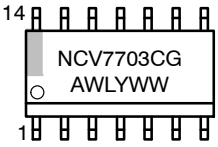
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MARKING DIAGRAM

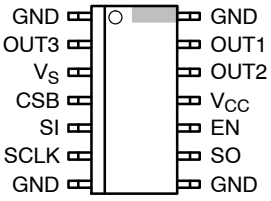


SOIC−14
D2 SUFFIX
CASE 751A



NCV7703C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCV7703CD2R2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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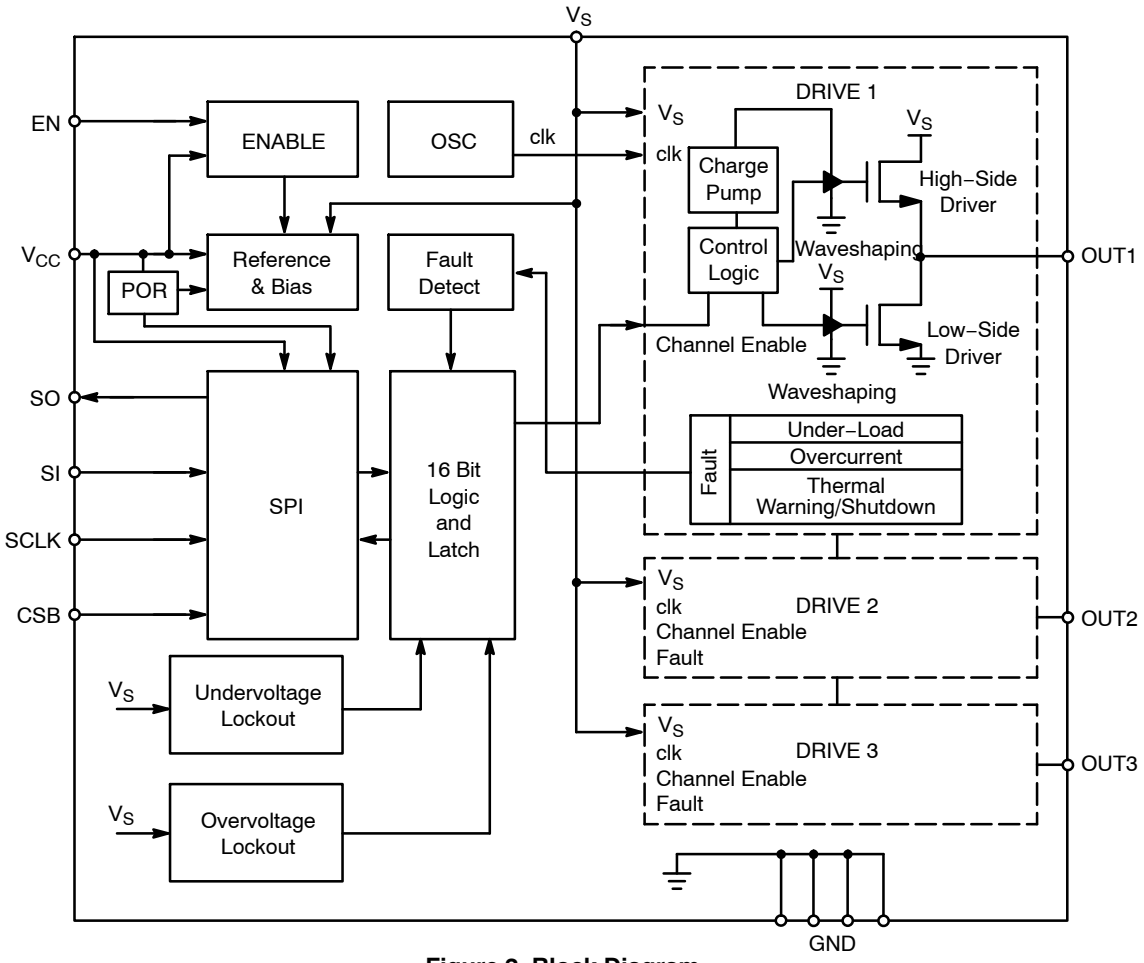
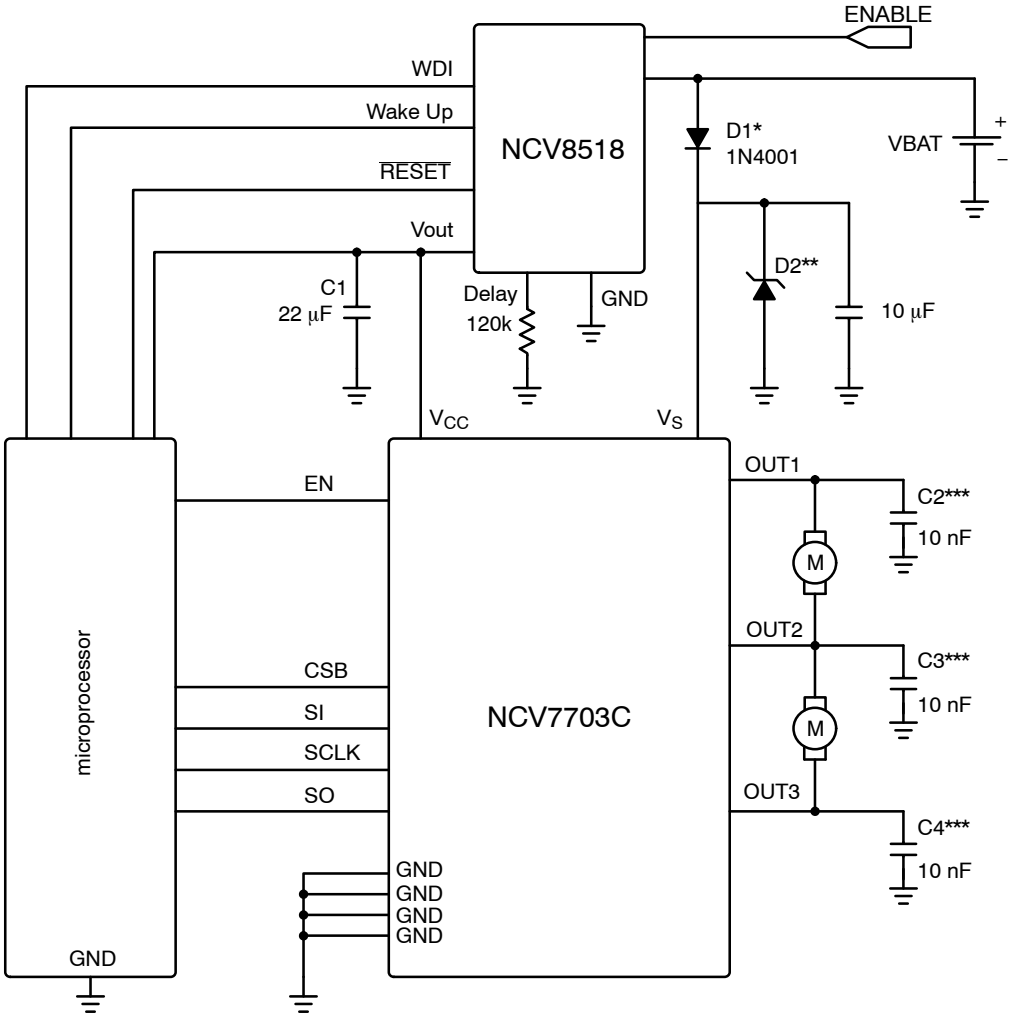


Figure 2. Block Diagram

PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	GND*	Ground. Connect all grounds together.
2	OUT3	Half Bridge Output 3.
3	V_S	Power Supply input for the output drivers and internal supply voltage.
4	CSB	Chip Select Bar. Active low serial port operation.
5	SI	Serial Input
6	SCLK	Serial Clock
7	GND*	Ground. Connect all grounds together.
8	GND*	Ground. Connect all grounds together.
9	SO	Serial Output
10	EN	Enable. Logic high wakes the IC up from a sleep mode.
11	V_{CC}	Power supply input for internal logic.
12	OUT2	Half Bridge Output 2.
13	OUT1	Half Bridge Output 1.
14	GND*	Ground. Connect all grounds together.

*Pins 1, 7, 8, and 14 are internally shorted together. It is recommended to also short these pins externally.



* D1 optional. For use where reverse battery protection is required.
** D2 optional. For use where load dump exceeds 40V.
*** C2−C4, Recommended for EMC performance.

Figure 3. Application Circuit

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage (V_S) (DC) (AC), t < 500 ms, Ivs > −2 A	 −0.3 to 40 −1	V
Output Pin OUTx (DC) (AC), t < 500 ms, IOUTx > −2 A	 −0.3 to 40 −1	V
Pin Voltage (Logic Input pins, SI, SCLK, CSB, SO, EN, V_{CC})	−0.3 to 5.5	V
Output Current (OUTx) (DC) (AC) (50 ms pulse, 1 s period)	 −2.0 to 2.0 −5.0 to 5.0	A
Electrostatic Discharge, Human Body Model, V_S, OUT1, OUT2, OUT3 (Note 3)	6	kV
Electrostatic Discharge, Human Body Model, all other pins (Note 3)	2	kV
Electrostatic Discharge, Machine Model, V_S, OUT1, OUT2, OUT3 (Note 3)	300	V
Electrostatic Discharge, Machine Model, all other pins (Note 3)	200	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−55 to 150	°C
Moisture Sensitivity Level (MAX 260°C Processing)	MSL3	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Thermal Parameters	Test Conditions (Typical Value)		Unit
14 Pin Fused SOIC Package	min−pad board (Note 1)	1″ pad board (Note 2)	
Junction−to−Lead (psi−JL8, Ψ_{JL8}) or Pins 1, 7, 8, 14	23	22	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	122	83	°C/W

1. 1−oz copper, 67 mm^2 copper area, 0.062″ thick FR4.
2. 1−oz copper, 645 mm^2 copper area, 0.062″ thick FR4.
3. This device series incorporates ESD protection and is characterized by the following methods:
   ESD HBM according to AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM according to AEC−Q100−003 (EIA/JESD22−A115)

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
GENERAL					
Supply Current (V_S) Sleep Mode (Note 5)	V_S = 13.2 V, OUTx = 0 V EN = SI = SCLK = 0 V, CSB = V_{CC} 0 V < V_{CC} < 5.25 V (T_J = −40°C to 85°C)	–	1.0	5.0	μA
	V_S = 13.2 V, OUTx = 0 V EN = SI = SCLK = 0 V, CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C	–	–	2.0	μA
Supply Current (V_S) Active Mode	EN = V_{CC}, 5.5 V < V_S < 35 V No Load	–	2.0	4.0	mA
Supply Current (V_{CC}) Sleep Mode (Note 6)	V_{CC} = CSB, EN = SI = SCLK = 0 V (T_J = −40°C to 85°C)	–	0.1	2.5	μA
Supply Current (V_{CC}) Active Mode	EN = V_{CC}	–	1.5	3.0	mA
V_{CC} Power−On−Reset Threshold		–	2.55	2.90	V
V_S Undervoltage Detection Threshold Hysteresis	V_S decreasing	3.7 100	4.1 365	4.5 450	V mV
V_S Overvoltage Detection Threshold Hysteresis	V_S increasing	33.0 1.0	36.5 2.5	40.0 4.0	V
Thermal Warning (Note 4) Threshold Hysteresis		120 –	140 20	170 –	°C
Thermal Shutdown (Note 4) Threshold Hysteresis		155 –	175 30	195 –	°C
Ratio of Thermal Shutdown to Thermal Warning temperature (Note 4)		1.05	1.20	–	°C/°C
OUTPUTS					
Output $R_{DS(on)}$ (Source)	I_{out} = −500 mA	–	–	1.7	Ω
Output $R_{DS(on)}$ (Sink)	I_{out} = 500 mA	–	–	1.7	Ω
Source Leakage Current Sum of I(OUTx) x = 1, 2, 3	OUTx = 0 V, V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V Sum(I(OUTx)	−5.0	–	–	μA
	OUTx = 0 V, V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C Sum(I(OUTx)	−1.0	–	–	
Sink Leakage Current	OUTx = V_S = 40 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V	–	–	300	μA
	OUTx = V_S = 13.2 V, EN = 0 V CSB = V_{CC} 0 V < V_{CC} < 5.25 V, T_J = 25°C	–	–	10	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Thermal characteristics are not subject to production test
5. For temperatures above 85°C, refer to Figure 6.
6. For temperatures above 85°C, refer to Figure 7.
7. Current limit is active with and without overcurrent detection.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
OUTPUTS					
Under Load Detection Threshold Source Sink		−17 2.0	−7.0 7.0	−2.0 17	mA
Power Transistor Body Diode Forward Voltage	I_f = 500 mA	–	0.9	1.3	V
OVERCURRENT					
Overcurrent Shutdown Threshold (OUTHx)	V_{CC} = 5 V, Vs = 13.2 V	−2.0	−1.45	−1.1	A
Overcurrent Shutdown Threshold (OUTLx)	V_{CC} = 5 V, Vs = 13.2 V	1.1	1.45	2.0	A
CURRENT LIMIT (Note 7)					
Current Limit (OUTHx)	V_{CC} = 5 V, Vs = 13.2 V	−5.0	−3.0	−2.0	A
Current Limit (OUTLx)	V_{CC} = 5 V, Vs = 13.2 V,	2.0	3.0	5.0	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS (EN, SI, SCLK, CSB)						
Input Threshold High Low			 2.0 –	 – –	 – 0.8	V
Input Hysteresis (EN, SI, SCLK, CSB)			100	400	800	mV
Pulldown Resistance (EN, SI, SCLK)		EN = SI = SCLK = V_{CC}	50	125	250	kΩ
Pullup Resistance (CSB)		CSB = 0 V	50	125	250	kΩ
Input Capacitance (Note 8)			–	10	15	pF
LOGIC OUTPUT (SO)						
Output High		I_{out} = 1 mA	V_{CC} – 1.0	V_{CC} – 0.7	–	V
Output Low		I_{out} = −1.6 mA	–	0.2	0.4	V
Tri−state Leakage		CSB = V_{CC}, 0 V ≤ SO ≤ V_{CC}	−10	–	10	μA
Tri−state Input Capacitance (Note 8)		CSB = V_{CC}	–	10	15	pF
TIMING SPECIFICATIONS						
Under Load Detection Delay Time			200	350	600	μs
Overcurrent Shutdown Delay Time		V_{CC} = 5 V, Vs = 13.2 V, Bit13 = 0 Bit13 = 1	 80 10	 200 25	 400 50	 μs μs
High Side Turn On Time	ThsOn	V_S = 13.2 V, R_{load} = 25 Ω	–	7.5	15	μs
High Side Turn Off Time	ThsOff	V_S = 13.2 V, R_{load} = 25 Ω	–	3.0	6.0	μs
Low Side Turn On Time	TlsOn	V_S = 13.2 V, R_{load} = 25 Ω	–	6.5	15	μs
Low Side Turn Off Time	TlsOff	V_S = 13.2 V, R_{load} = 25 Ω	–	3.0	6.0	μs
High Side Rise Time	ThsTr	V_S = 13.2 V, R_{load} = 25 Ω	–	5.0	10	μs
High Side Fall Time	ThsTf	V_S = 13.2 V, R_{load} = 25 Ω	–	2.0	5.0	μs
Low Side Rise Time	TlsTr	V_S = 13.2 V, R_{load} = 25 Ω	–	1.0	3.0	μs
Low Side Fall Time	TlsTf	V_S = 13.2 V, R_{load} = 25 Ω	–	1.0	3.0	μs
NonOverlap Time	ThsOffLsOn	High Side Turn Off to Low Side Turn On	1.0	–	–	μs
NonOverlap Time	TlsOffHsOn	Low Side Turn Off to High Side Turn On	1.0	–	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Not production tested.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ V_S ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE (V_{CC} = 5 V)						
SCLK Frequency		–	–	–	5.0	MHz
SCLK Clock Period	V_{CC} = 5 V V_{CC} = 3.3 V	–	200 500	– –	– –	ns
SCLK High Time		TCLKH	85	–	–	ns
SCLK Low Time		TCLKL	85	–	–	ns
SCLK Setup Time		TCLKSU1 TCLKSU2	85 85	– –	– –	ns
SI Setup Time		TISU	50	–	–	ns
SI Hold Time		TIHT	50	–	–	ns
CSB Setup Time		TCSBSU1 TSSBSU2	100 100	– –	– –	ns
CSB High Time (Note 10)		TCSBHT	5.0	–	–	μs
SO enable after CSB falling edge		TSOCSBF	–	–	50	ns
SO disable after CSB rising edge		TSOCSBR	–	–	50	ns
SO Rise Time (10% to 90%)	C_{load} = 40 pF	–	–	10	25	ns
SO Fall Time (90% to 10%)	C_{load} = 40 pF	–	–	10	25	ns
SO Valid Time (Note 9)	SCLK High to SO 50%	TSOV	–	50	100	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Not tested in production
10. This is the minimum time the user must wait between SPI commands.

CHARACTERISTIC TIMING DIAGRAMS

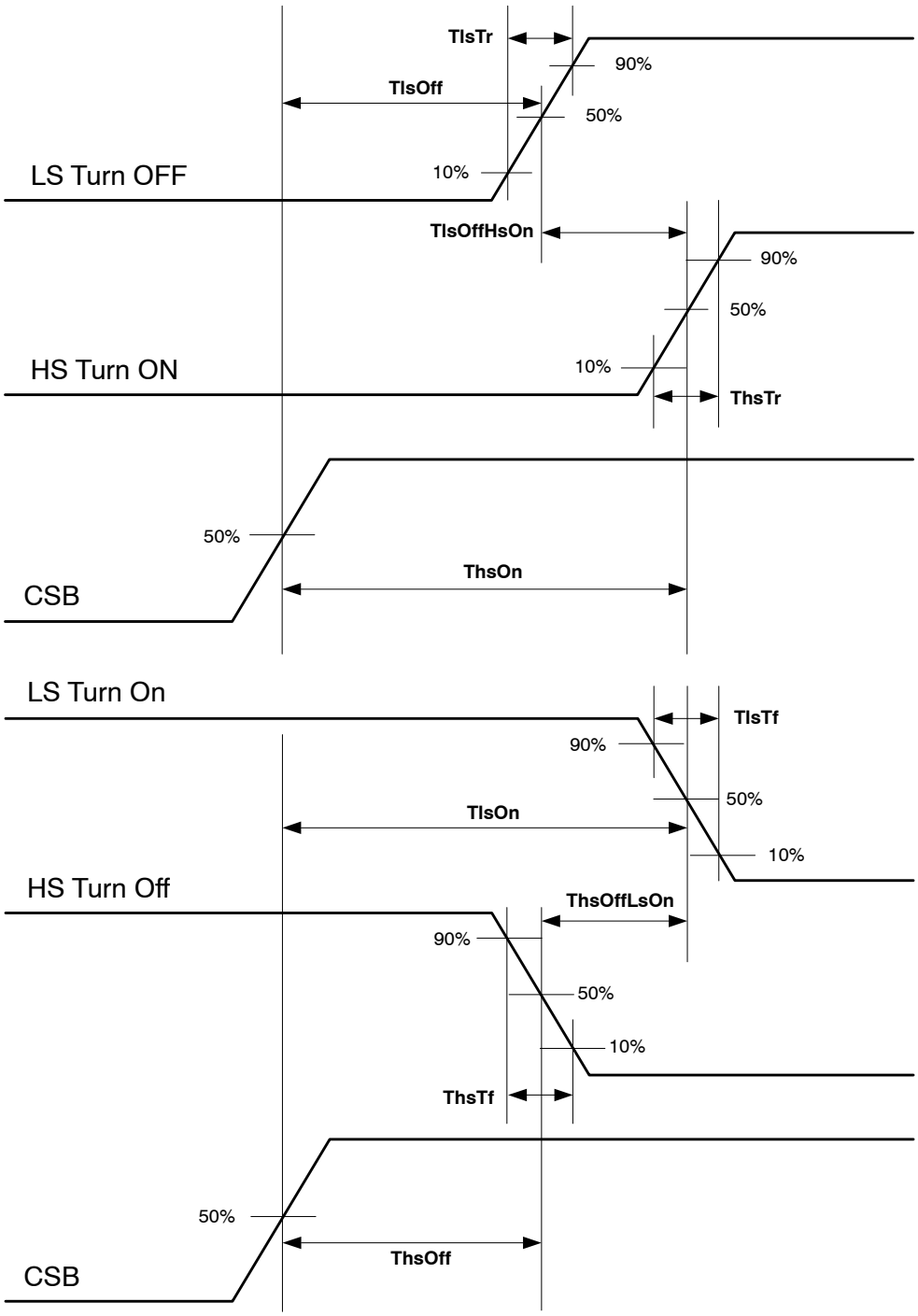


Figure 4. Detailed Driver Timing

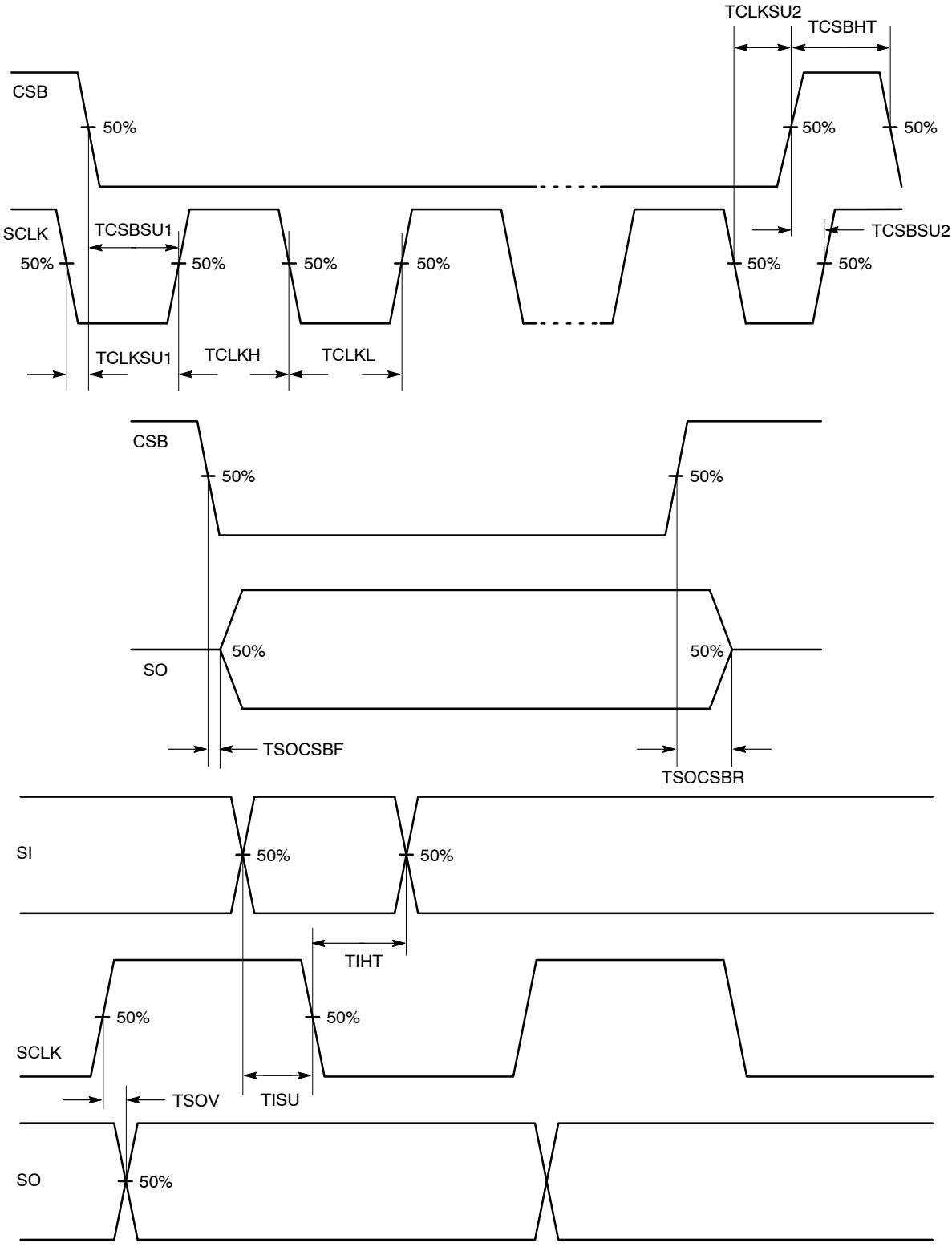


Figure 5. SPI Timing Diagram

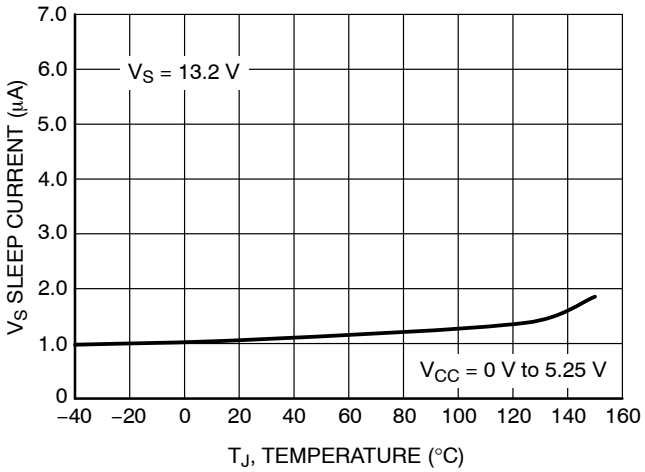


Figure 6. V_S Sleep Supply Current vs. Temperature

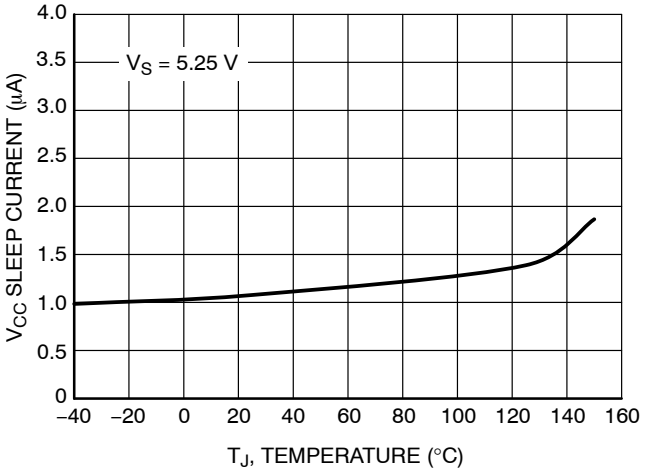


Figure 7. V_{CC} Sleep Supply Current vs. Temperature

TYPICAL CHARACTERISTICS

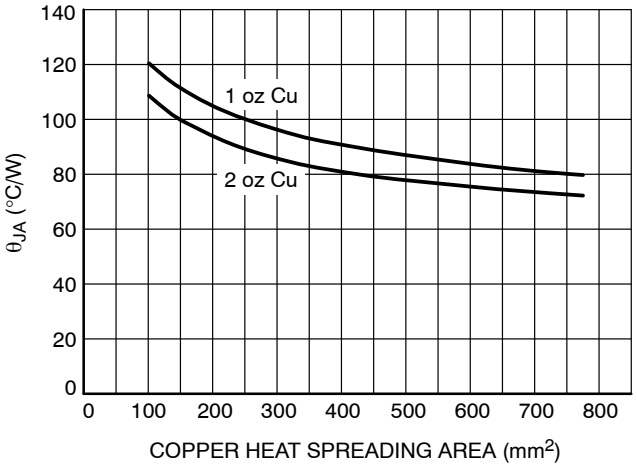


Figure 8. θ_{JA} vs. Copper Spreader Area, 14 Lead SON (fused leads)

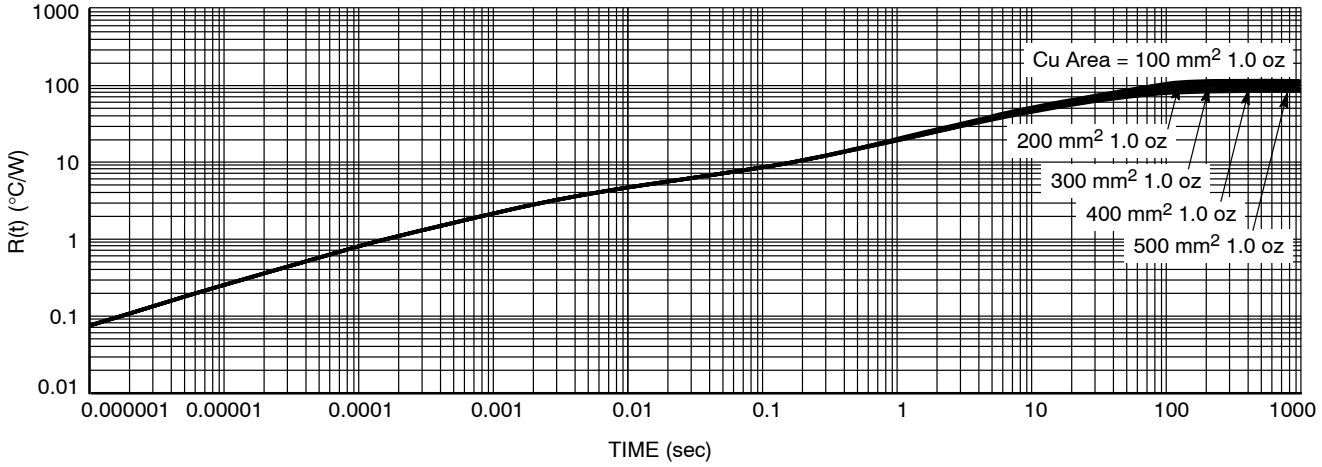


Figure 9. Transient Thermal Response to a Single Pulse 1 oz Copper (Log−Log)

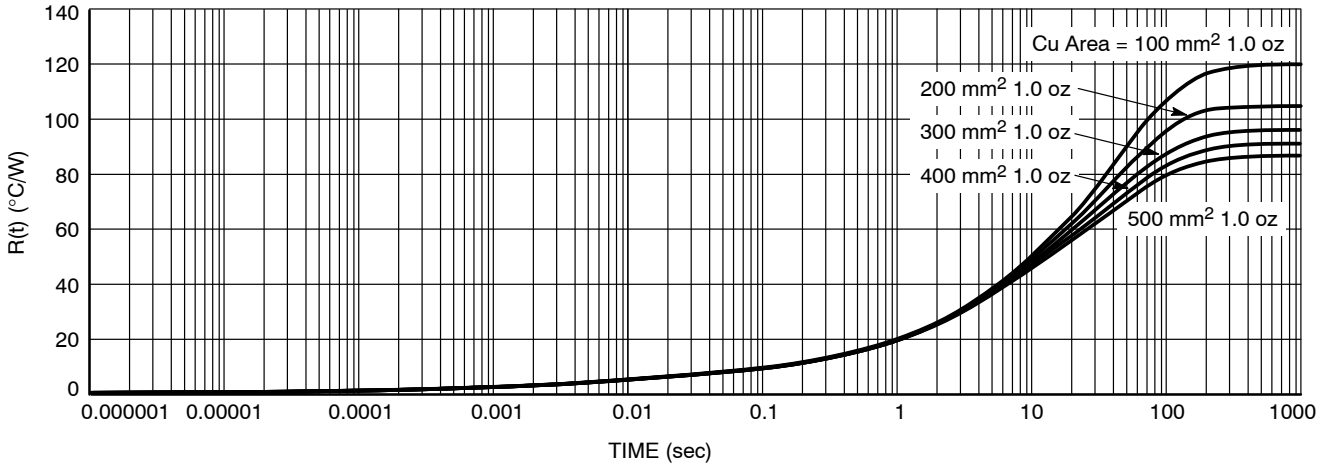


Figure 10. Transient Thermal Response to a Single Pulse 1 oz Copper (Semi−Log)

SPI Communication

Standard 16−bit communication has been implemented to this IC to turn drivers on/off, and to report faults. (See Figure 12). The LSB (Least Significant Bit) is clocked in first.

Communication is Implemented as Follows:

1. CSB goes low to allow serial data transfer.
2. A 16 bit word is clocked (SCLK) into the SI (Serial Input) pin.
3. CSB goes high to transfer the clocked in information to the data registers.

NOTE: SO is tristate when CSB is high.

Frame Detection

Input word integrity (SI) is evaluated by the use of a frame consistency check. The word frame length is compared to an η x 16 bit acceptable word length before the data is latched into the input register. This guarantees the proper word length has been imported and allows for daisy chain operation applications.

The frame length detector is enabled with the CSB falling edge and the SCLK rising edge.

SCLK must be low during the CSB rising edge. The fault register is cleared with a valid frame detection. Existing faults are re−latched after the fault filter time.

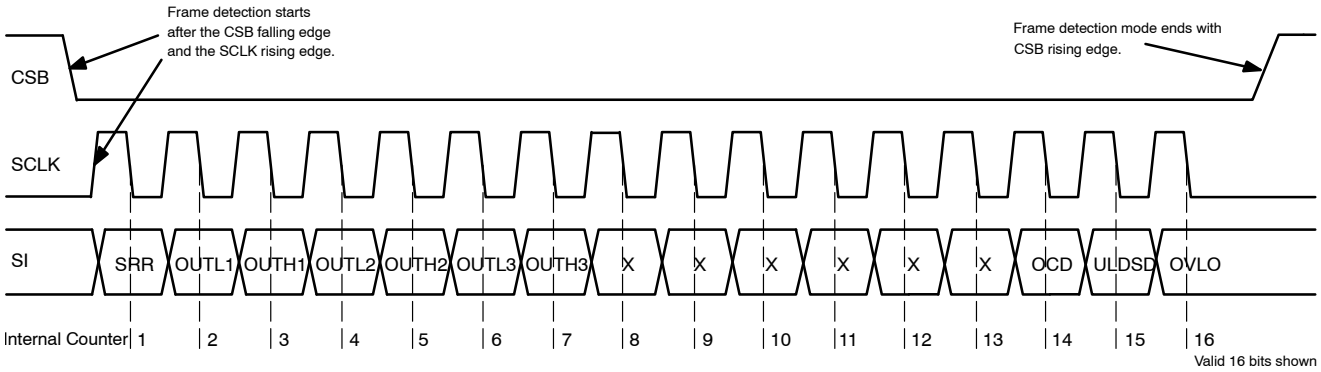


Figure 11. Frame Detection

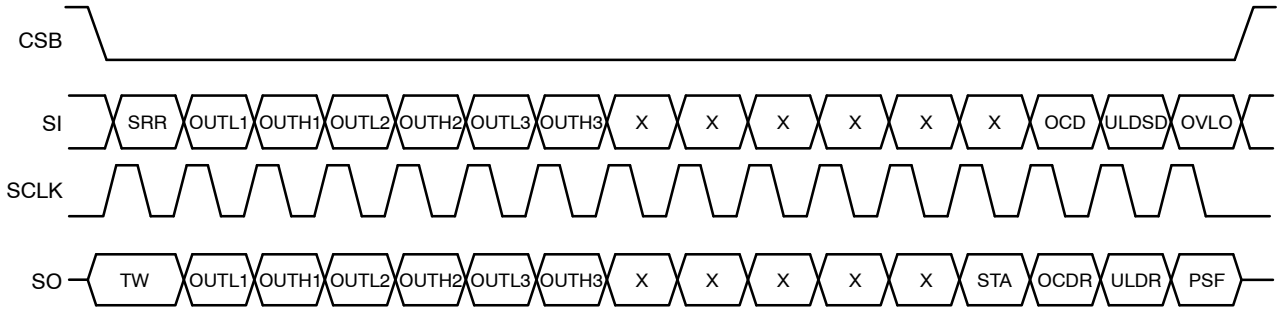


Figure 12. SPI Communication Frame Format

Table 1 defines the programming bits and diagnostic bits. Figure 12 displays the timing diagram associated with Table 1. Fault information is sequentially clocked out the SO pin of the NCV7703C as programming information is clocked into the SI pin of the device. Daisy chain communication between SPI compatible IC's is possible by connection of the Serial Output pin (SO) to the input of the sequential IC (SI) (Reference the Daisy Chain Section).

Table 1. SPI BIT DESCRIPTION

Input Data			Output Data		
Bit Number	**Bit Description**	**Bit Status**	**Bit Number**	**Bit Description**	**Bit Status**
15	Over Voltage Lock Out Control (OVLO)	0 = Disable	15	V_S Power Supply Fail Signal (PSF for OVLO or UVLO)	0 = No Fault
		1 = Enable			1 = Fault
14	Under Load Detection Shut Down Control (ULDSD)	0 = Disable	14	Under Load Detection Reporting Signal (ULDR)	0 = No Fault
		1 = Enable			1 = Fault
13	Over Current Detection Shut Down Control (OCD)	0 = 200 μsec	13	Over Current Detection Reporting Signal (OCDR)	0 = No Fault
		1 = 25 μsec			1 = Fault
12	Not Used		12	Shoot−Through Attempt (STA)	0 = No Attempt
					1 = Attempt
11	Not Used		11	Not Used	
10	Not Used		10	Not Used	
9	Not Used		9	Not Used	
8	Not Used		8	Not Used	
7	Not Used		7	Not Used	
6	OUTH3	0 = Off	6	OUTH3	0 = Off
		1 = On			1 = On
5	OUTL3	0 = Off	5	OUTL3	0 = Off
		1 = On			1 = On
4	OUTH2	0 = Off	4	OUTH2	0 = Off
		1 = On			1 = On
3	OUTL2	0 = Off	3	OUTL2	0 = Off
		1 = On			1 = On
2	OUTH1	0 = Off	2	OUTH1	0 = Off
		1 = On			1 = On
1	OUTL1	0 = Off	1	OUTL1	0 = Off
		1 = On			1 = On
0	Status Register Reset (SRR)	0 = No Reset	0	Thermal Warning (TW)	0 = Not in TW
		1 = Reset			1 = In TW

DETAILED OPERATING DESCRIPTION

General

The NCV7703C Triple Half Bridge Driver provides drive capability for 3 Half−Bridge configurations. Each output drive is characterized for a 500 mA load and has a typical 1.4 A surge capability. Strict adherence to integrated circuit die temperature is necessary, with a maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port.

An Enable function (EN) provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the EN, SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull−up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Power Up/Down Control

A feature incorporated in the IC is an under voltage lockout circuit that prevents the output drivers from turning on unintentionally. V_{CC} and V_S are monitored for undervoltage conditions supporting a smooth turn−on transition. All drivers are initialized in the off (high impedance) condition, and will remain off during a V_{CC} or V_S undervoltage condition. This allows power up sequencing of V_{CC}, and V_S up to the user. Once V_{CC} is above the Power−On−Reset threshold, SPI communication can begin regardless of the voltage on V_S. The V_S supply input does not ever affect the SPI logic. However, drivers will remain off if V_S is in an undervoltage condition. Hysteresis in both V_{CC} and V_S circuits results in glitch free operation during power up/down.

Overvoltage Shutdown (Table 2)

Overvoltage lockout circuitry monitors the voltage on the V_S pin. The response to an overvoltage condition is selected by SPI input bit 15. PSF output bit 15 is set when a V_S overvoltage condition exists. If input bit 15 (OVLO) is set to "1", all outputs will turn off during this overvoltage condition. Turn On/Off status is maintained in the logic circuitry, so that when proper input voltage level is reestablished, the programmed outputs will turn back on. The PSF output bit is reset with SRR = 1.

Table 2. INPUT BIT 15, OVERVOLTAGE LOCK OUT (OVLO) SHUT DOWN

OVLO Input Bit 15	V_S OVLO Condition	Output Data Bit 15 Power Supply Fail (PSF) Status	OUTx Status
0	0	0	Unchanged
0	1	1 (Need SRR to reset)	Unchanged
1	0	0	Unchanged
1	1	1 (Need SRR to reset)	All Outputs Shut Off (Remain off until V_S is out of OVLO)

H−Bridge Driver Configuration

The NCV7703C has the flexibility of controlling each half bridge driver independently. This allows for high side, low side and H−bridge control. H−bridge control provides forward, reverse, brake and high impedance states.

Overvoltage Clamping − Driving Inductive Loads

Each output is internally clamped to ground and VS by internal freewheeling diodes. The diodes have ratings that complement the FETs they protect. A flyback event from driving an inductive load causes the voltage on the output to rise up. Once the voltage rises higher than VS by a diode voltage (body diode of the high−side driver), the energy in the inductor will dissipate through the diode to VS. If a reverse battery diode is used in the system, care must be taken to insure the power supply capacitor is sufficient to dampen any increase in voltage to VS caused by the current flow through the body diode so that it is below 40 V. Negative transients will momentarily occur when a high−side driver driving an inductive load is turned off. This will be clamped by an internal diode from the output pin (OUT1 or OUT2) to the IC ground.

Current Limit

OUTx current is limited per the Current Limit electrical parameter for each driver. The magnitude of the current has a minimum specification of 2 A at V_{CC} = 5 V and V_s = 13.2 V. The output is protected for high power conditions during Current Limit by thermal shutdown and the Overcurrent Detection shutdown function. Overcurrent Detection shutdown protects the device during current limit because the Overcurrent threshold is below the Current Limit threshold. The Overcurrent Detection Shutdown Control Timer is initiated at the Overcurrent Shutdown Threshold which starts before the Current Limit is reached.

Note: High currents will cause a rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

Shoot−Through Attempt

The NCV7703C provides detection for attempting to turn on common drivers of the same channel (OUTL1&OUTH1, OUTL2&OUTH2, OUTL3&OUTH3) simultaneously. An attempt to turn on common drivers if allowed would result in a high current event from VS to GND. Any attempt to create this setup is recorded in bit 12 of the output data and forces the common high−side and low−side driver to an off state. The STA output bit is reset with SRR = 1. The STA bit must be cleared before an affected driver can turn on.

Overcurrent Shutdown

Effected outputs will turn off when the Overcurrent Shutdown Threshold has been breached for the Overcurrent Shutdown Delay Time. The respective OCDR status bit will be set to a "1" and the driver will latch off. The driver can only be turned back on via the SPI port with a SPI command that includes an SRR = 1.

Note: High currents will cause a rise in die temperature. Devices will not be allowed to turn on if the die temperature exceeds the thermal shutdown temperature.

Table 3. OVERCURRENT DETECTION SHUT DOWN

OCD Input Bit 13	OUTx OCD Condition	Output Data Bit 13 Over Current Detect (OCDR) Status	OUTx Status	Current Limit of all Drivers
0	0	0	Unchanged	3 A
0	1	1 (Need SRR to reset)	OUTx Latches off after 200 μs (Need SRR to reset)	3 A
1	0	0	Unchanged	3 A
1	1	1 (Need SRR to reset)	OUTx Latches Off After 25 μs (Need SRR to reset)	3 A

Overcurrent Detection Shut Down Control Timer

There are two protection mechanisms for output current, overcurrent and current limit.

1. Current limit − Always active with a typical threshold of 3 A (typ).
2. Overcurrent Detection − Selectable shutdown time via Bit 13 with a 1.45 A (typ) threshold.

Figure 13 shows the typical performance of a part which has exceeded the 1.45 A (typ) Overcurrent Detection threshold and started the shutdown control timer. When Bit 13 = 1, the shutdown time is 25 μsec (typ). When Bit 13 = 0, the shutdown time is 200 μsec (typ).

Once an Overcurrent Shutdown Delay Time event has been detected by the NCV7703C, the timer setting cannot be interrupted by an attempted change via a SPI command of Bit 13.

Table 4.

Input Bit 13	Overcurrent Shutdown Delay Time
0	200 μsec (typ)
1	25 μsec (typ)

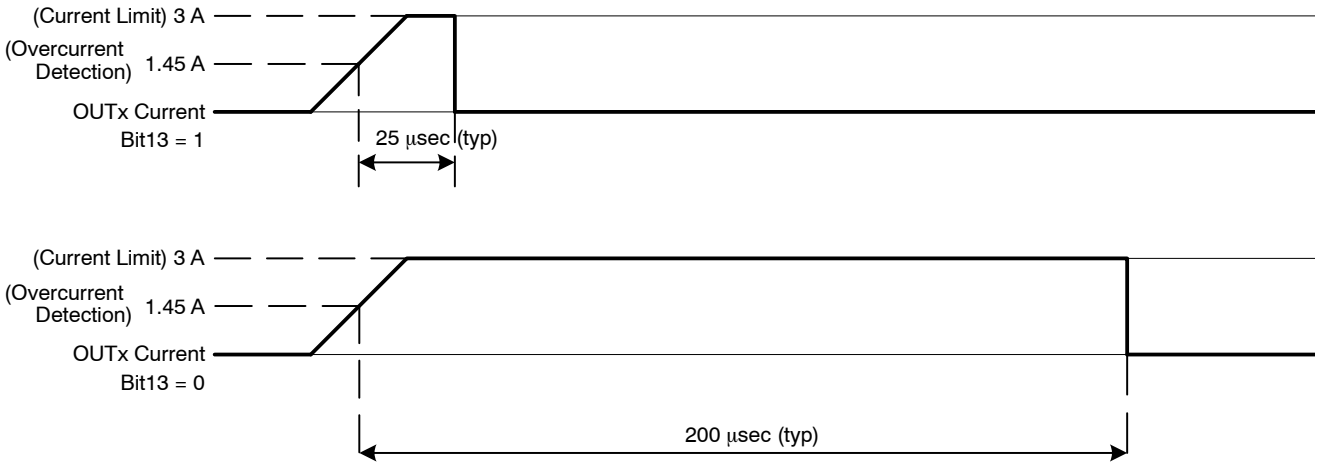


Figure 13. Output Current Shutdown Control

UnderLoad Detection (Table 5)

The underload detection circuit monitors the current from each output driver. A minimum load current (this is the maximum open circuit detection threshold) is required when the drivers are turned on. If the under−load detection threshold has been detected continuously for more than the under−load delay time, the ULDR bit (output bit #14) will be set to a “1”. In addition, the offending driver will be latched off if input Bit 14 (ULDSD) is set to 1 (true).

The NCV7703C uses a global under load timer. An under load condition starts the global under load delay timer. If under load occurs in another channel after the global timer has been started, the delay for any subsequent under load will be the remainder of the initially started timer. The timer runs continuously with any persistent under load condition and will impact multi−underload situations. The under load detect bit is reset by setting input data bit 0, SRR = 1. Figures 14 and 15 highlight the timing conditions for an underload state where the global timer is reset (discontinuous time) and the conditions where the global timer is not reset (continuous time).

Table 5. OUTPUT BIT 14, UNDER LOAD DETECTION SHUT DOWN

ULDSD Input Bit 14	OUTx ULD Condition	Output Data Bit 14, Under Load Detect (ULDR) Status	OUTx Status
0	0	0	Unchanged
0	1	1 (Need SRR to reset)	Unchanged
1	0	0	Unchanged
1	1	1 (Need SRR to reset)	OUTx Latches Off (Need SRR to reset)

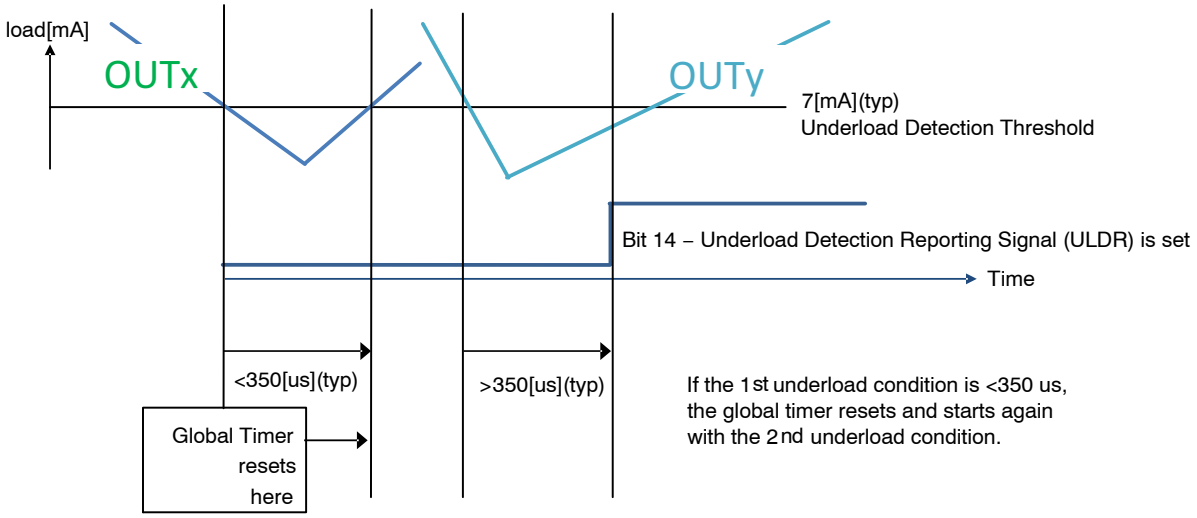


Figure 14. Underload Discontinuous Time

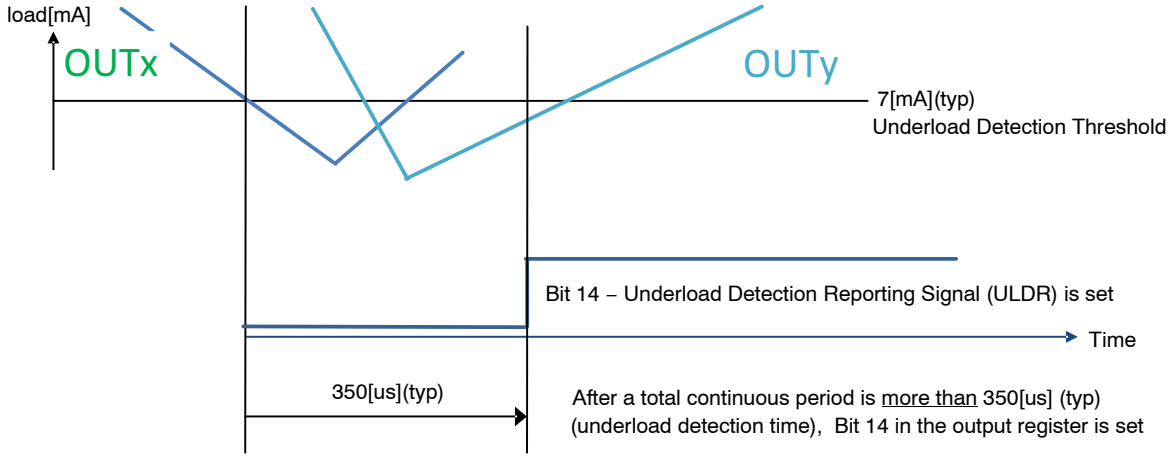


Figure 15. Underload Continuous Time

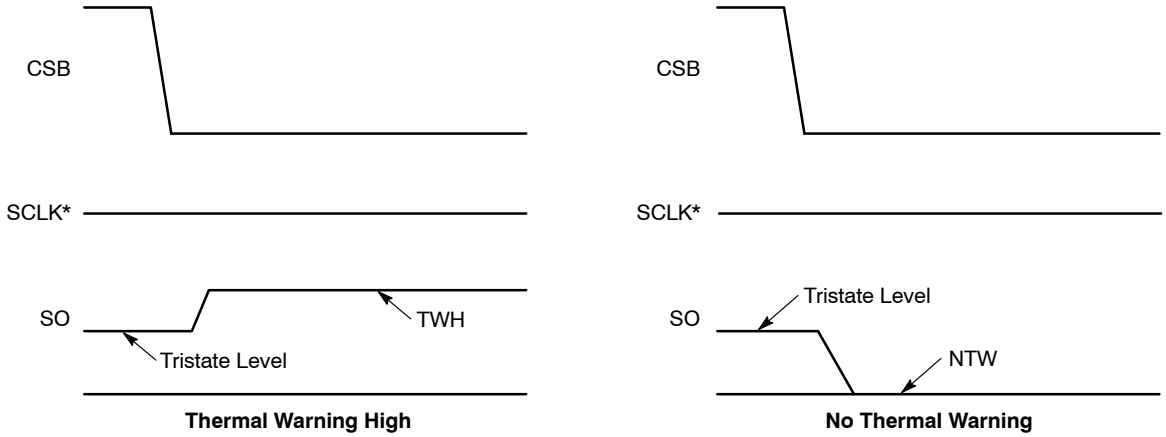
Thermal Shutdown

Three independent thermal shutdown circuits are featured (one common sensor for each HS and LS transistor pair). Each sensor has two temperature levels; Level 1, Thermal Warning sets the “TW” status bit to a 1 and would have to be reset with a command that includes the SRR after the IC cools to a temperature below Level 1. The output will remain on in this condition.

If the IC temperature reaches Level 2, Over Temperature Shutdown, all drivers are latched off. It can be reset only after the part cools below the shutdown temperature, (including thermal hysteresis) with a turn−on command that includes the SRR set bit.

The output data bit 0, Thermal Warning, will latch and remain set, even after cooling, and is reset by sending a SPI command to reset the status register (SRR, input 0 set to “1”). Since thermal warning precedes a thermal shutdown, software polling of this bit will allow for load control and possible prevention of thermal shutdown conditions.

Thermal warning information can be retrieved immediately without performing a complete SPI access cycle. Figure 16 below displays how this is accomplished. Bringing the CSB pin from high to low with SI = 0 immediately displays the information on Output Data Bit 0, thermal warning. As the temperature of the NCV7703C changes from a condition from below the thermal warning threshold to above the thermal warning threshold, the state of the SO pin changes and this level is available immediately when the CSB goes low. A low on SO indicates there is no thermal warning, while a high indicates the IC is above the thermal warning threshold. This warning bit is reset by setting SRR to “1”.



*SCLK can be high or low in order to maintain the thermal information on SO. Toggling SCLK will cause other output bits to shift out.
TWH = Thermal Warning High
NTW = No Thermal Warning

Figure 16. Access to Temperature Warning Information

Applications Drawing

Daisy Chain

The NCV7703C is capable of being setup in a daisy chain configuration with other similar devices which include additional NCV7703C devices as well as the NCV7708 Double Hex Driver. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be the Diagnostic Output Data. These are the bits representing the status of the IC and are detailed in the SPI Bit Description Table. Additional programming bits should be clocked in which follow the Diagnostic Output bits. Word length must be η x 16 due to the use of frame detection.

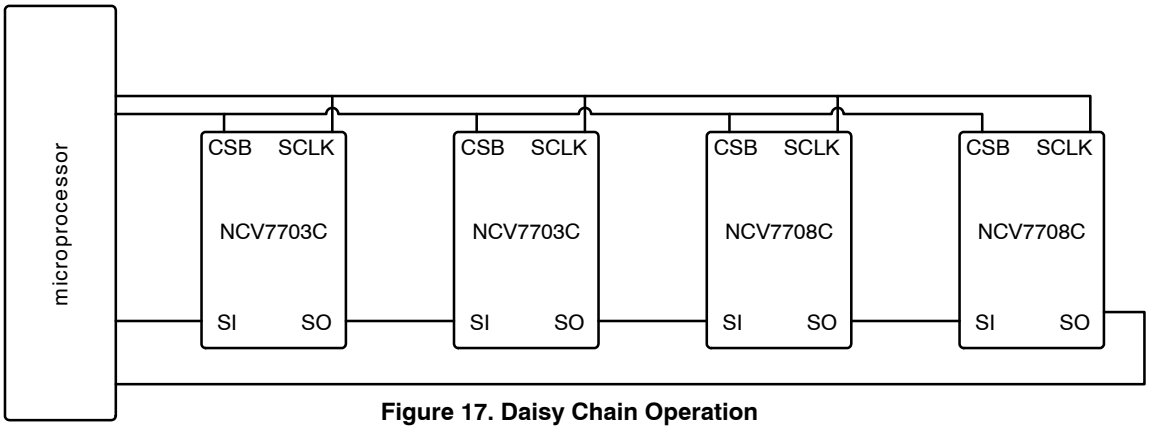


Figure 17. Daisy Chain Operation

Parallel Control

A more efficient way to control multiple SPI compatible devices is to connect them in a parallel fashion and allow each device to be controlled in a multiplex mode. The diagram below shows a typical connection between the microprocessor or microcontroller and multiple SPI compatible devices. In a daisy chain configuration, the programming information for the last device in the serial string must first pass through all the previous devices. The parallel control setup eliminates that requirement, but at the cost of additional control pins from the microprocessor for each individual CSB pin for each controllable device. Serial data is only recognized by the device that is activated through its respective CSB pin.

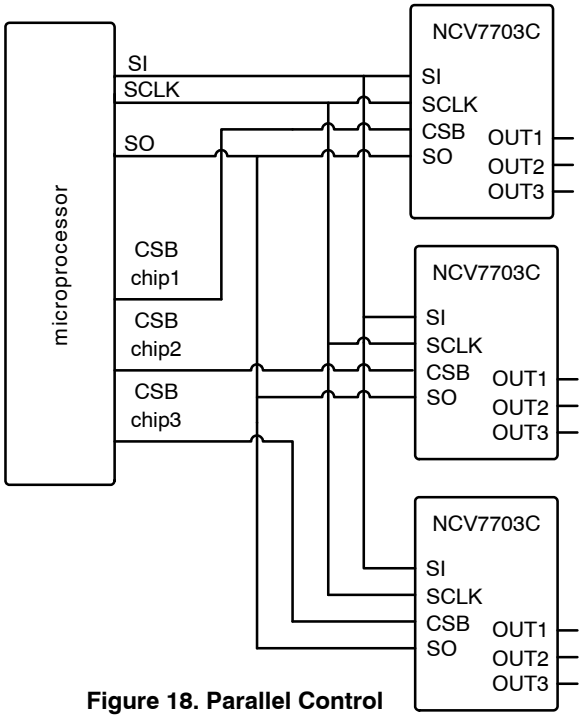


Figure 18. Parallel Control

Additional Application Setup

In addition to the cascaded H−Bridge application shown in Figure 1, the NCV7703C can also be used as a high−side driver or low−side driver (Figure 19).

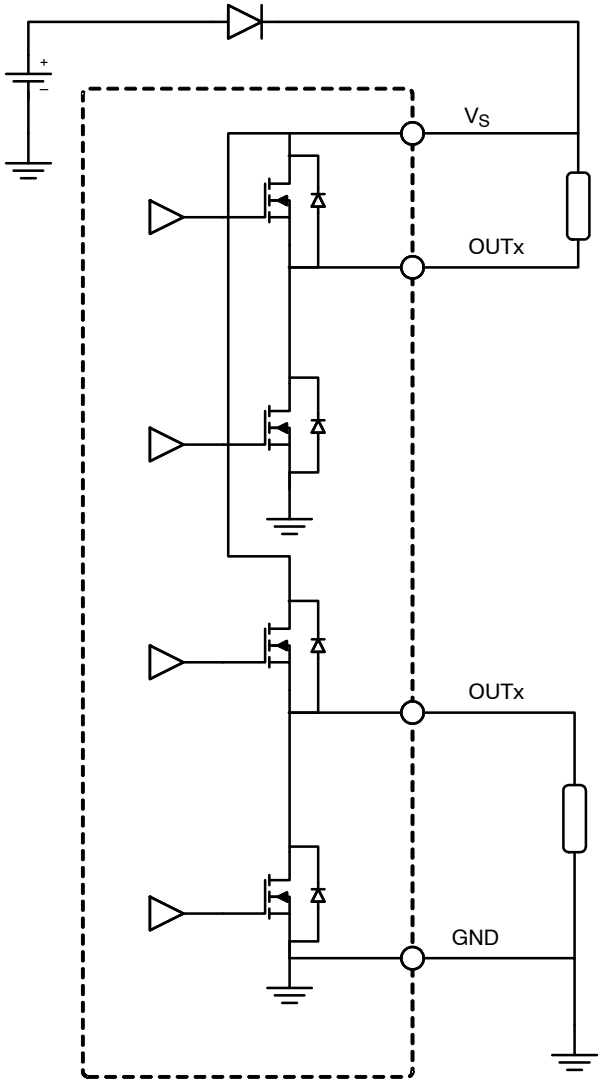
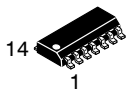


Figure 19. High−Side / Low−Side Application Drawing

Any combination of H−bridge and high or low−side drivers can be designed in. This allows for flexibility in many systems.

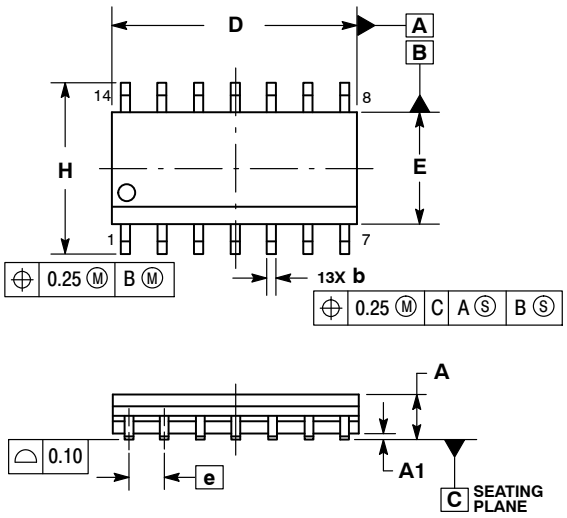
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

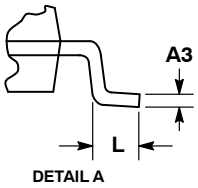


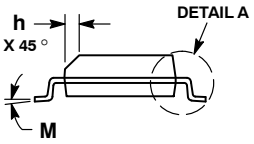
SCALE 1:1

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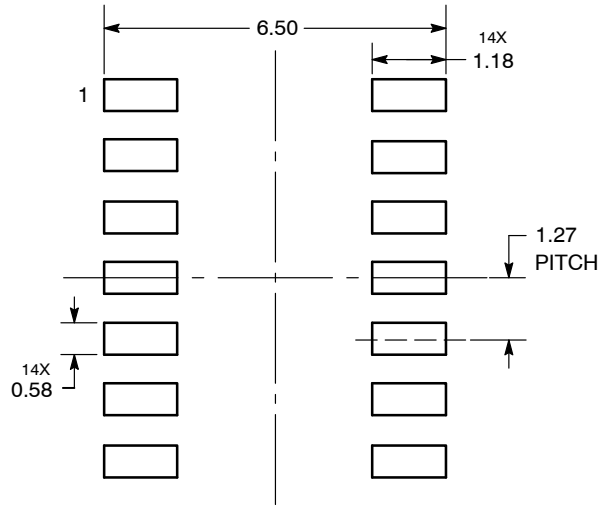




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

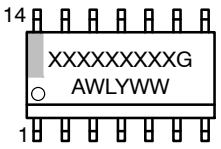
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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