10 Channel Half-Bridge Driver

NCV7725B

The NCV7725B is a ten channel half−bridge driver with protection features designed specifically for automotive and industrial motion control applications. The product has independent controls and diagnostics, and the drivers can be operated in forward, reverse, brake, and high impedance states. The device is controlled via a 16 bit SPI interface and is daisy chain compatible. Outputs 1 and 2 can be controlled through an external PWM signal.

Features

- Low Quiescent Current Sleep Mode
- High−Side and Low−Side Drivers Connected in Half−Bridge Configurations
- Integrated Freewheeling Protection (LS and HS)
- 500 mA Typical, 1.1 A Peak Current
- $R_{DS(on)}$ = 0.8 Ω (Typ)
- OUT1 and OUT2 External PWM Control
- 5 MHz SPI Communication
- 16 Bit Frame Error Detection
- Daisy Chain Compatible with Multiple of 8 bit Devices
- Compliance with 3.3 V and 5 V Systems
- Undervoltage and Overvoltage Lockout
- Per Channel Fault Reporting
- Overcurrent Protection
- Overtemperature Protection
- Underload Detection (HS and LS)
- Exposed Pad Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Automotive
- Industrial
- DC Motor Management for HVAC Application

MARKING DIAGRAM



SSOP24 NB EP
CASE 940AK



NCV7725B = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 25 of this data sheet.

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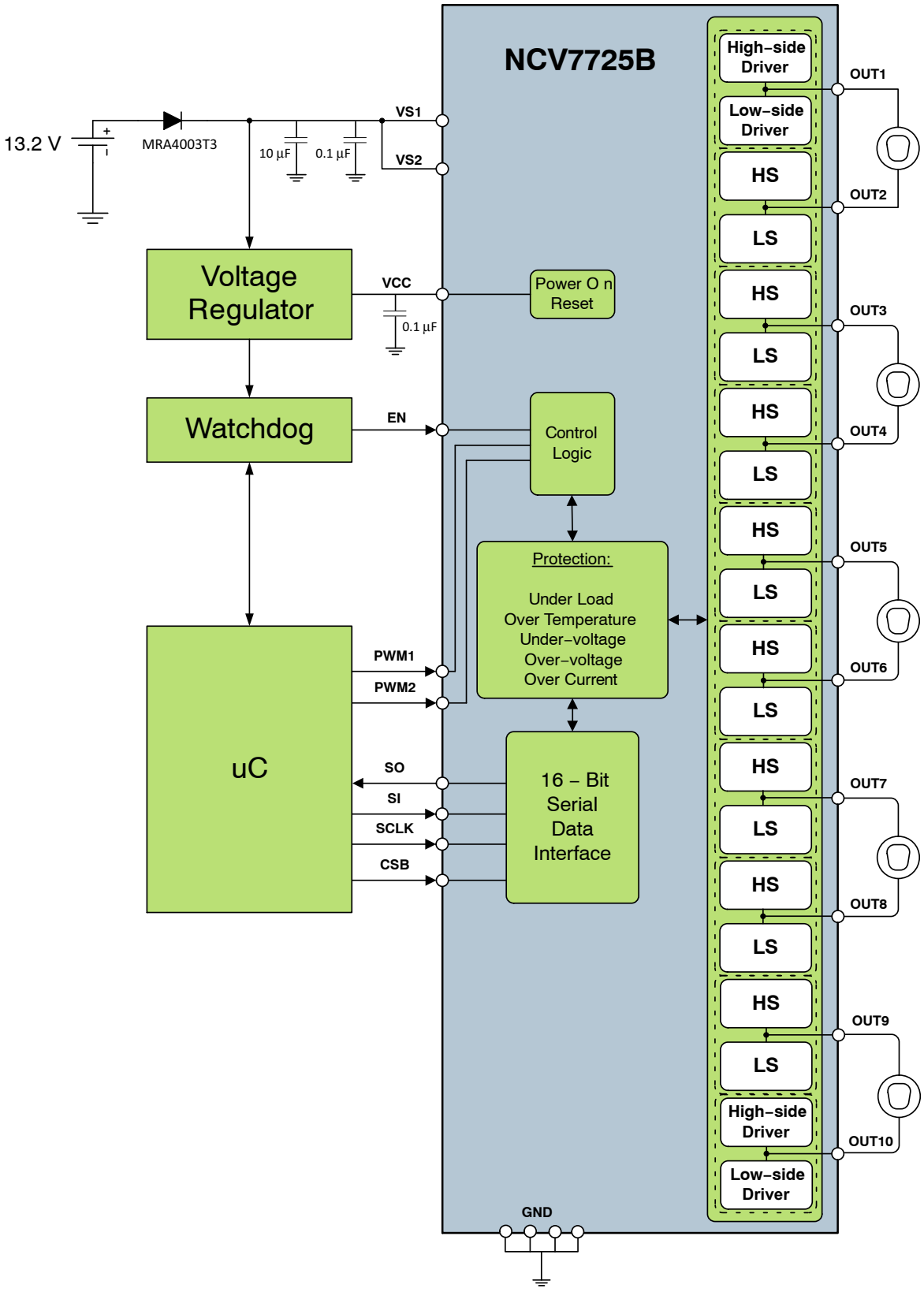


Figure 1. Typical Application

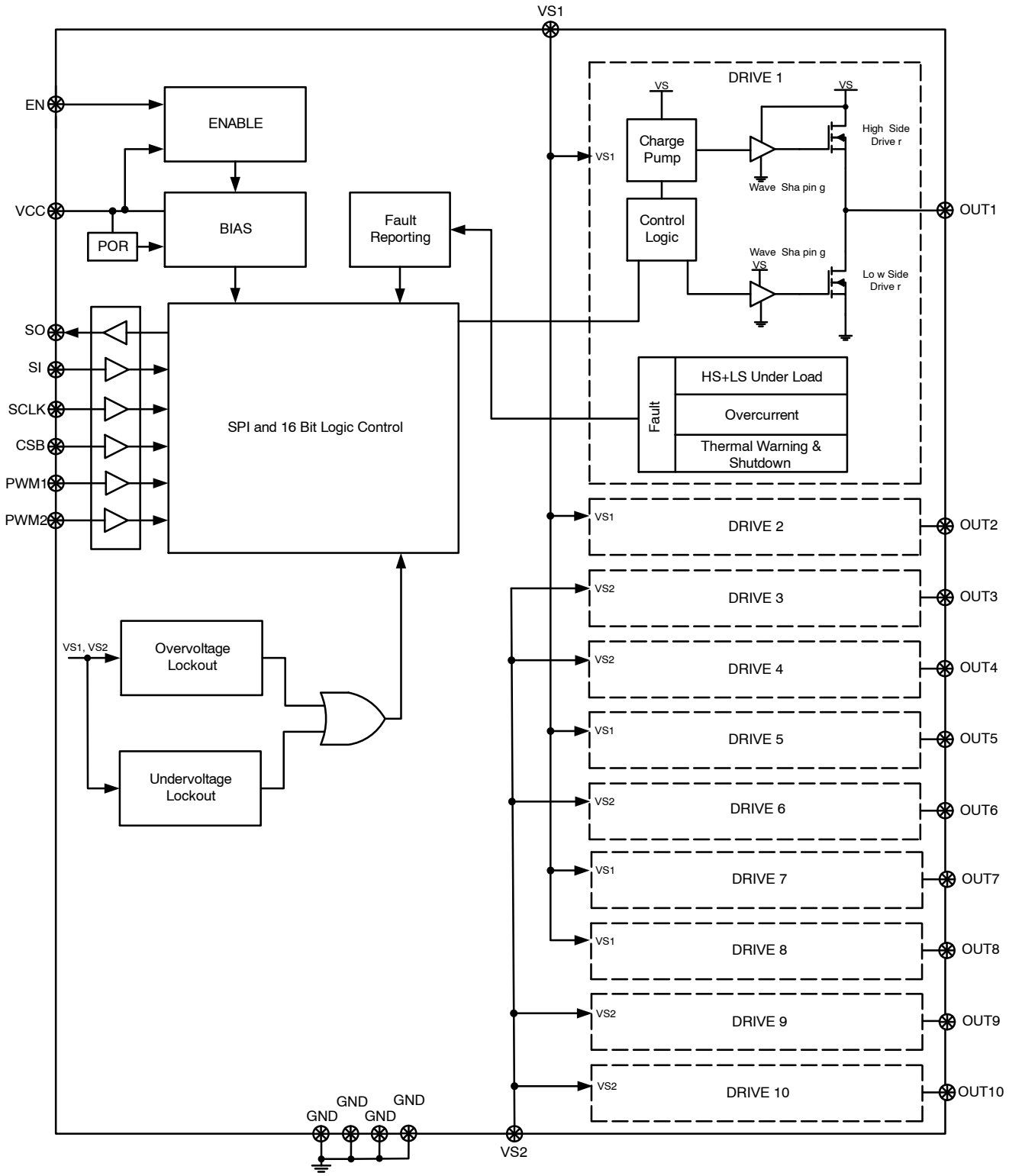


Figure 2. Block Diagram

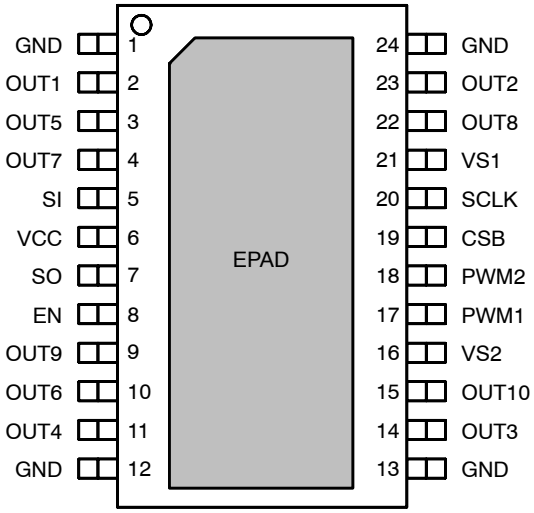


Figure 3. Pinout – SSOP24 NB EP

PIN FUNCTION DESCRIPTION The pin−out for the Half−Bridge Driver in SSOP24 NB EP package is shown in the table below.

Pin# SSOP24	Symbol	Description
1	GND	Ground. Must be connected to other GND pins externally.
2	OUT1	Half−bridge output 1
3	OUT5	Half−bridge output 5
4	OUT7	Half−bridge output 7
5	SI	16 bit serial communication input. 3.3 V / 5 V (TTL) Compatible − internally pulled down.
6	VCC	Power supply input for Logic.
7	SO	16 bit serial communication output. 3.3 V / 5 V Compliant
8	EN	Enable − active high; wakes the device from sleep mode. 3.3 V / 5 V (TTL) Compatible − internally pulled down.
9	OUT9	Half−bridge output 9
10	OUT6	Half−bridge output 6
11	OUT4	Half−bridge output 4
12	GND	Ground. Must be connected to other GND pins externally.
13	GND	Ground. Must be connected to other GND pins externally.
14	OUT3	Half−bridge output 3
15	OUT10	Half−bridge output 10
16	VS2	Power Supply input for outputs 3, 4, 6, 9, and 10. This pin must be connected to VS1 externally.
17	PWM1	External PWM input for output 1. 3.3 V / 5 V (TTL) Compatible − internally pulled down.
18	PWM2	External PWM input for output 2. 3.3 V / 5 V (TTL) Compatible − internally pulled down.
19	CSB	Chip select bar − active low; enables serial communication operation. 3.3 V / 5 V (TTL) Compatible − internally pulled up.
20	SCLK	Serial communication clock input. 3.3 V / 5 V (TTL) Compatible − internally pulled down.
21	VS1	Power Supply input for outputs 1, 2, 5, 7, and 8. This pin must be connected to VS2 externally.
22	OUT8	Half−bridge output 8
23	OUT2	Half−bridge output 2
24	GND	Ground. Must be connected to other GND pins externally.
EPAD	Exposed Pad	Connect to GND or leave unconnected.

MAXIMUM RATINGS (Voltages are with respect to GND)

Rating		Symbol	Value	Unit
VSx Pin Voltage	(VS1, VS2) (DC) (AC), t < 500 ms, Ivsx > −2 A	 VsxdcMax VSxac	 −0.3 to 45 −1.0	V
Pin Voltage	(Vcc, SI, SCLK, CSB, SO, EN, PWM1, PWM2)	VioMax	−0.3 to 5.5	V
OUTx Pin Voltage (DC) (AC) (AC), t < 500 ms, IOUTx > −1.1 A (AC), t < 500 ms, IOUTx < 1 A		 VoutxDc VoutxAc	 −0.3 to 45 −0.3 to 45 −1.0 1.0	V
OUTx Pin Current (OUT1, ..., OUT10)		IoutxImax	−2.0 to 2.0	A
Junction Temperature Range		T_J	−40 to 150	°C
Storage Temperature Range		Tstr	−55 to 150	°C
Peak Reflow Soldering Temperature: Pb−free 60 to 150 seconds at 217°C		(Note 1)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. See or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ATTRIBUTES

Characteristic		Symbol	Value	Unit
Short Circuit Reliability Characterization		AECQ10x	Grade A	
ESD Capability Human Body Model per AEC−Q100−002 Charged Device Model per AEC−Q100−011	 VSx, OUTx All Other Pins	 Vesd4k Vesd2k Vesd750	 ≥ ±4.0 kV ≥ ±2.0 kV ≥ ±750 V	
Moisture Sensitivity Level		MSL	MSL2	
Package Thermal Resistance − Still−air Junction−to−Ambient Junction−to−Board	 (Note 2) (Note 2)	 $R_{\theta JA}$ $R_{\Psi JBOARD}$	 31.0 12.0	 °C/W °C/W

2. Based on JESD51−7, 1.6 mm thick FR4, 2S2P PCB with 600 mm^2 2 oz. copper and 18 thermal vias to 80x80 mm 1 oz. internal spreader planes. Simulated with each channel dissipating 0.2 W.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Digital Supply Input Voltage	VCCOp	3.15	5.25	V
Battery Supply Input Voltage (VS1 = VS2)	VSxOp	5.5	32	V
DC Output Current	IxOp	−	0.5	A
Junction Temperature	TjOp	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
Supply Current (VS1 + VS2) Sleep Mode	IqVSx85	VS1 = VS2 = 13.2 V, V_{CC} = 0 V −40°C to 85°C	–	1.0	2.5	μA
Supply Current (VS1 + VS2) Active Mode	IvsOp	EN = V_{CC}, 5.5V < VSx < 32 V No Load,All Outputs Off	–	0.5	1.0	mA
Supply Current (Vcc) Sleep Mode Active Mode	 I_qV_{CC} $IV_{CC}Op$	CSB = V_{CC}, EN = SI = SCLK = 0 V −40°C to 85°C EN = CSB = V_{CC}, SI = SCLK = 0 V No Load, All Outputs Off	 – –	 1.0 1.5	 2.5 3.0	 μA mA
Total Sleep Mode Current I(VS1) + I(VS2) + I(VCC)	IqTot	Sleep Mode, −40°C to 85°C VS1 = VS2 = 13.2 V, No Load	–	2.0	5.0	μA
VCC Power−on Reset Threshold	V_{CC}por	V_{CC} increasing	–	2.70	2.90	V
VSx Undervoltage Detection Threshold	VSxuv	VSx increasing	3.7	4.3	4.7	V
		VSx decreasing	3.5	4.1	4.5	
VSx Undervoltage Detection Hysteresis	VSxuHys		–	200	–	mV
VSx Overvoltage Detection Threshold	VsXov	VSx increasing	32	36	40	V
		VSx decreasing	29.5	33.5	37.5	
VSx Overvoltage Detection Hysteresis	VSxoHys		–	2.5	–	V
DRIVER OUTPUT CHARACTERISTICS						
Output High $R_{DS(on)}$ (source)	RDSonHS	Iout = −500 mA, Vs = 13.2 V V_{CC} = 3.15 V	–	0.8	1.8	Ω
Output Low $R_{DS(on)}$ (sink)	RDSonLS	Iout = 500 mA, Vs = 13.2 V V_{CC} = 3.15 V	–	0.8	1.8	Ω
Source Leakage Current	 IsrcLkg13.2 IsrcLkg28	V_{CC} = 5 V, OUT (1−10) = 0 V, EN = 0/5 V VSx = 13.2 V VSx = 28 V	 −1.0 −2.0	 – –	 – –	 μA μA
Sink Leakage Current	 IsnkLkg13.2 IsnkLkg28	V_{CC} = 5 V, EN = 0/5 V OUT (1−10) = VSx = 13.2 V OUT (1−10) = VSx = 28 V	 – –	 – –	 1.0 2.0	 μA μA
Overcurrent Shutdown Threshold (Source)	IsdSrc	V_{CC} = 5 V, VSx = 13.2 V	−2.0	−1.5	−1.1	A
Overcurrent Shutdown Threshold (Sink)	IsdSnk	V_{CC} = 5 V, VSx = 13.2 V	1.1	1.5	2.0	A
Over Current Delay Timer	TdOc		10	25	50	μs
Underload Detection Threshold (Low Side)	IuldLS	V_{CC} = 5 V, VSx = 13.2 V	–	2.5	7.5	mA
Underload Detection Threshold (High Side)	IuldHS	V_{CC} = 5 V, VSx = 13.2 V	−7.5	−2.5	–	mA
Underload Detection Delay Time	TdUld	V_{CC} = 5 V, VSx = 13.2 V	200	350	600	μs
Body Diode Forward Voltage	IbdFwd	If = 500 mA	–	0.9	1.3	V
DRIVER OUTPUT SWITCHING CHARACTERISTICS						
High Side Turn On Time	ThsOn	Vs = 13.2 V, R_{load} = 70 Ω	–	120	165	μs
High Side Turn Off Time	ThsOff	Vs = 13.2 V, R_{load} = 70 Ω	–	20	45	μs
Low Side Turn On Time	TlsOn	Vs = 13.2 V, R_{load} = 70 Ω	–	120	165	μs
Low Side Turn Off Time	TlsOff	Vs = 13.2 V, R_{load} = 70 Ω	–	35	75	μs
High Side Rise Time	ThsTr	Vs = 13.2 V, R_{load} = 70 Ω	10	30	50	μs
High Side Fall Time	ThsTf	Vs = 13.2 V, R_{load} = 70 Ω	10	30	50	μs
Low Side Rise Time	TlsTr	Vs = 13.2 V, R_{load} = 70 Ω	10	30	50	μs
Low Side Fall Time	TlsTf	Vs = 13.2 V, R_{load} = 70 Ω	10	30	50	μs
High Side Off to Low Side On Non−Overlap Time	ThsOffLsOn	Vs = 13.2 V, R_{load} = 70 Ω	5	–	–	μs

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.) (continued)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
DRIVER OUTPUT SWITCHING CHARACTERISTICS						
Low Side Off to High Side On Non−Overlap Time	TlsOffHsOn	Vs = 13.2 V, R_{load} = 70 Ω	5	–	–	μs
PWM High to High Side On Time	ThsOnPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	120	165	μs
PWM Low to High Side Off Time	ThsOffPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	20	45	μs
PWM High to Low Side On Time	TlsOnPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	120	165	μs
PWM Low to Low Side Off Time	TlsOffPWM	Vs = 13.2 V, R_{load} = 70 Ω	–	35	75	μs
THERMAL RESPONSE						
Thermal Warning	Twr	(Note 3)	120	140	170	°C
Thermal Warning Hysteresis	TwHy	(Note 3)	–	20	–	°C
Thermal Shutdown	Tsd	(Note 3)	150	175	200	°C
Thermal Shutdown Hysteresis	TsdHy	(Note 3)	–	20	–	°C
LOGIC INPUTS − EN, SI, SCLK, CSB, PWM1, PWM2						
Input Threshold High Low	VthInH VthInL		2.0 –	– –	– 0.6	V V
Input Hysteresis − SI, SCLK, CSB, PWM1, PWM2	VthInHys		50	150	300	mV
Input Hysteresis − EN	VthENHys		150	400	800	mV
Pull−down Resistance − EN, SI, SCLK, PWM1, PWM2	Rpdx	EN = SI = SCLK = V_{CC}	50	125	200	kΩ
Pull−up Resistance − CSB	RpuCSB	CSB = 0 V	50	125	250	kΩ
Input Capacitance	Cinx	(Note 3)	–	–	15	pF
LOGIC OUTPUT − SO						
Output High	VsoH	ISOURCE = −1 mA	V_{CC} − 0.6	–	–	V
Output Low	VsoL	ISINK = 1.6 mA	–	–	0.4	V
Tri−state Leakage	ItriStLkg	CSB = 5 V	−5	–	5	μA
Tri−state Output Capacitance	ItriStCout	CSB = V_{CC}, 0 V < V_{CC} < 5.25 V (Note 3)	–	–	15	pF

ELECTRICAL CHARACTERISTICS

(−40°C ≤ T_J ≤ 150°C, 5.5 V ≤ VSx ≤ 40 V, 3.15 V ≤ V_{CC} ≤ 5.25 V, EN = V_{CC}, unless otherwise specified.) (continued)

Characteristic	Symbol	Conditions	Timing Charts #	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE							
SCLK Frequency	Fclk		–	–	–	5.0	MHz
SCLK Clock Period	TpClk	V_{CC} = 5 V V_{CC} = 3.3 V	 –	200 500	– –	– –	ns
SCLK High Time	TclkH		1	85	–	–	ns
SCLK Low Time	TclkL		2	85	–	–	ns
SCLK Setup Time	TclkSup		3, 4	85	–	–	ns
SI Setup Time	TsiSup		11	50	–	–	ns
SI Hold Time	TsiH		12	50	–	–	ns
CSB Setup Time	TcsbSup		5, 6	100	–	–	ns
CSB High Time	TcsbH	(Note 4)	7	5.0	–	–	μs
SO enable after CSB falling edge	TenSo		8	–	–	200	ns
SO disable after CSB rising edge	TdisSo		9	–	–	200	ns
SO Rise/Fall Time	TsoR/F	Cload = 40 pF (Note 3)	–	–	10	25	ns
SO Valid Time	TsoV	Cload = 40 pF (Note 3) SCLK ↑ to SO 50%	10	–	50	100	ns
EN Low Valid Time	TenL	V_{CC} = 5 V; EN H → L 50% to OUTx turning off 50%	–	10	–	–	μs
EN High to SPI Valid	TenHspiV		–	–	–	100	μs
SRR Delay Between Consecutive Frames	Tsrr	(Note 5)	–	150	–	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Not production tested.
4. This is the minimum time the user must wait between SPI commands.
5. This is the minimum time the user must wait between consecutive SRR requests.

CHARACTERISTIC TIMING DIAGRAMS

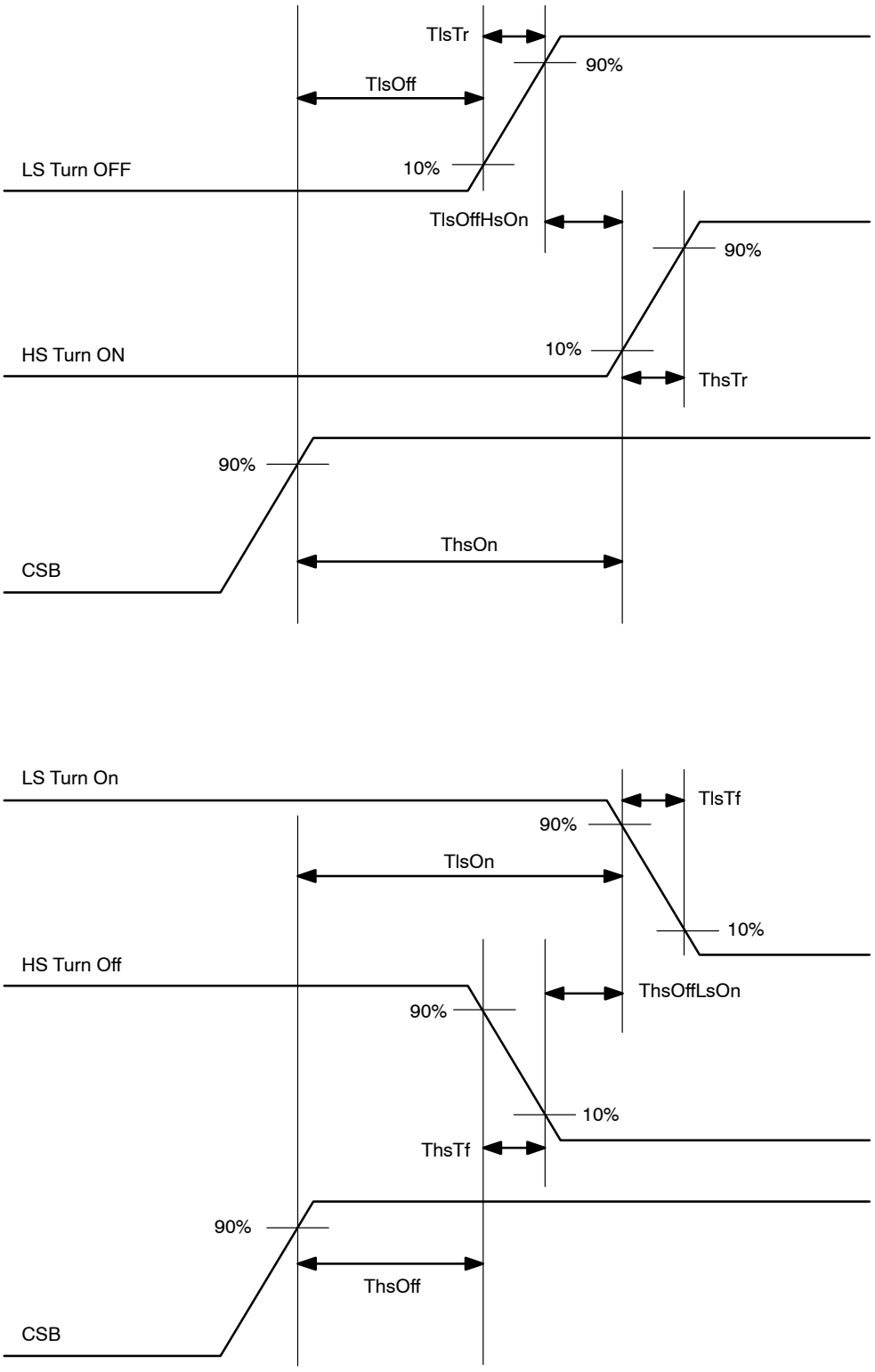


Figure 4. Detailed Driver Timing

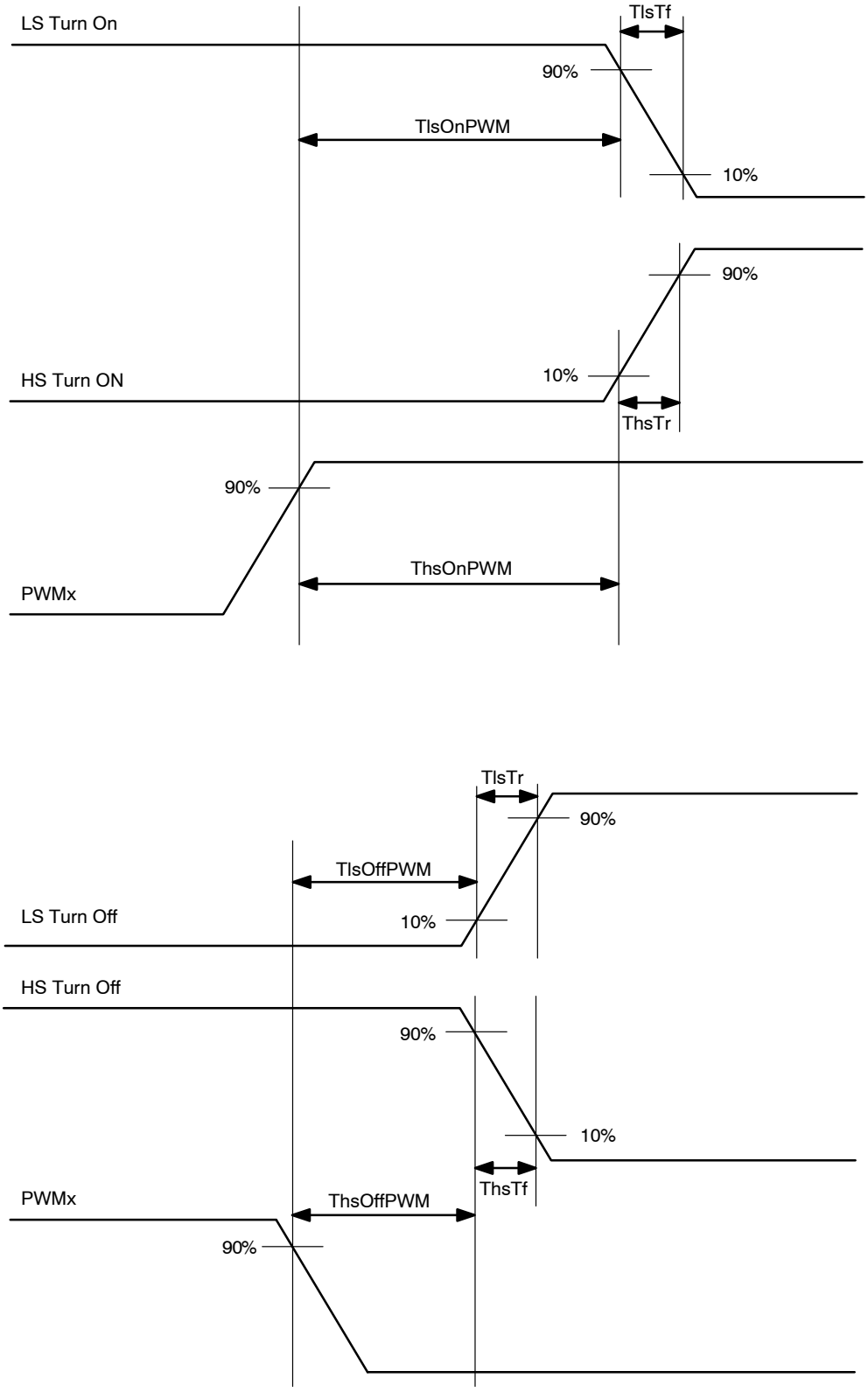


Figure 5. Detailed Driver Timing (OUT1 / OUT2 PWM)

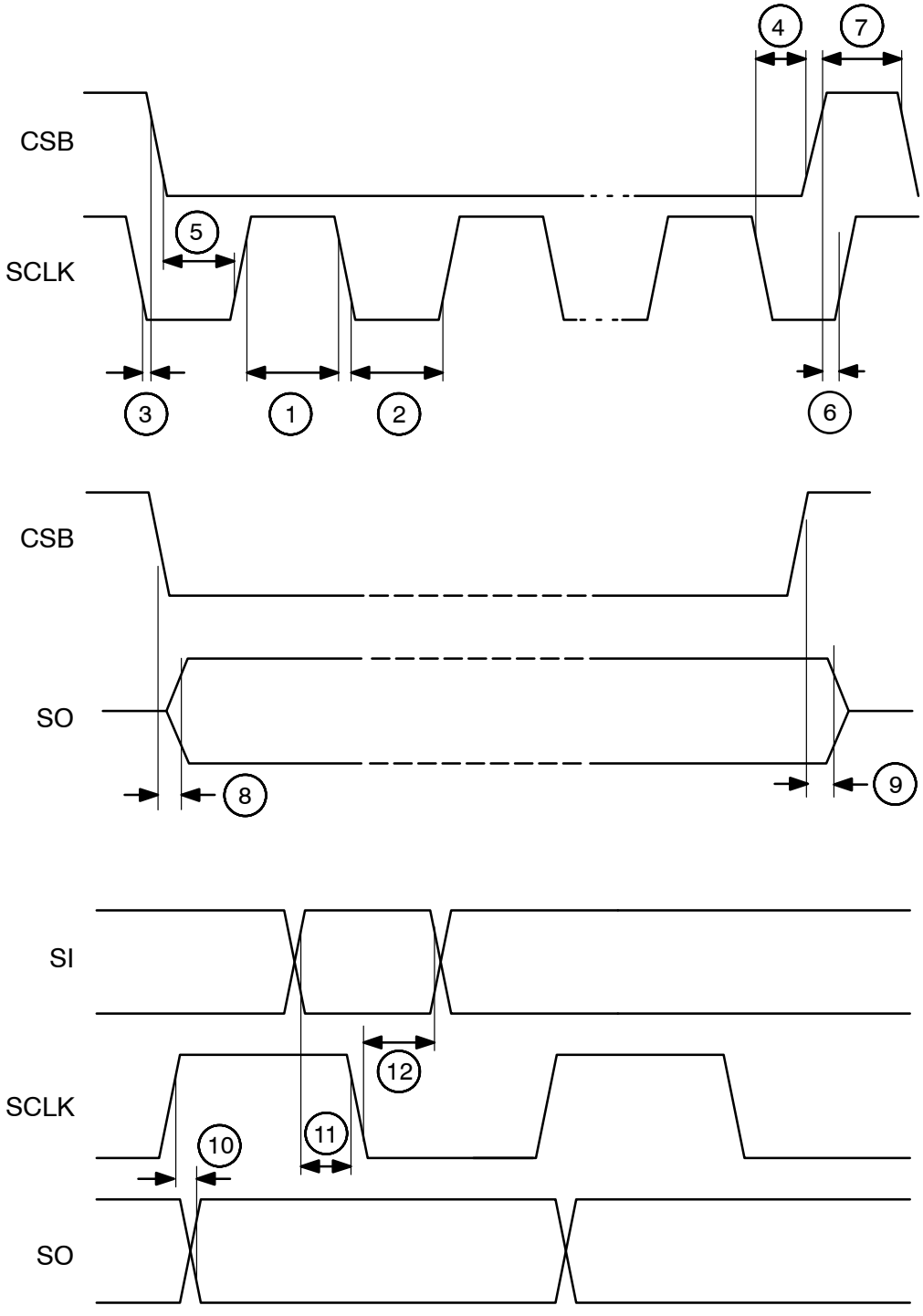


Figure 6. Detailed SPI Timing

TYPICAL CHARACTERISTICS

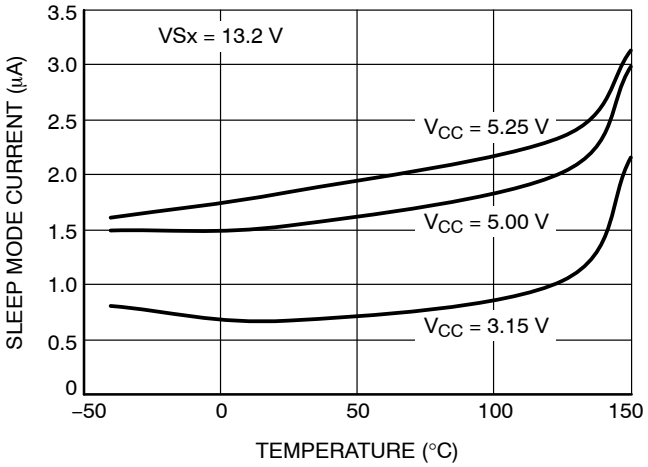


Figure 7. $I_{Q(tot)}$ vs. Temperature

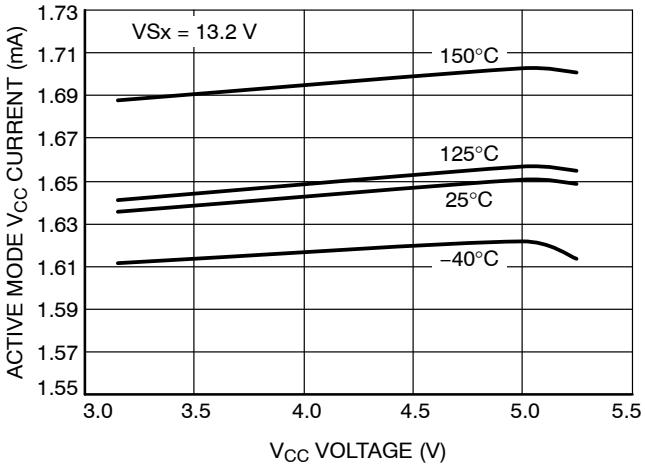


Figure 8. $I_{(Vcc)}$ Active Mode vs. $V_{(Vcc)}$

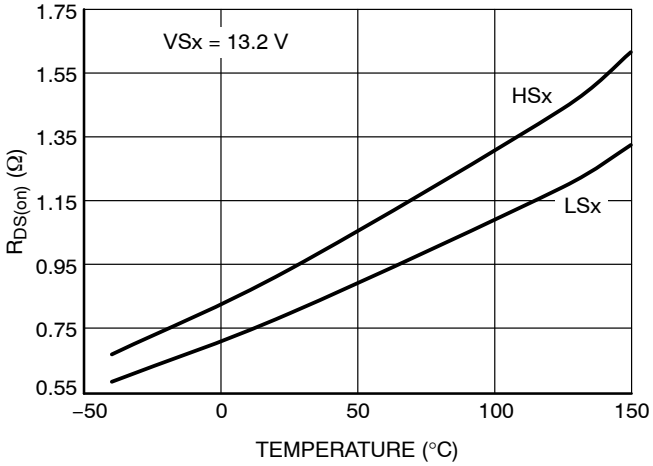


Figure 9. $R_{DS(on)}$ vs. Temperature

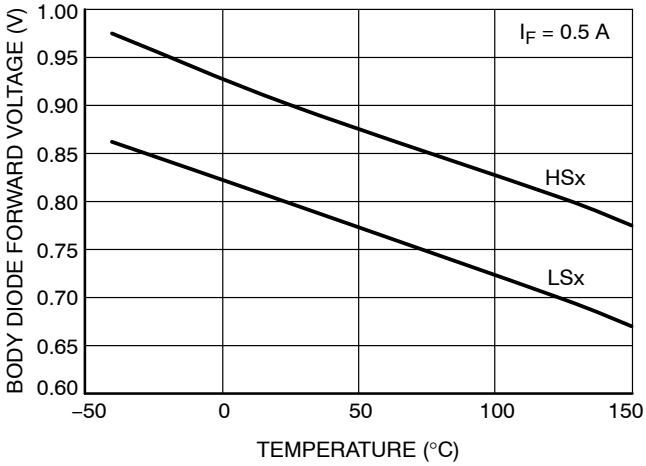


Figure 10. Body Diode Voltage vs. Temperature

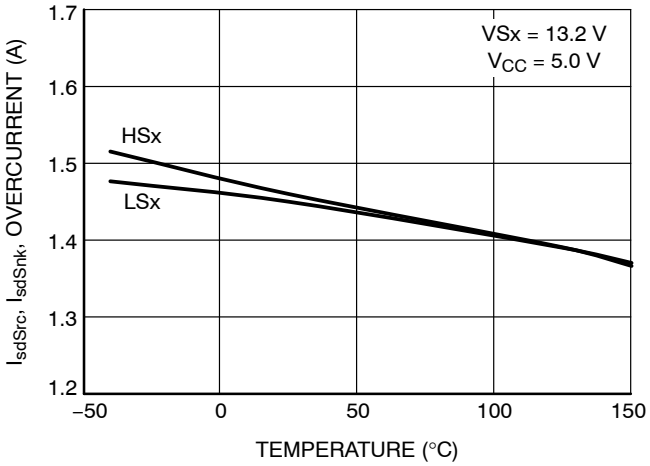


Figure 11. Overcurrent vs. Temperature

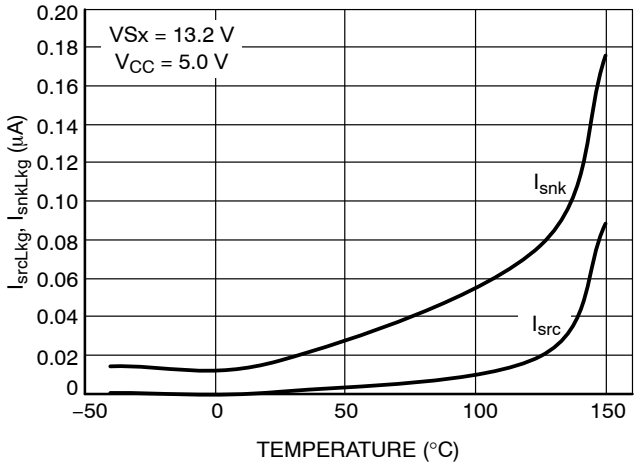


Figure 12. Leakage vs. Temperature

DETAILED OPERATING DESCRIPTION

General Overview

The NCV7725B is comprised of twenty NMOS power drivers. The drivers are arranged as ten half−bridge output channels, allowing for five independent full−bridge configured loads. Output control and status reporting is handled via the SPI (Serial Peripheral Interface) communications port. OUT1 and OUT2 can be controlled with an external PWM signal.

Each output is characterized for a typical 0.5 A DC load and has a maximum 2.0 A surge capability (at VSx = 13.2 V). Maximum allowable junction temperature is 150°C and may constrain the maximum load current and/or limit the number of drivers active at once.

An active−high enable function (EN) allows global control of the outputs and provides a low quiescent current sleep mode when the device is not being utilized. An internal pull−down resistor is provided on the input to ensure the device enters sleep mode if the input signal is lost.

After EN transitions from low to high, the V_{CC} POR cycle will proceed and bring the device into normal operation. The device configuration registers can then be programmed via SPI. Bringing EN low clears all registers (no configuration or status data is stored), disables the drivers, and enters sleep mode.

SPI Communication

16−bit full duplex SPI communication has been implemented for device configuration, driver control, and reading the status data. In addition to the 16−bit status data, a pseudo−bit (PRE_15) can also be retrieved from the SO output.

The device must be enabled (EN = H) for SPI communication. The SPI inputs are TTL compatible and the SO output high level is defined by the applied V_{CC}. The active−low CSB input has a pull−up resistor and the remaining inputs have pull−down resistors to bias them to known states when SPI communication is inactive.

The latched thermal shutdown (TSD) status bit PRE_15 is available on SO until the first rising SCLK edge after CSB goes low. The following conditions must be met for a valid TSD read to be captured:

1. SCLK and SI are low before the CSB cycle;
2. CSB transitions from high to low;
3. CSB setup time (TcsbSup: Figure 6, #5) is satisfied.

Figure 13 shows the SPI communication frame format, and Tables 1 and 2 define the command input and diagnostic status output bits.

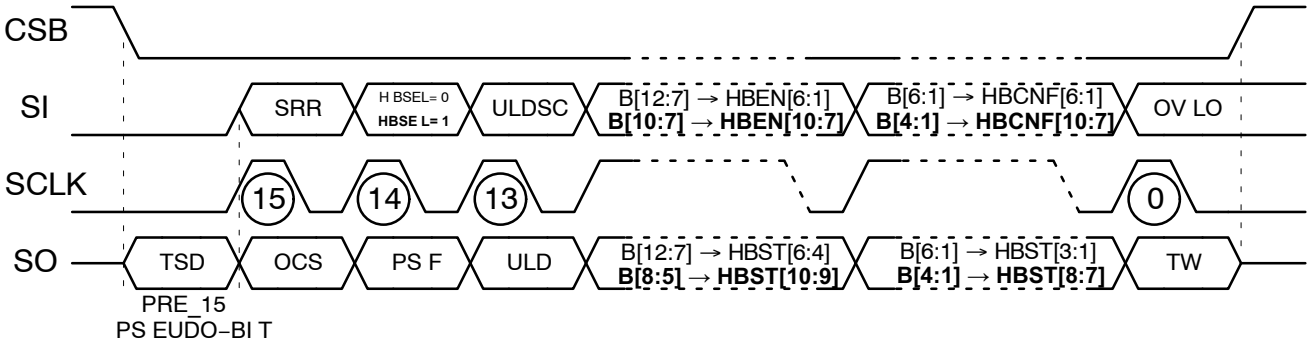


Figure 13. SPI Communication Frame Format

Communication is implemented as follows and is also illustrated in Figures 13 and 15:

1. SI and SCLK are set low before the CSB cycle.
2. CSB goes low to begin a serial data frame; pseudo−bit PRE_15 is immediately available at SO.
3. SI data is shifted in on every rising edge of SCLK, starting with the most significant bit (MSB), SRR.
4. SI data is recognized on every falling edge of the SCLK.
5. Current SO data is simultaneously shifted out on every rising edge of SCLK, starting with the MSB (OCS).
6. CSB goes high to end the frame and SO becomes tri−state.
7. The last 16 bits clocked into SI are transferred to the device's data register if no frame error is detected, otherwise the entire frame is ignored and the previous input data is preserved.

Table 1. SPI COMMAND INPUT DEFINITIONS

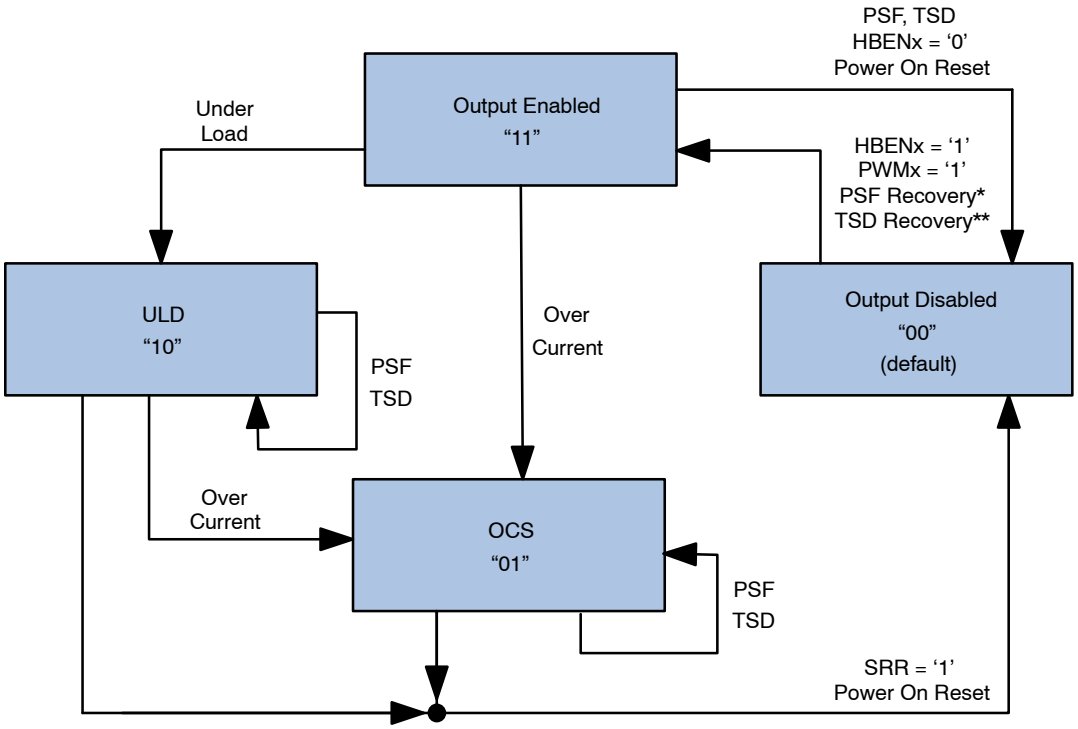
Channels 10 – 7 (Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	Status Reset per **HBSEL**
14	HBSEL	Channel Group Select	1 = HB [10:7]	1 = HB [10:7] | 0 = HB [6:1]
13	ULDSC	Underload Shutdown Control	1 = Enabled	Enabled per **HBSEL**; Per Half−Bridge Operation
12	X	Not Used	–	–
11				
10	HBEN10	Enable Half−Bridge 10	0 = Hi−Z 1 = Enabled	Per Half−Bridge
9	HBEN9	Enable Half−Bridge 9		
8	HBEN8	Enable Half−Bridge 8		
7	HBEN7	Enable Half−Bridge 7		
6	X	Not Used	–	–
5				
4	HBCNF10	Configure Half−Bridge 10	0 = LS On, HS Off 1 = LS Off, HS On	Per Half−Bridge
3	HBCNF9	Configure Half−Bridge 9		
2	HBCNF8	Configure Half−Bridge 8		
1	HBCNF7	Configure Half−Bridge 7		
0	OVLO	VSx Overvoltage Lockout	1 = Enabled	Global Lockout
Channels 6 – 1 (Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**
15	SRR	Status Register Reset**	1 = Reset	Status Reset per **HBSEL**
14	HBSEL	Channel Group Select	0 = HB [6:1]	1 = HB [10:7] | 0 = HB [6:1]
13	ULDSC	Underload Shutdown Control	1 = Enabled	Enabled per **HBSEL**; Per Half−Bridge Operation
12	HBEN6	Enable Half−Bridge 6	0 = Hi−Z 1 = Enabled	Per Half−Bridge
11	HBEN5	Enable Half−Bridge 5		
10	HBEN4	Enable Half−Bridge 4		
9	HBEN3	Enable Half−Bridge 3		
8	HBEN2	Enable Half−Bridge 2		
7	HBEN1	Enable Half−Bridge 1		
6	HBCNF6	Configure Half−Bridge 6	0 = LS On, HS Off 1 = LS Off, HS On	Per Half−Bridge
5	HBCNF5	Configure Half−Bridge 5		
4	HBCNF4	Configure Half−Bridge 4		
3	HBCNF3	Configure Half−Bridge 3		
2	HBCNF2	Configure Half−Bridge 2		
1	HBCNF1	Configure Half−Bridge 1		
0	OVLO	VSx Overvoltage Lockout	1 = Enabled	Global Lockout

*All command input bits are set to 0 at V_{CC} power−on reset.
**Latched faults are cleared and outputs can be re−programmed if no fault exists after SRR asserted.

Table 2. SPI STATUS OUTPUT DEFINITIONS

Channels 10 – 7 (If Previous Input Bit # 14 = 1)				
Bit#	**Name**	**Function**	**Status***	**Scope**
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification and Global Operation
13	ULD	Underload Detect	1 = Fault	Notification per **HBSEL**; Per Half−Bridge Operation
12	X	Not Used	–	–
11				
10				
9				
8	HBST10 [1:0]	Half−Bridge 10 Output Status	0x00b – Output Disabled 0x01b – OCS 0x10b – ULD 0x11b – Output Enabled	Per Half−Bridge
7				
6	HBST9 [1:0]	Half−Bridge 9 Output Status		
5				
4	HBST8 [1:0]	Half−Bridge 8 Output Status		
3				
2	HBST7 [1:0]	Half−Bridge 7 Output Status		
1				
0	TW	Thermal Warning	1 = Fault	Global Notification; Per Half−Bridge Operation
Channels 6 – 1 (If Previous Input Bit # 14 = 0)				
Bit#	**Name**	**Function**	**Status***	**Scope**
PRE_15	TSD	Latched Thermal Shutdown	1 = Fault	Global Notification; Per Half−Bridge Operation
15	OCS	Latched Overcurrent Shutdown	1 = Fault	
14	PSF	VS1 and/or VS2 Undervoltage or Overvoltage	1 = Fault	Global Notification; Global Operation
13	ULD	Underload Detect	1 = Fault	Global Notification; Per Half−Bridge Operation
12	HBST6 [1:0]	Half Bridge 6 Output Status	0x00b – Output Disabled 0x01b – OCS 0x10b – ULD 0x11b – Output Enabled	Per Half−Bridge
11				
10	HBST5 [1:0]	Half Bridge 5 Output Status		
9				
8	HBST4 [1:0]	Half Bridge 4 Output Status		
7				
6	HBST3 [1:0]	Half Bridge 3 Output Status		
5				
4	HBST2 [1:0]	Half Bridge 2 Output Status		
3				
2	HBST1 [1:0]	Half Bridge 1 Output Status		
1				
0	TW	Thermal Warning	1 = Fault	Global Notification; Per Half−Bridge Operation

*All status output bits are set to 0 at Vcc power−on reset (POR).
HBSTx[1:0] bits are priority encoded to provide the status information of each of the half−bridge outputs. Figure 14 shows the priority encoding state diagram for the HBSTx[1:0] bits.



*PSF Recovery: VSx rising above the undervoltage threshold or falling below the overvoltage threshold (OVLO = 1)
**TSD Recovery: Sending SRR after junction temperature has fallen below the thermal shutdown threshold

Figure 14. SO HBSTx [1:0] Priority Encoding State Diagram

Priority Encoding

If an under load event precedes an over current event on the same half−bridge, the device will report HBSTx = '10' and then HBSTx = '01' as shown in Figure 14. An over current event preceding an under load event will report HBSTx = '01' since there is no direct path from the OCS state to the ULD state. Thus an over current shutdown fault must be cleared before an underload fault is reported on the same half−bridge.

Frame Error Detection

The NCV7725B employs frame error detection to help ensure input data integrity. SCLK is compared to an *n x 8* bit counter and a valid frame (CSB H−L−H cycle) has integer multiples of 8 SCLK cycles. For the first 16 bits shifted into SI, SCLK is compared to a modulo16 counter (n = 2), and SCLK is compared to a modulo 8 counter (n = 1, 2, ...m) thereafter. This variable modulus allows for daisy chain operation with devices using different word lengths.

The last 16 bits clocked into SI are transferred to the NCV7725B's data register if no frame error is detected, otherwise the entire frame is ignored and the previous input data is preserved.

Daisy Chain Operation

Daisy chain operation is possible with multiple 16−bit and 8−bit devices that have a compatible SPI protocol. The clock phase and clock polarity with respect to the data for all the devices in the chain must be the same as the NCV7725B.

CSB and SCLK are parallel connected to every device in the chain while SO and SI are series connected between each device. The master's MOSI is connected to the SI of the first device and the first device's SO is connected to the next device's SI. The SO of the final device in the chain is connected to the master's MISO.

The hardware configuration for the NCV7725B daisy chained with an 8−bit SPI device is shown in Figure 15. A 24−bit frame made of 16−bit word 'A' and 8−bit word 'B' is sent from the master. Command word B is sent first followed by word A. The master simultaneously receives status word B first followed by word A. The progression of data from the MCU through the sequential devices is illustrated in Figure 15.

Compliance with the illustrated frame format is required for proper daisy chain operation. Situations should be avoided where an incorrect multiple of 8 bits is sent to the devices, but the frame length does not cause a frame error in the devices. For example, the word order could be inadvertently interleaved or reversed. Invalid data is accepted by the NCV7725B in such scenarios and possibly by other devices in the chain, depending on their frame error implementation. Data is received as a command by the device at the beginning of the chain, but the device at the end of the chain may receive status data from the preceding device as a command.

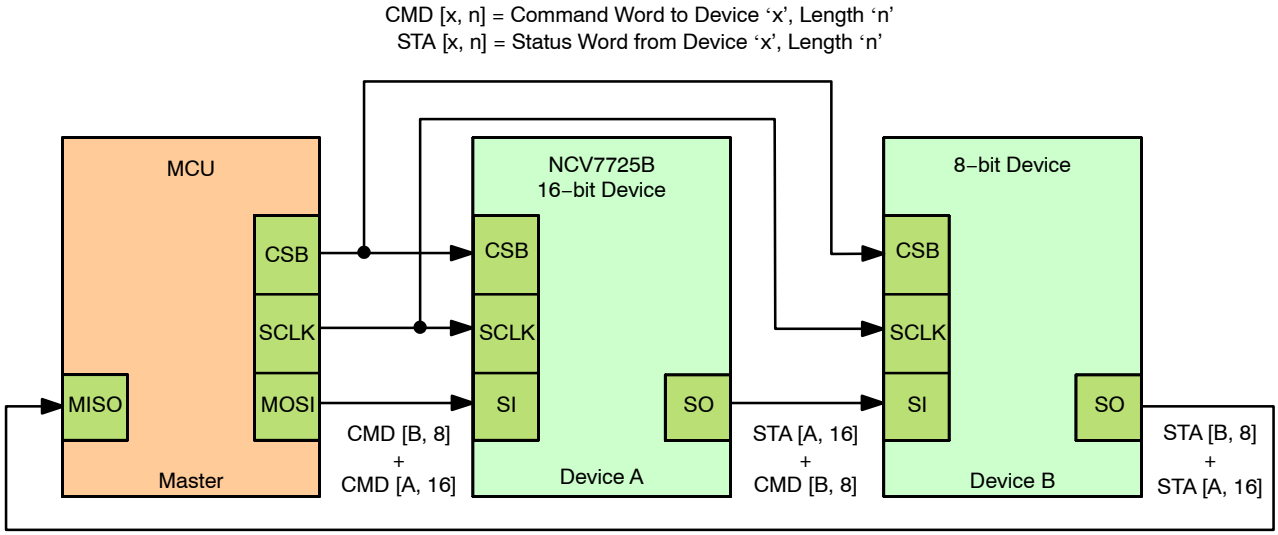


Figure 15. Daisy Chain Configuration

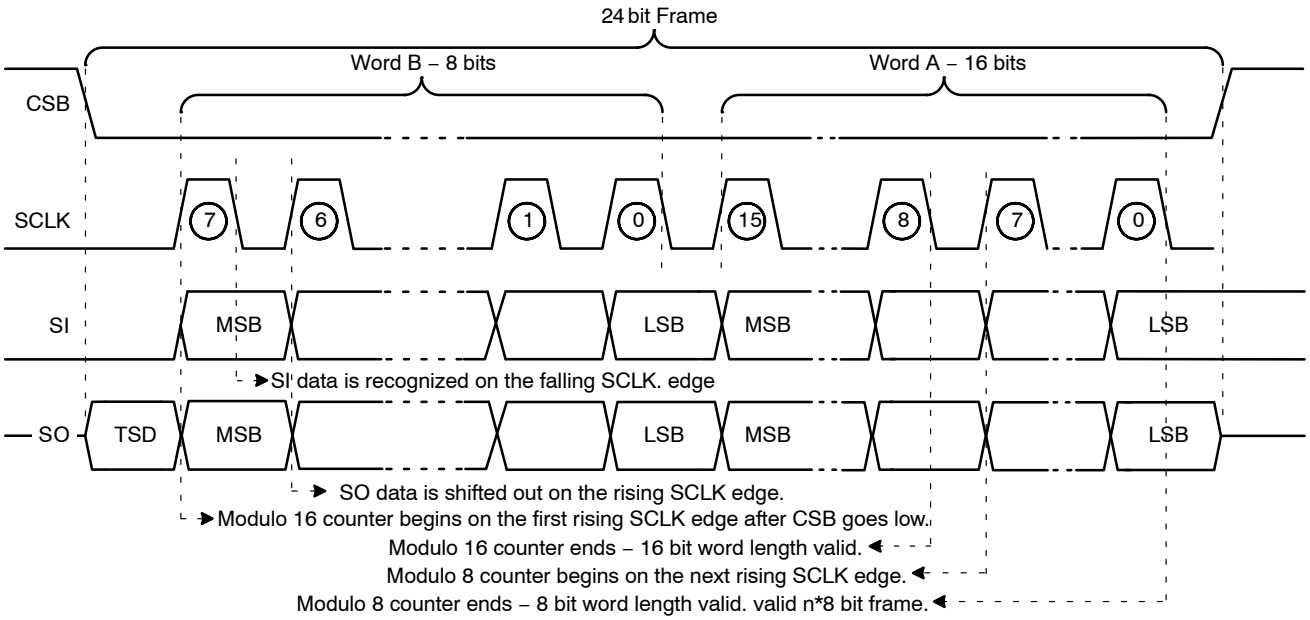


Figure 16. Daisy Chain – 24 bit Frame Format

TSD Bit in Daisy Chain Operation

The SO frame is designed to allow TSD status retrieval in a daisy chain configuration using NCV7725B or other devices with identical SPI functionality. The TSD status bit is OR’d with SI and then multiplexed with the device’s usual status data (Figure 17).

CSB is held high and SI and SCLK are held low by the master before the start of the SPI frame. TSD status is immediately available as bit PRE_15 at SO (SO = TSD) when CSB goes low to begin the frame. The usual status data (SO = STA) becomes available after the first rising SCLK edge.

The TSD status automatically propagates through the chain from the SO output of the previous device to the SI input of the next. This is shown in Figures 18 and 19, first without a TSD fault in either device (Figure 18), and then subsequently with a latched TSD fault (TSD = 1) in device “A” propagating through to device “B” (Figure 19).

Since the TSD status of any device propagates automatically through the entire chain, it is not possible to determine which device (or devices) has a fault (TSD = 1). The usual status data from each device will need to be examined to determine where a fault (or faults) may exist.

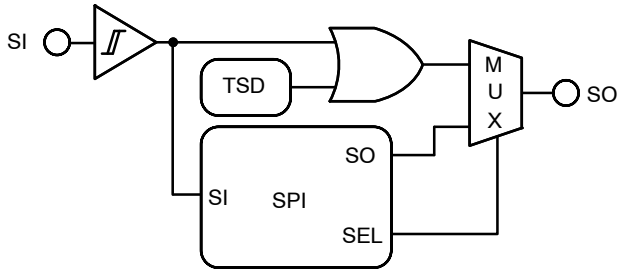


Figure 17. TSD SPI Link

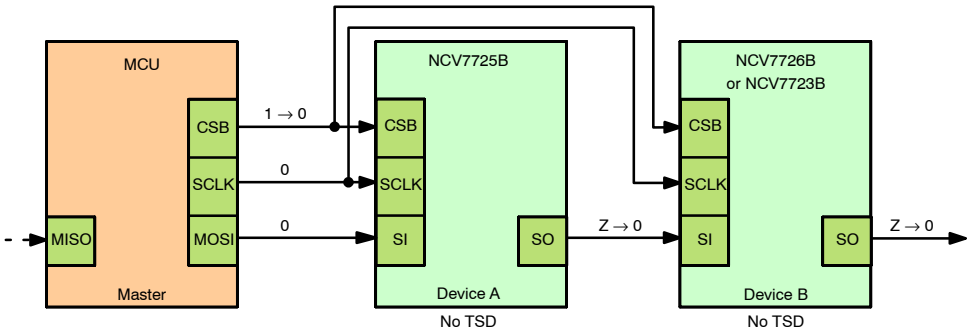


Figure 18. Daisy Chain Without TSD Fault

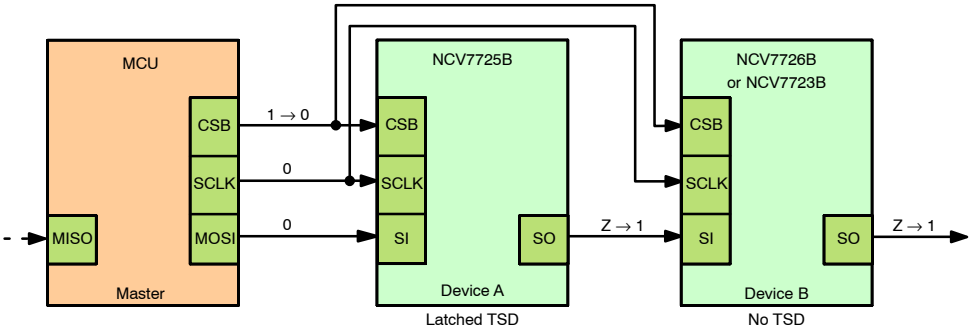


Figure 19. Daisy Chain With TSD Fault

Power Up/Down Control

The V_{CC} supply input powers the device's logic core. A V_{CC} power−on reset (POR) function provides controlled power−up/down. V_{CC} POR initializes the command input and status output registers to their default states (0x00), and ensures that the bridge output and SO drivers maintain Hi−Z as power is applied. SPI communication and normal device operation can proceed once V_{CC} rises above the POR threshold and EN remains high.

The VS1 and VS2 supply inputs power their respective output drivers (refer to Figure 2 and the PIN FUNCTION DESCRIPTION). The VSx inputs are monitored to ensure that the supply stays within the recommended operating range. If the VSx supply moves into either of the VS undervoltage or overvoltage regions, the output drivers are switched to Hi−Z but command and status data is preserved. Output drivers will remain on if OVLO = 0 during an overvoltage condition.

Driver Control

The NCV7725B has the flexibility to control each half−bridge driver channel via SPI. Actual driver output state is determined by the command input and the current fault status bits.

The channels are divided into two groups and each group is selected by the HBSEL input bit (see Table 1). High−side (HSx) and low−side (LSx) drivers of the same channel cannot be active at the same time, and non−overlap delays are imposed when switching between HSx and LSx drivers in the same channel, preventing current shoot−through.

After the device has powered up and the drivers are allowed to turn on, the drivers remain on until commanded off via SPI or until a fault condition occurs.

PWM Control

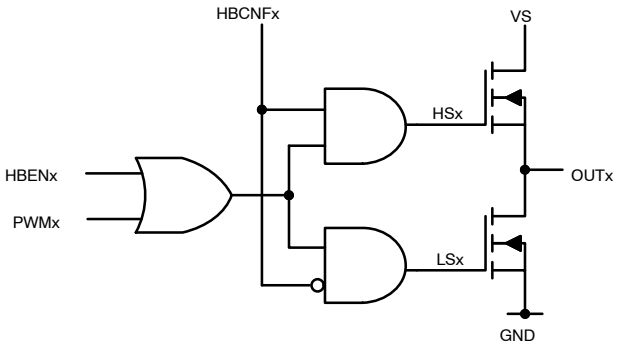
Outputs 1 and 2 can be controlled in two ways: through normal SPI control (see Table 1) or from an external PWM signal. OUT1 can be turned on/off using the HBEN1 bit or applying a logic level signal to pin 17 (PWM1). OUT2 can be turned on/off using the HBEN2 bit or applying a logic level signal to pin 18 (PWM2). Simplified logic functions are shown below in Figure 20.

PWM Example: Turn on OUT1 High Side

To use OUT1 High Side with external PWM control, perform the following steps:

1. Send command 0b0000000000000010 (0x0002)
   - Configures OUT1 to High Side (HBCNF1)
   - Disables OUT1 SPI Enable (HBEN1)
2. Apply logic level PWM signal to PWM1

To use OUT1 Low Side with external PWM, set the HBCNF1 bit to 0 during step 1.



PWMx	HBENx	HBCNFx	HSx	LSx	OUTx
0	0	x	OFF	OFF	Z
x	1	0	OFF	ON	Low
x	1	1	ON	OFF	High
1	x	0	OFF	ON	Low
1	x	1	ON	OFF	High

Figure 20. PWM Control Logic

DIAGNOSTICS, PROTECTIONS, STATUS REPORTING AND RESET

Overview

The NCV7725B employs diagnostics designed to prevent destructive overstress during a fault condition. Diagnostics are classified as either supervisory or protection functions (Table 3). Supervisory functions provide status information about device conditions. Protection functions provide status information and activate fault management behaviors. Diagnostics resulting in output shutdown and latched status may depend on a qualifier and may require user intervention for output recovery and status memory clear. Diagnostics resulting in output lockout and non−latched status (VSOV or VSUV) may recover and clear automatically. Output configurations can be changed during output lockout. Outputs assume the new configurations or resume the previous configurations when an auto−recover fault is resolved. Table 4 shows output states during faults and output recovery modes, and Table 5 shows the status memory and memory clear modes.

Table 3. DIAGNOSTIC CLASSES AND FUNCTIONS

Name	Class	Function
TSD	Protection	Thermal Shutdown
OCS	Protection	Overcurrent Shutdown
PSF	Protection	Under/overvoltage Lockout (OVLO = 1)
ULD	Protection	Underload Shutdown
HBSTx[1:0]	Supervisory	Half−Bridge X Output Status
TW	Supervisory	Thermal Warning

Table 4. OUTPUT STATE VS. FAULT AND OUTPUT RECOVERY

Fault	Qualifier	OUTx State	OUTx Recovery	OUTx Recovery Scope
TSD	–	→ Z	Send SRR	Per HBSEL
OCS	–	→ Z	Send SRR	Per HBSEL
PSF – VSOV	OVLO = 1	→ Z → Y_n | Y_{n+1}	Auto*	All Outputs
	OVLO = 0	Unaffected	–	–
PSF – VSUV	–	→ Z → Y_n | Y_{n+1}	Auto*	All Outputs
ULD	ULDSC = 1	→ Z	Send SRR	Per HBSEL
	ULDSC = 0	Unaffected	–	–
TW	–	Unaffected	–	–

*OUTx returns to its previous state (Y_n) or new state (Yn+1) if fault is removed.

Table 5. STATUS MEMORY VS. FAULT AND MEMORY CLEAR

Fault	Qualifier	Status Memory	Memory Clear	Memory Clear Scope
TSD	–	Latched	Send SRR	Per HBSEL
OCS	–	Latched	Send SRR	Per HBSEL
PSF – VSOV	OVLO = X	Non−Latched	Auto*	Global
PSF – VSUV	_	Non−Latched	Auto*	Global
ULD	ULDSC = X	Latched	Send SRR	Per HBSEL
TW	–	Non−Latched	Auto*	Global

*Status memory returns to its no−fault state if fault is removed.

Status Information Retrieval

Current status information as selected by HBSEL is retrieved during each SPI frame. To preserve device configuration and output states, the previous SI data pattern must be sent during the status retrieval frame.

Status information is prevented from being updated during a SPI frame but new status becomes available after CSB goes high at the end of the frame provided the frame did not contain an SRR request. Status information includes both global and per channel fault notification. To determine the channel(s) affected after detecting a global fault, examine driver output status and input configuration.

Status Register Reset – SRR

Sending SRR = 1 clears status memory and re−activates faulted outputs for all channels within an HBSEL group. The previous SI data pattern must be sent with SRR to preserve device configuration and output states.

At the rising edge of CSB, the SRR function is activated and an internal timer (Tsrr) is started. Tsrr is the minimum time the user must wait between consecutive SRR requests. If a fault is still present when SRR is sent, protection will be re−engaged and shutdown will recur. The status registers can also be reset by toggling the EN pin or by VCC power−on reset.

Diagnostics Details

The following sections describe individual diagnostics and behaviors. In each description and illustration, a SPI frame is assumed to always be valid and the SI data pattern sent for HBCNFx and HBENx is the same as the previous frame. Actual results can depend on asynchronous fault events and SPI clock frequency and frame rate.

Undervoltage Lockout

Global Notification, Global Operation

Undervoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Undervoltage hysteresis is provided to ensure clean detection transitions. Undervoltage timing is shown in Figure 21.

Undervoltage at either VSx input turns off all outputs and sets the power supply fail (PSF) status bit. The outputs return to their previously programmed state and the PSF status bit is cleared when VSx rises above the hysteresis voltage level. SPI communication is available and programmed output enable and configuration states are maintained if proper VCC is present during VSx undervoltage. Output enable and configuration states can also be programmed during VSx undervoltage if proper VCC is present, and state changes will take effect as VSx rises above the undervoltage threshold level. VCC undervoltage turns all outputs off and clears the command input and status output registers.

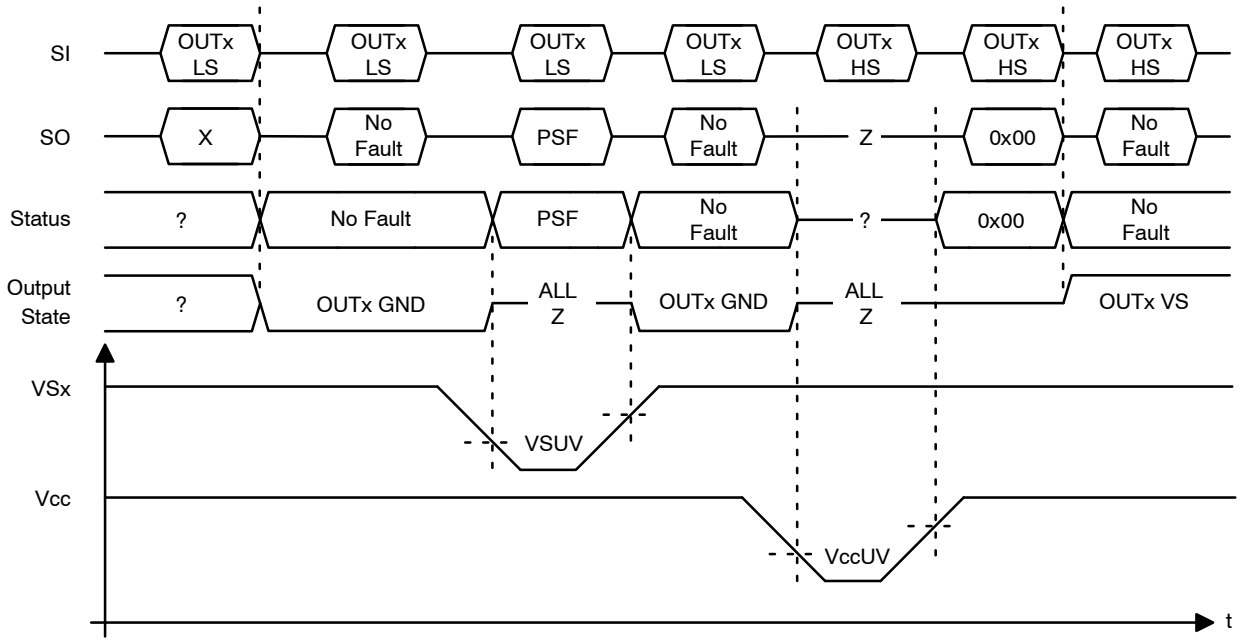


Figure 21. Undervoltage Timing

Overvoltage Lockout

Global Notification, Global Operation

Overvoltage detection and lockout control is provided by monitoring the VS1 and VS2 supply inputs. Hysteresis is provided to ensure clean detection transitions. Overvoltage timing is shown in Figure 22. Overvoltage at either VSx input turns off all outputs if the overvoltage lockout input bit is set (OVLO = 1, HBSEL = X) and sets the power supply fail (PSF) status bit (see Tables 4 and 5). The outputs return to their previously programmed state and the PSF status bit is cleared when VSx falls below the hysteresis voltage level.

Output enable and configuration states can also be programmed during an overvoltage lockout event but will not change state until VSx falls below the overvoltage threshold level.

NOTE: to reduce stress, it is recommended to operate the device with OVLO bit asserted to ensure that the drivers turn off during a load dump scenario. If OVLO = 0 during an overvoltage condition, outputs will remain on and the PSF status bit will be set.

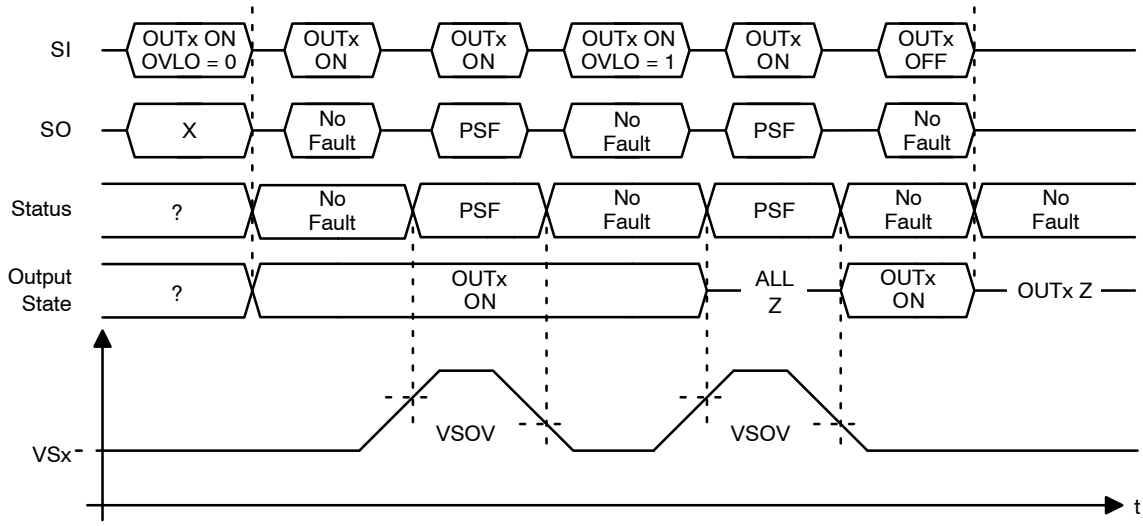


Figure 22. Overvoltage Timing

Overcurrent Shutdown

Global and per Channel Notification per HBSEL Per Half−Bridge Operation

Overcurrent detection and shutdown control is provided by monitoring each HS and LS driver. Overcurrent timing is shown in Figure 23. Overcurrent in either driver starts a channel's overcurrent delay timer (TdOc). If overcurrent exists after the delay, both drivers are latched off and the global overcurrent (OCS) status bit is set. The channel's corresponding HBSTx[1:0] bits are also set to "01" to indicate an OCS fault. Note that OCS fault reporting has priority over other faults as shown in Figure 14. The global OCS bit and individual channel bits are cleared and channels are re−activated by sending SRR = 1 (HBSEL = X).

A persistent overcurrent cause should be resolved prior to re−activation to avoid repetitive stress on the drivers.

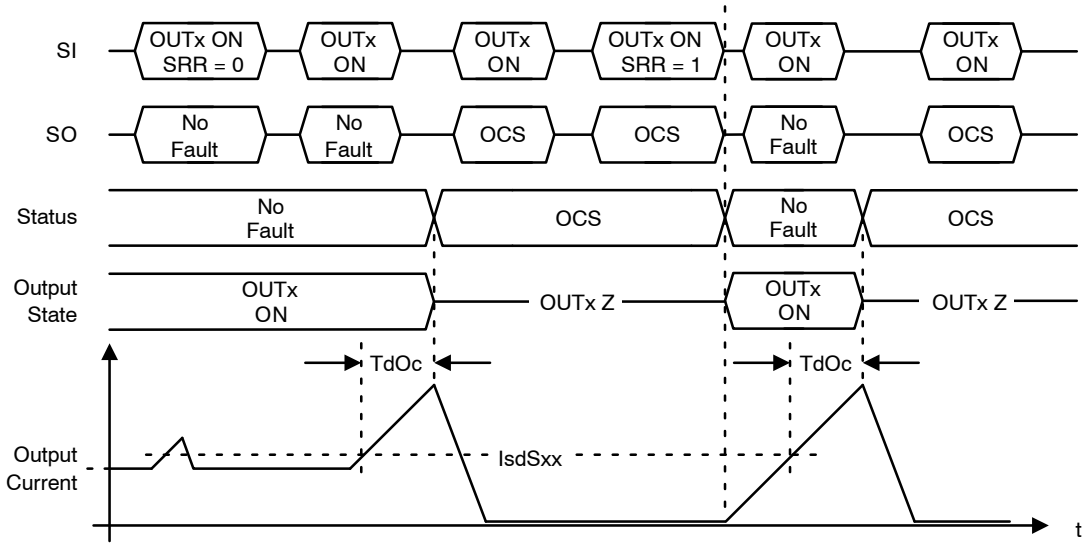


Figure 23. Overcurrent Timing

Underload Shutdown

Global and per Channel Notification per HBSEL
Shutdown Control per HBSEL,
Per Half−Bridge Operation

Underload detection and shutdown control is provided by monitoring each half bridge driver. Underload timing is shown in Figure 24. Underload at any driver starts the global underload delay timer. If underload occurs in another channel after the global timer has been started, the delay for any subsequent underload will be the remainder of the timer.

If underload exists after the global delay timer and if the underload shutdown (ULDSC) command bit is set, both HSand LS drivers are latched off and the global underload (ULD) status bit is set along with the corresponding per channel status bits HBSTx[1:0] set to “10”. Drivers will remain on if the ULDSC input bit is 0 (see Table 4 and 5). The global ULD bit and per channel HBSTx bits are cleared and channels are re−activated by sending SRR = 1 (HBSEL = X).

NOTE: underload may result from a fault (e.g. open−load) condition or normal circuit behavior (e.g. L/R tau). In motor applications it is often desirable to actively brake the motor by turning on both HS or LS drivers in two half−bridge channels which may result in an underload condition as current decays.

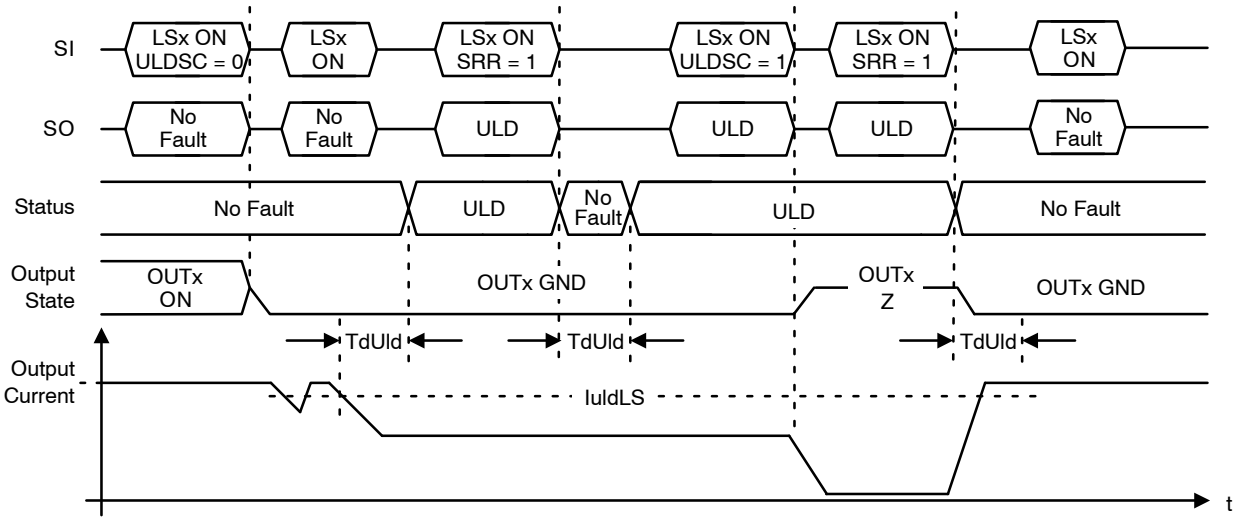


Figure 24. Underload Timing

Thermal Warning and Thermal Shutdown

Global Notification, Per Half−Bridge Operation

Thermal warning (TW) and thermal shutdown (TSD) detection and control are provided for each half−bridge by monitoring the driver pair's thermal sensor. Thermal hysteresis is provided for each of the warning and shutdown functions to ensure clean detection transitions. Software polling of the TW bit allows for avoidance of thermal shutdown since TW notification precedes TSD notification. Thermal warning and shutdown timing is shown in Figure 25.

The TW status bit is set when a half−bridge's sensor temperature exceeds the warning level (T_J > Twr), and the bit is automatically cleared when sensor temperature falls below the warning hysteresis level (T_J < TwHy). A channel's output state is unaffected by TW.

When sensor temperature exceeds the shutdown level (T_J > Tsd), the channel's HS and LS drivers are latched off, the TW bit is/remains set, and the TSD (PRE_15) bit is set. The TSD bit is cleared and all affected channels are re−activated (T_J < TsdHy) by sending SRR = 1.

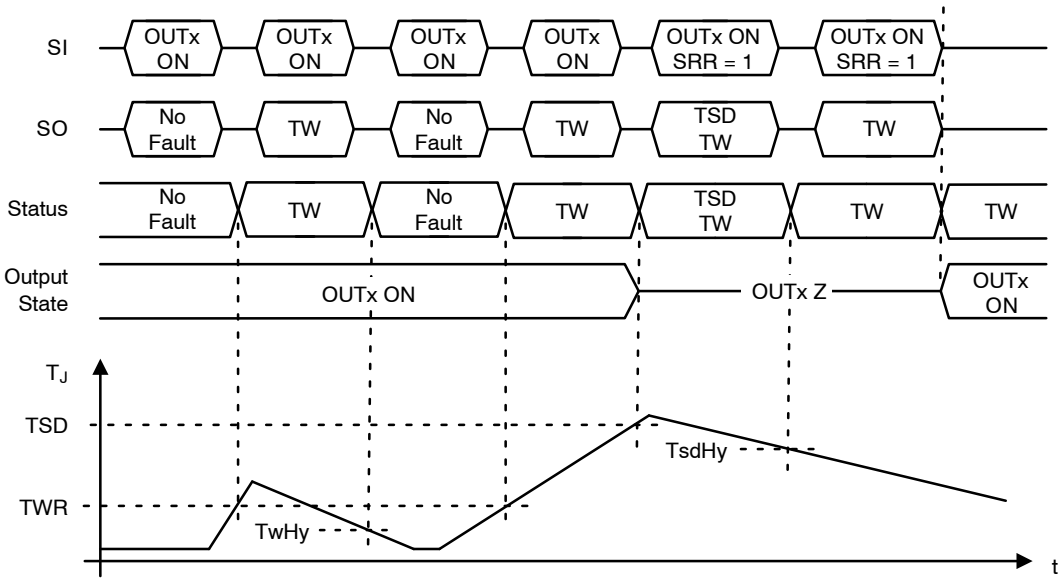


Figure 25. Thermal Warning and Shutdown Timing

The latched thermal shutdown (TSD) information is available on SO after CSB transitions from high to low and before the first rising SCLK edge. The following procedures must be met for a true TSD reading:

1. SCLK and SI are low before the CSB cycle. Violating these conditions will results in an undetermined SPI behavior or/and an incorrect TSD reading.
2. CSB transitioning from high to low.
3. CSB setup time (TcsbSup) is satisfied and the data is captured before the first SCLK rising edge.

THERMAL PERFORMANCE ESTIMATES

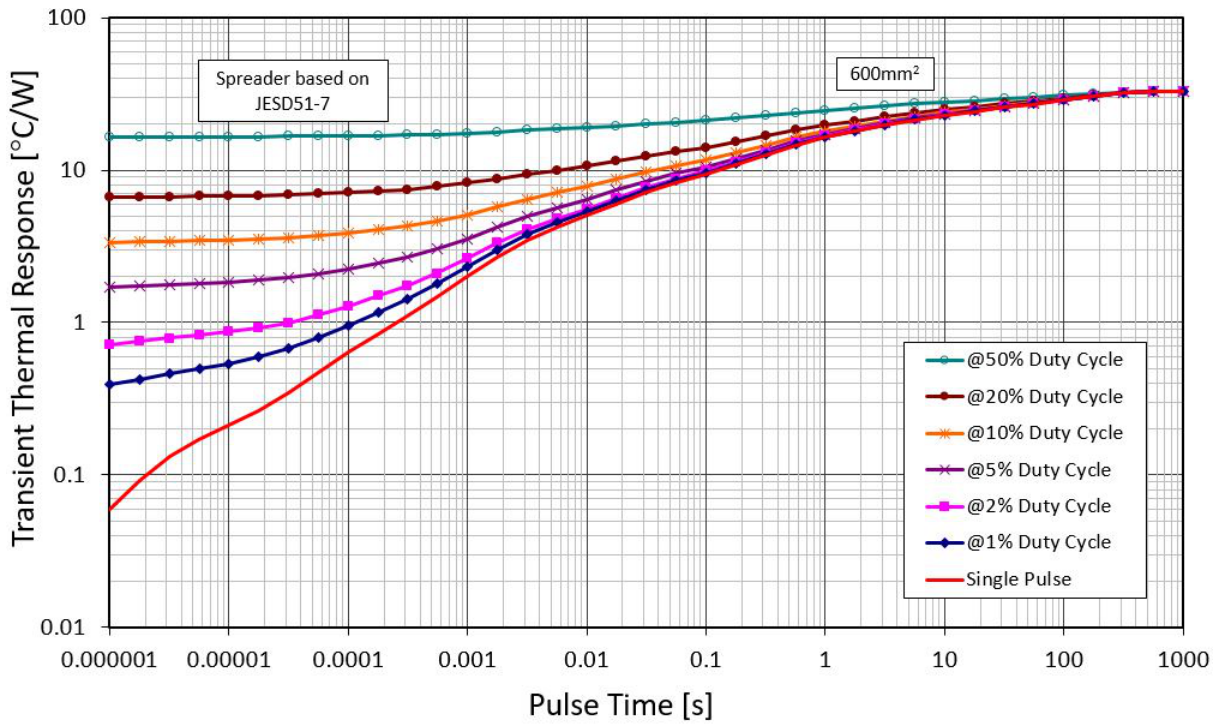


Figure 26. Transient R(t) vs. Pulse Time for 2 oz Spreader

ORDERING INFORMATION

Device	Package	Shipping†
NCV7725DQBR2G	SSOP24 NB EP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

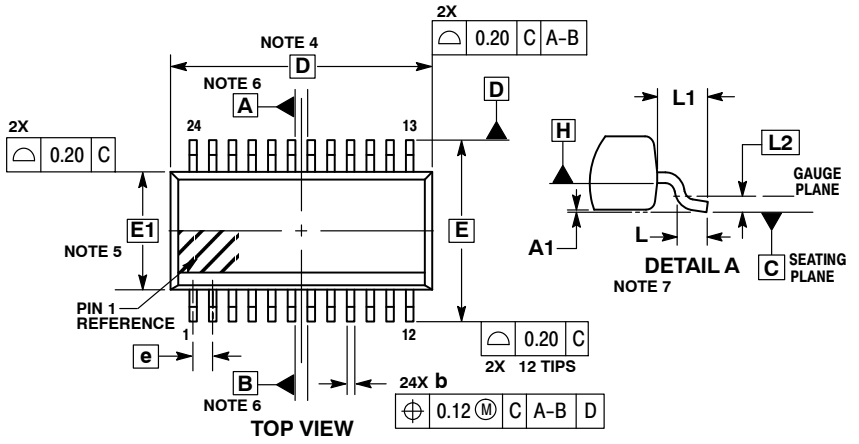
ON Semiconductor®

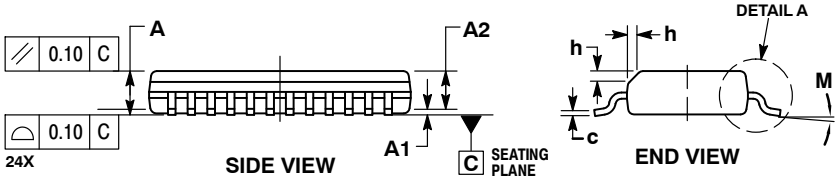


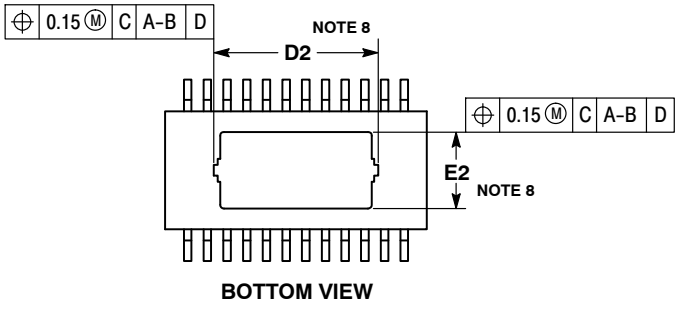
SCALE 1:1

SSOP24 NB EP
CASE 940AK
ISSUE O

DATE 24 APR 2012



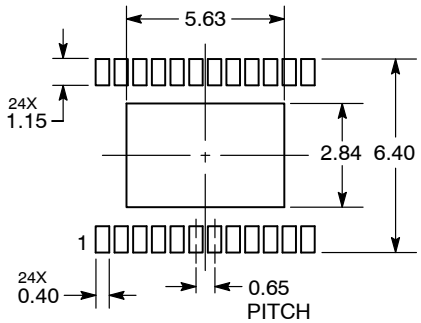




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.10 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. DIMENSION b APPLIES TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. CONTOURS OF THE THERMAL PAD ARE UNCONTROLLED WITHIN THE REGION DEFINED BY DIMENSIONS D2 AND E2.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.70
A1	0.00	0.10
A2	1.10	1.65
b	0.19	0.30
c	0.09	0.20
D	8.64 BSC	
D2	5.28	5.58
E	6.00 BSC	
E1	3.90 BSC	
E2	2.44	2.64
e	0.65 BSC	
h	0.25	0.50
L	0.40	0.85
L1	1.00 REF	
L2	0.25 BSC	
M	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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