NCV78663

Power Ballast and Dual LED Driver for Automotive Front Lighting

The NCV78663 is a single−chip and high efficient smart Power ballast and Dual LED DRIVER designed for automotive front lighting applications like high beam, low beam, daytime running light (DRL), turn indicator, fog light, static cornering, and so on.

The NCV78663 is a best fit for high current LEDs and provides a complete solution to drive two strings up to 60 V, by means of two internal independent buck switch channels, with a minimum of external components.

For each channel, the output current and voltage can be customized according to the application requirements. Diagnostic feature for automotive front lighting is provided on−chip.

The device integrates a voltage booster controller, realizing a unique input current filter with a limited number of externals.

The NCV78663 can be used in stand−alone mode or together with a companion microcontroller allowing maximum flexibility. Depending on the voltage and current of the connected LED string, the LED ballast parameters can be adapted by writing the SPI settings in the device, as such that no hardware changes are required.

Features

- Single Chip Boost−Buck Solution
- Two Independent LED Strings Up to 60 V
- High Overall Efficiency
- Minimum of External Components
- Active Input Filter with Low Current Ripple from Battery
- Integrated Switched Mode Buck Current Regulator
- Two Integrated Buck Switches with 1.4 A Peak Current Capability
- Integrated Boost Controller
- Programmable Input Current Limitation
- Average Current Regulation Through the LEDs
- High Operating Switching Frequencies to Reduce Inductor Sizes
- Integrated PWM Dimming with Wide Frequency Range
- Low EMC Emission for LED Switching and Dimming
- SPI Interface for Optional External μC and Dynamic Control of System Parameters
- This is a Pb−Free Device

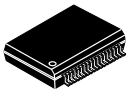
Typical Applications

- High Beam
- Low Beam
- DRL
- Position or Park light
- Turn Indicator
- Fog Light
- Static Cornering

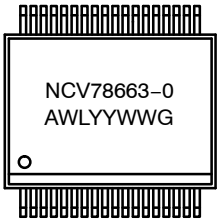
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MARKING DIAGRAM



SSOP36 EP
CASE 940AB



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 36 of this data sheet.

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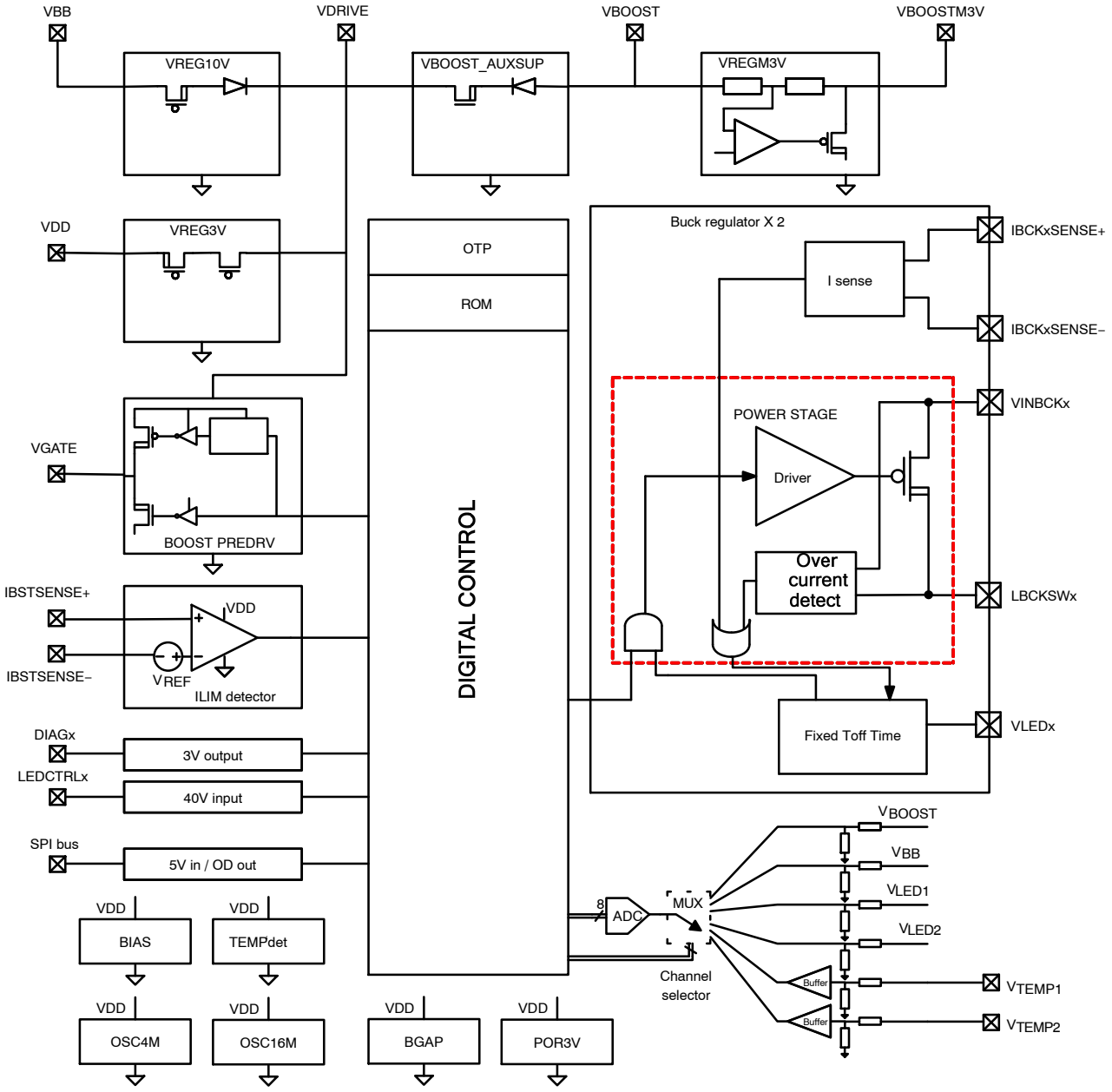
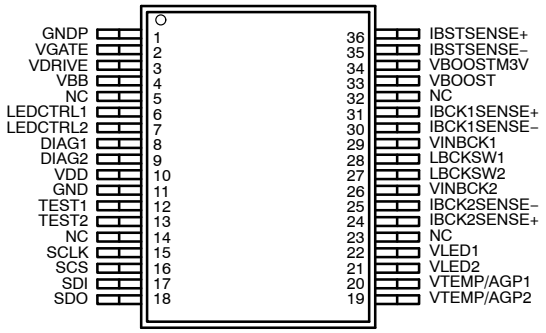


Figure 1. Internal Block Diagram

PACKAGE AND PIN DESCRIPTION



SSOP36

Figure 2. Pin Connections

Table 1. PIN DESCRIPTION

Pin#	Pin Name	IO Type	Function
1	GNDP	ground	Power ground
2	VGATE	MV out	Booster MOSFET gate pre−driver
3	VDRIVE	MV supply	10 V supply
4	VBB	HV supply	Battery supply
5	N.C.		Not used (can be connected to GND)
6	LEDCTRL1	HV IO	LED string 1 enable
7	LEDCTRL2	HV IO	LED string 2 enable
8	DIAG1	LV out	LED string 1 diagnostic output
9	DIAG2	LV out	LED string 2 diagnostic output
10	VDD	LV supply	3 V logic supply
11	GND	Ground	Ground
12	TEST1	LV in	Test (not used in application, must connected to GND)
13	TEST2	LV in	Test (not used in application, must connected to GND)
14	N.C.		Not used (can be connected to GND)
15	SCLK	MV in	SPI clock
16	SCS (CSB)	MV in	SPI chip select (chip select bar)
17	SDI	MV in	SPI data input
18	SDO	MV open−drain	SPI data output
19	VTEMP/AGP2	LV in	LED string 2 temperature feedback input
20	VTEMP/AGP1	LV in	LED string 1 temperature feedback input
21	VLED2	HV in	LED string 2 forward voltage input
22	VLED1	HV in	LED string 1 forward voltage input
23	N.C.		Not used (can be connected to GND)
24	IBCK2SENSE+	HV in	Buck 2 positive sense input
25	IBCK2SENSE−	HV in	Buck 2 negative sense input
26	VINBCK2	HV in	Buck 2 high voltage supply
27	LBCKSW2	HV out	Buck 2 switch output
28	LBCKSW1	HV out	Buck 1 switch output

Table 1. PIN DESCRIPTION

Pin#	Pin Name	IO Type	Function
29	VINBCK1	HV in	Buck 1 high voltage supply
30	IBCK1SENSE−	HV in	Buck 1 negative sense input
31	IBCK1SENSE+	HV in	Buck 1 positive sense input
32	N.C.		Not used (can be connected to GND)
33	VBOOST	HV supply	High voltage feedback input
34	VBOOSTM3V	HV IO	VBOOST−3V output
35	IBSTSENSE−	LV IO	Battery current negative feedback input
36	IBSTSENSE+	LV IO	Battery current positive feedback input

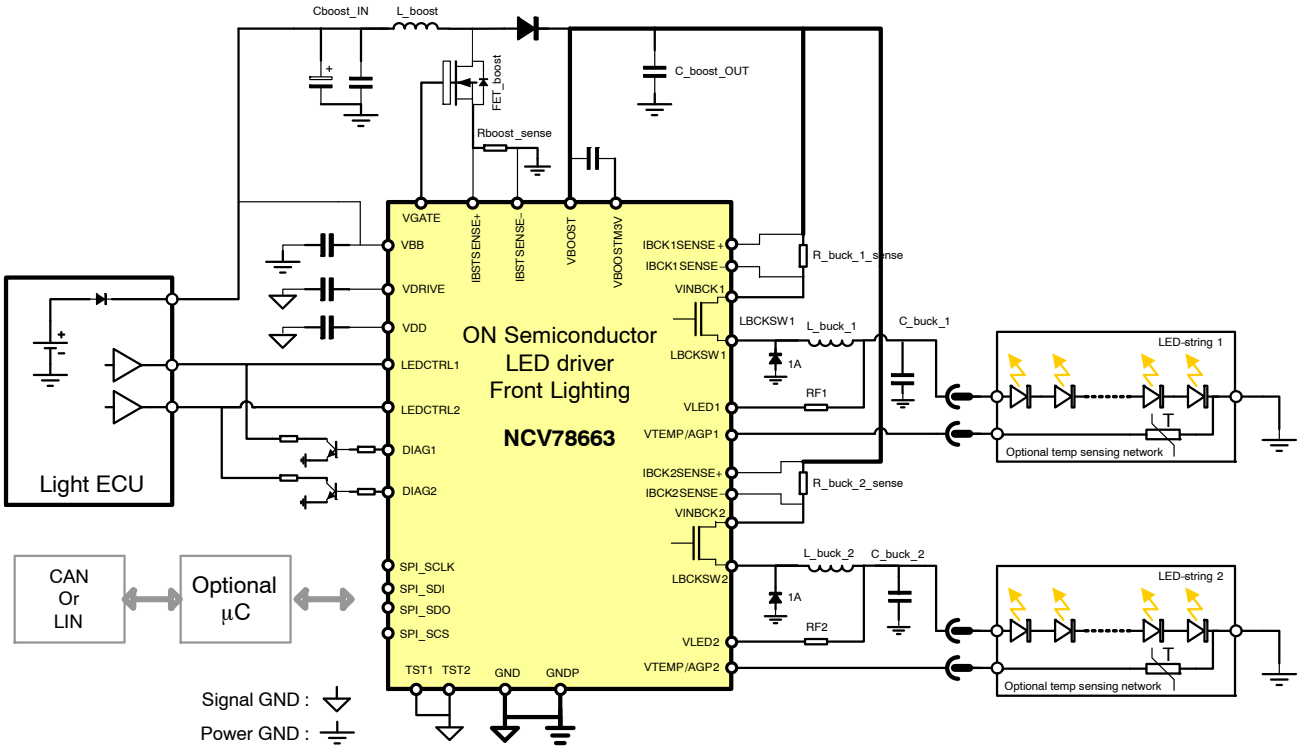


Figure 3. NCV78663 Application Circuit

1. As reported in the application diagram, the device pins TEST1 and TEST2 must be connected to ground.
2. For details about PCB layout, please refer to the dedicated section.
3. RF1 and RF2 resistors typical value is 2.2 kΩ and minimum required value is 1 kΩ. It is recommended not to exceed a value of 22 kΩ in order not to alter the VLED sampled value.

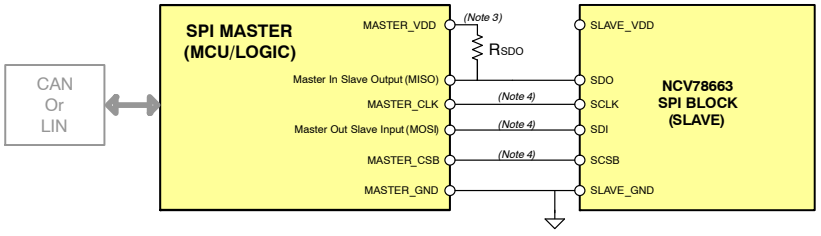


Figure 4. Details on NCV78663 Connection Diagram for SPI (Optional)

4. R_{SDO} external resistor typical value is 1 kΩ. An additional capacitor to ground (typically 47 pF) may be used in case of application noise observed.
5. External capacitors or RC may be added to these SPI lines for stable communication in case of application noise. The selection of these components must be done so that the resulting waveforms are respecting the limits reported in Table 23.

OPERATING CONDITIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage (Note 6)	VBB	−0.3	60	V
LED supply voltage (Note 7)	VBOOST	−0.3	68	V
Logic Supply voltage	VDD	−0.3	3.6	V
Low voltage I/O pins (Note 8)	IOLV	−0.3	VDD + 0.3	V
Gate driver supply voltage (Note 9)	VDRIVE	−0.3	12	V
GNDP voltage	GNDP_V	−0.3	0.3	V
Input current sense voltage	IBSTSENSE+, IBSTSENSE−	−1.0	3.6	V
Medium voltage IO pins (Note 10)	IOMV	−0.3	7.0	V
Buck switch low side	LBCKSW1, LBCKSW2	−2.0	VBOOST	V
Relative voltage IO pins (Note 11)	ΔV_IO	VBOOSTM3V	VBOOST	V
Storage Temperature	Tstrg	−50	135	°C
Buck switch output current (Note 12)	I_LBCKSW		1.4	A
Electrostatic discharge on component level (Note 13)	VESD	−2	+2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

6. Absolute maximum rating for pins: VBB, LEDCTRL1, LEDCTRL2.
7. Absolute maximum rating for pins: VBOOST, VBOOSTM3V, IBCK1SENSE+, IBCK1SENSE−, VINBCK1, VLED1, IBCK2SENSE+, IBCK2SENSE−, VINBCK2, VLED2.
8. Absolute maximum rating for pins: TEST1, TEST2, VTEMP1, VTEMP2, DIAG1, DIAG2.
9. Absolute maximum rating for pins: VDRIVE, VGATE.
10. Absolute maximum rating for pins: SCLK, SCS, SDI, SDO.
11. Relative maximum rating for pins: VINBCK1, VINBCK2, IBCK1SENSE+, IBCK2SENSE+, IBCK1SENSE−, IBCK2SENSE−
12. Peak value.
13. Human Body Model (100 pF via 1.5 kΩ, according to JEDEC EIA/JESD22−A114).

Table 3. RECOMMENDED OPERATING CONDITIONS

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the device outside the operating ranges described in this section is not warranted. Operating outside the recommended operating ranges for extended time may affect device reliability. A mission profile (Note 14) is a substantial part of the operation conditions, hence the Customer must contact ON Semiconductor in order to mutually agree in writing on the allowed missions profile(s) in the application.

Characteristic	Symbol	Min	Max	Unit
Battery Supply Voltage	VBB	5	40	V
Battery Supply Current (Note 15)	IBB		20	mA
Logic Supply Output Current	IDD		10	mA
5V Tolerant IO pins	DIG_IO_V	0	5.5	V
VTEMP/AGPx pins	VTEMPAGP_V	0.3	VDD	V
Gate Driver Supply Current (Note 16)	Idrive		10	mA
Ambient Temperature	T_A	−40	125	°C
Junction Temperature	T_J	−45	170	°C
VBB Voltage during OTP Zapping	V_{BB_ZAP}	13	40	V
OTP zap Ambient Temperature	T_A_zap	10	30	°C
Buck Switch Output Current (Note 17)	I_LBCKSW		1.2	A

14. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
15. VBB = 13 V; I_{drive} = 10 mA
16. VBB = 13 V; I_{drive} = Q_gate x f_boost
17. Average value

Table 4. THERMAL RESISTANCE

Characteristic	Package	Symbol	Max	Unit
Thermal resistance junction to exposed pad	SSOP36	θ_{JCbot}	3.49	KW^{-1}

ELECTRICAL CHARACTERISTICS

NOTE: Unless differently specified, all device Min & Max parameters boundaries are given for the full supply operating range and the junction temperature (T_J) range (-40;160) (°C).

Table 5. VBB: BATTERY SUPPLY INPUT

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Nominal Operating Supply Range	VBB		5		40	V
Device Current Consumption	IBB_0	buck regulators off, gate drive off, outputs unloaded		6	10	mA

Table 6. VDRIVE: 10 V SUPPLY FOR BOOST FET GATE DRIVE CIRCUIT

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VDRIVE regulator output voltage	VDRIVE	V_{BB} > 11 V: VDRIVE generated from VREG10V	9	10	11	V
		V_{BB} < 10 V: VDRIVE generated from VBOOST_AUXSUP*	MAX(5.5; V_{BB} – 1.65)	7.8		V
DC output current capability	Iout_VDRIVE				15	mA
Output current limitation	ILIM_VDRIVE	V_{BB} > 11 V: VDRIVE generated from VREG10V	36		185	mA
		V_{BB} < 10 V: VDRIVE generated from VBOOST_AUXSUP	15		190	mA
Typical VDRIVE external decoupling capacitor	C_VDRIVE			0.47		μF
	ESR				200	mΩ

*Boost regulator must be active.

Table 7. VDD: 3 V LOW VOLTAGE ANALOG DIGITAL SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VDD regulator output voltage	VDD	VDRIVE > 4.5 V	2.9	3	3.1	V
DC output current capability	Iout_VDD	VDRIVE > 4.5 V			10	mA
Output current limitation	Ilim_VDD	VDRIVE > 4.5 V	40		200	mA
Typical VDD external decoupling capacitor	C_VDD		0.22	0.47	10	μF
	ESR				200	mΩ
POR Toggle level on VDD rising	POR3V_H		1.43	2.3	2.54	V
POR Toggle level on VDD falling	POR3V_L		1.26	2.0	2.14	V
POR Hysteresis	POR3V_ Hyst			0.25		V

Table 8. VBOOSTM3V: HIGH SIDE AUXILIARY SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VBSTM3 regulator output voltage	VBSTM3	Referenced to VBOOST	−3.6	−3.3	−2.9	V
Output current limitation	Ilim_VBOOSTM3V				200	mA
Typical VBSTM3 decoupling capacitor	C_VBSTM3	Referenced to VBOOST		0.47	4.7	μF
	ESR	Referenced to VBOOST			200	mΩ

Table 9. OSC4M: SYSTEM OSCILLATOR CLOCK

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
System oscillator frequency	FOSC4M	After trimming	3.5	4.0	4.5	MHz

Table 10. ADC FOR MEASURING VBOOST, VBB, VLED1, VLED2, VTEMP/AGP1, VTEMP/AGP2

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
ADC Resolution	ADC_res			8		Bits
Integral Nonlinearity (INL)	ADC_INL		−1.5		+1.5	LSB
Differential Nonlinearity (DNL)	ADC_DNL		−2.0		+2.0	LSB
Full path gain error for measurements via VBB, VLEDx, VTEMP, VBOOST	ADC_GAINERROR		−3.25		3.25	%
Offset at output of ADC	ADC_OFFSET		−2		2	LSB
Time for 1 SAR conversion	ADCConv			8		μs
ADC full scale for VBB measurement	ADCFS_VBB			40		V
ADC full scale for VLED	ADCFS_VLED			80		V
ADC full scale for VTEMP	ADCFS_VTEMP			3		V
ADC full scale for Vboost	ADCFS_VBOOST			80		V
VLEDx input impedance	ADC_VLED_INZ		355	500	710	kΩ
VTEMP/AGPx input impedance	ADC_VTAGP_INZ		1.2	3	4.5	MΩ

Table 11. BOOSTER

Name	Symbol	Conditions	SPI/OTP SETTING	Normal Regulation Window (Note 18)			SHUTDOWN	Unit
				NREGL	TRGT	NREGH	MAX	
Booster output range	VBOOST	Range 0	[0000]	19.5	24.5	30	49	V
		Range 1	[0001]	22	27	32.5	49	
		Range 2	[0010]	24	29.5	35	49	
		Range 3	[0011]	27	32	38	49	
		Range 4	[0100]	29	35	40.5	49	
		Range 5	[0101]	31.5	37	43.0	49	
		Range 6	[0110]	34	40	45.5	59	
		Range 7	[0111]	36.5	42	48	59	
		Range 8	[1000]	39.0	45	51	59	
		Range 9	[1001]	41.5	47	53.5	59	
		Range 10	[1010]	44	50	56	59	
		Range 11	[1011]	46	52	57.5	59	
		Range 12	[1100]	48	54.5	60.5	62	
		Range 13	[1101]	49	57	65.0	67	
		Range 14	[1110]	52	59.5	65.5	67	
		Range 15	[1111]	57.5	62	66.5	67	

18. For further details about the booster table and definitions, please refer to the related section contained in this datasheet.

Table 11. BOOSTER (continued)

Name	Symbol	Booster Oscillator Frequency [2:0]					
		Conditions	SPI/OTP Setting	Min	Typ	Max	Unit
Booster oscillator frequency	OSC16M	FPWMBOOST = 180 kHz	[011]	−12%	11.5	+12%	MHz
		FPWMBOOST = 203 kHz	[010]		13		
		FPWMBOOST = 227 kHz	[001]		14.5		
		FPWMBOOST = 250 kHz	[000]		16		
		FPWMBOOST = 273 kHz	[111]		17.5		
		FPWMBOOST = 297 kHz	[110]		19		
		FPWMBOOST = 320 kHz	[101]		20.5		
		FPWMBOOST = 344 kHz	[100]		22		
Booster PWM frequency	FPWMBOOST	= f_OSC16M / 64		OSC16M is programmable in SPI/OTP			

Table 11. BOOSTER (continued)

Name	Symbol	Boost_ctrl_rate [2:0]				
		OTP Setting Only	Min	Typ	Max	Unit
Booster control rate	Boost_ctrl_rate	[011]	−12.5%	86	+12.5%	μs
		[010]		144		
		[001]		240		
		[000]		400		
		[111]		667		
		[110]		1111		
		[101]		31		
		[100]		52		

Table 12. BOOSTER PRE−DRIVER

Name	Symbol		Min	Typ	Max	Unit
High−side switch impedance	RONHI			2.5	4	Ω
Low−side switch impedance	RONLO			2.5	4	Ω

Table 13. BOOSTER − CURRENT LIMITATION

Name	Symbol		Min	Typ	Max	Unit
Current limitation threshold voltage	VLIMTH	Over full operating range	78	100	122	mV
	VLIMTH_hot	At T_J = 160 °C	85	100	115	mV
Threshold voltage hysteresis	VLIMHYS		5	10	20	mV
Sense voltage common mode range	CMVSENSE		−1		1	V

Table 14. ON−CHIP TEMPERATURE SENSOR

Name	Symbol		Min	Typ	Max	Unit
Thermal shut−down level (junction temperature)	TSD		163	169	175	°C
Thermal warning level (junction temperature)	TW			TSD − 5		°C

Table 15. BUCK REGULATOR − SWITCH

Name	Symbol		Min	Typ	Max	Unit
On resistance	$R_{DS(on)}$			0.82	1.0	Ω
Overcurrent detection	OCD		1.4		3	A
Switching slope	Trise			3		V/ns
	Tfall			3		V/ns

Table 16. BUCK REGULATOR − CURRENT REGULATION

Name	Symbol			Min	Typ	Max	Unit
Current sense comparator threshold voltage setpoint (= end of the BUCK ON−phase) MIN value	VThreshold_MIN	Programmable with 7−bit resolution internal DAC (bit code 0 = [0 0 0 0 0 0 0])		25	30	35	mV
Current sense comparator threshold voltage setpoint (= end of the BUCK ON−phase) MAX value	VThreshold_MAX	Programmable with 7−bit resolution internal DAC (bit code 127 = [1 1 1 1 1 1 1])		370	411	451	mV
Current comparator threshold voltage setpoint step (internal DAC resolution)	Delta VThreshold				3		mV
Name	**Symbol**	**SPI/OTP SETTING**		**Min**	**Typ**	**Max**	**Unit**
Smallest Toff x VLED constant	Toff_V_1	[0000]	Value on the right represents [VLED * Toff_i] VLED = 55 V and T_J = 155°C	9.9	12.4	14.9	µs x V
	Toff_V_2	[0001]		19.8	24.5	29.2	
	Toff_V_3	[0010]		39.6	45.9	52.2	
	Toff_V_4	[0011]		57	66.6	76.2	
	Toff_V_5	[0100]		76.4	88	99.6	
	Toff_V_6	[0101]		96.2	110	123.8	
	Toff_V_7	[0110]		116.8	132	147.2	
	Toff_V_8	[0111]		135.8	154	172.2	
Mid range off−time (trimmed @ VLED = 55 V)	Toff_V_9	[1000]		154.5	176	197.5	
	Toff_V_10	[1001]		173.2	198	222.8	
	Toff_V_11	[1010]		191.8	220	248.2	
	Toff_V_12	[1011]		210.6	242	273.4	
	Toff_V_13	[1100]		229.1	264	298.9	
	Toff_V_14	[1101]		248	286	324	
	Toff_V_15	[1110]		266.4	308	349.6	
Longest off−time	Toff_V_16	[1111]		283.3	330	376.2	
Off−time = f (VLED)	Toff_V_i	VLED > 5.4 V		Toff_i * VLED = CONST			µs x V
		6V < VLED < 55 V and Tj is fixed		CONST − 8.5%	Toff_i * VLED = CONST	CONST + 8.5%	µs x V
		10V < VLED < 55 V and Tj is fixed		CONST − 7%	Toff_i * VLED = CONST	CONST + 7%	µs x V
		−45°C<Tj<155°C and VLED is fixed		Toff_i * VLED = CONST ± 4%			µs x V
		1.9 V ≤ VLED < 2.6 V			9		µs
		VLED < 1.9 V			63		µs

Table 17. 5 V TOLERANT DIGITAL INPUTS (CSB, SDI, SCLK)

Name	Symbol		Min	Typ	Max	Unit
High−level input voltage	VINHI		2			V
Low−level input voltage	VINLO				0.8	V
Input leakage resistance	R_{pull} (Note 19)		5	10	20	kΩ

19. Pull down resistor (Rpulldown) for SDI and SCLK, pull up resistor (Rpullup) for CSB.

Table 18. 5 V TOLERANT OPEN−DRAIN DIGITAL OUTPUT (SDO)

Name	Symbol		Min	Typ	Max	Unit
Low−voltage output voltage	VOUTLO	I_{SDO_out} = −10 mA (current flows into the pin)			0.4	V
Equivalent output resistance	$R_{DS(on)}$_DIAG	Lowside switch		20	40	Ω

Table 19. 3 V TOLERANT DIGITAL INPUTS (TEST1, TEST2)

Name	Symbol		Min	Typ	Max	Unit
High−level input voltage	VINHI		2			V
Low−level input voltage	VINLO				0.8	V
Input leakage resistance	$R_{pulldown}$	Pulldown resistance		20	40	kΩ

Table 20. 3 V PUSH−PULL DIGITAL OUTPUTS (DIAG1, DIAG2)

Name	Symbol		Min	Typ	Max	Unit
High−level output voltage	VOUTHI	I_{DIAG_out} = 10 mA (current flows out of the pin)	2.4			V
Low−voltage output voltage	VOUTLO	I_{DIAG_out} = −10 mA (current flows into the pin)			0.4	V
Equivalent output resistance	$R_{DS(on)}$	Lowside switch		20	40	Ω

Table 21. 40 V TOLERANT DIGITAL INPUTS (LEDCTRL1, LEDCTRL2)

Name	Symbol		Min	Typ	Max	Unit
High−level input voltage	VINHI		0.7 x V_{BB}			V
Low−level input voltage	VINLO				0.3 x V_{BB}	V
Input leakage current	ILEAK		−1		1	μA

Table 22. DIMMING INTERFACE

Name	Symbol		Min	Typ	Max	Unit
Input dimming frequency	FDIMMING		50	1000	8000	Hz
Dimming signal input measurement and output reconstruction resolution	DIMres_IN_OUT			10		µs
Dimming Frequency Factor (= Output dimming frequency / input dimming frequency)	DFF[2:0]	SPI/OTP setting [100]		1		
		SPI/OTP setting [101]		2		
		SPI/OTP setting [110]		3		
		SPI/OTP setting [111]		4		
		SPI/OTP setting [000]		5		
		SPI/OTP setting [001]		6		
		SPI/OTP setting [010]		7		
		SPI/OTP setting [011]		8		

Table 23. SPI INTERFACE

Name	Symbol		Min	Typ	Max	Unit
SPI clock period	t_{CLK}		1			µs
SPI clock high time	t_{CLK_HI}		100			ns
SPI clock low time	t_{CLK_LO}		100			ns
SDI set up time, valid data before rising edge of CLK	t_{SET_DI}		50			ns
SDI hold time, hold data after rising edge of CLK	t_{HOLD_DI}		50			ns
CSB high time	t_{CS_HIGH}		2.5			µs
CSB set up time, CSB low before rising edge of CLK	t_{SET_CSB}		1			µs
CLK set up time, CLK low before rising edge of CSB	t_{SET_CLK}		100			ns
Delay time from falling edge of CSB to a valid DO signal	Td_{CSB_DO}		50			ns
Delay time from falling edge of CLK to a valid DO signal	Td_{CLK_DO}		50			ns

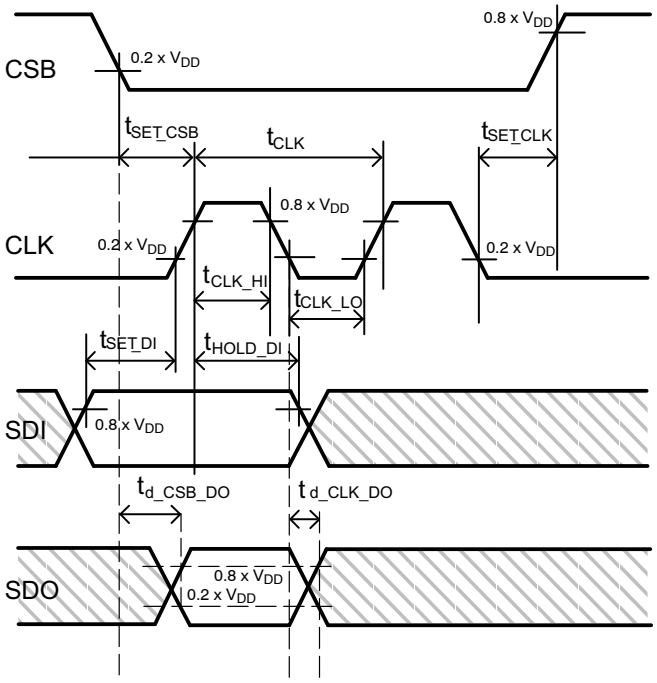


Figure 5. SPI Timing

DETAILED OPERATING AND PIN DESCRIPTION

SUPPLY CONCEPT IN GENERAL

Low operating voltages become more and more required due to the growing use of start stop systems. In order to respond to this necessity, the NCV78663 is designed to support power−up with a minimum guaranteed V_{BB} = 5 V.

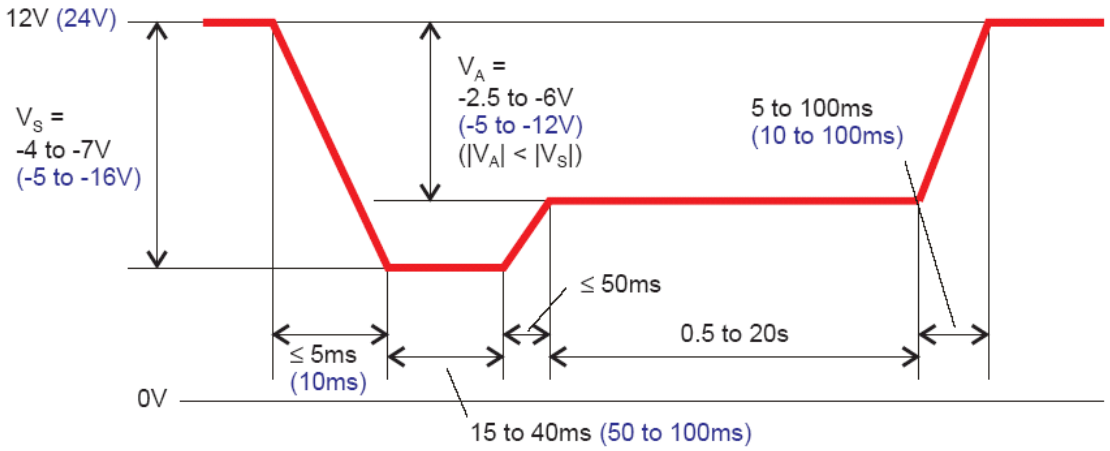


Figure 6. Cranking Pulse (ISO7637−1): System has to be Fully Functional (Grade A) from V_S = 5 V to 28 V

VDRIVE Supply

The VDRIVE supply voltage is the primary supply for the complete chip and sustains the VREG3V (which provides the VDD voltage, used by the internal circuitry) and the BOOST PREDRV, which generates the VGATE, used to switch the booster MOSFET.

In order to support low VBB battery voltages and long crank pulse drops, the VDRIVE supply takes its energy from the source with the highest output voltage, either from:

- the VREG10V supply, which derives its energy from the VBB input.
- the VBOOST_AUXSUP, which gets its energy from the VBOOST path.

Under normal operating conditions, VREG10V is the highest and all the internal device plus gate driver energies are supplied via VBB.

At power−up, the VREG3V (for VDD) is supplied through the VREG10V from the VBB input pin. Due to the low drop−out, the chip starts up from VBB ≥ 5 V and, the boost voltage starts to build−up.

In case VBB drops below the regulator margin of VREG10V, the VDRIVE supply is then sustained by the VBOOST_AUXSUP regulator: after this occurs, VBB can drop below 5 V and lower, as long as the booster is capable to generate sufficient voltage.

Note: Powering the device via the VBOOST_AUXSUP will produce an extra power dissipation linked to the related linear drop (VBOOST−VBOOST_AUXSUP), which must be taken into account during the thermal design.

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip and takes energy from VDRIVE. Due to the low drop−out regulator design, VDD is guaranteed already from low VDRIVE voltages (see Table 7). The Power On Reset circuit (POR) monitor is based on the VDD voltage.

VBOOSTM3V Supply

The VBOOSTM3V is the high side auxiliary supply for the gate drive of the buck regulators' integrated high−side P−MOSFET switches. This supply receives energy directly from the VBOOST pin.

INTERNAL CLOCK GENERATION

Two internal clocks are fully internally generated without the need for any further trimming by the user. Their accuracy is guaranteed under full operating conditions and independent from external component selection.

OSC4M Clock

The OSC4M clock is the system clock and factory trimmed to 4 MHz. It provides a time base for the entire digital part, except the boost converter PWM and the SPI clock. For details about the accuracy see Table 9.

OSC16M Clock

The OSC16M clock is the booster reference clock. It is factory trimmed and user selectable between typical 11.5 MHz and 22 MHz. The booster PWM frequency is 1/64 of the OSC16M frequency, thus between 179.7 kHz and 343.8 kHz. Refer to Table 11 for accuracy details.

ADC

General

The built−in analog to digital converter (ADC) is an 8−bit capacitor based successive approximation register (SAR).

This embedded peripheral can be used to provide the following measurements to an external Micro Controller Unit (MCU):

- VBOOST voltage
- VBB voltage
- VLED1, VLED2 voltages
- VTEMP_AGP1, VTEMP_AGP2 voltages

The internal NCV78663 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The device LED diagnostics and the digital boost controller make use of the values as inputs.

To remark that the VLEDx (1, 2) lines are sampled only when the respective LED output is activated and the last sampled value is kept, until it is overwritten (refreshed) by a new one.

An external MCU can read−out all measured values via the SPI interface in order to take application specific decisions. Please note that the MCU SPI commands do not interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

Each new boost voltage sample occurs at 17 μs worst case rate. VLED1 and VLED2 voltages are typically sampled at a rate of about 52 μs (when the buck switches are on), while VTEMP_AGP1 and VTEMP_AGP2 are continuously sampled at a rate of 4 ms. The battery voltage is sampled typically each 108 μs.

ADC Channel Selection

The ADC channel selection readout is done via the SPI-CR11 register (the part “ADC_Sel” behaves as a pointer to the requested data), while the SPI−SR3 registers will hold the data (see section SPI Address Map). When polling the same channel over time, there is no need to refresh the address field, as the SPI−SR3 register will be automatically refreshed with the latest available data.

ADC_SEL[2:0]	VBOOST	VBB	VLED1	VLED2	VTEMP_AGP1	VTEMP_AGP2
000	1	0	0	0	0	0
001	0	1	0	0	0	0
010	0	0	1	0	0	0
011	0	0	0	1	0	0
100	0	0	0	0	1	0
101	0	0	0	0	0	1
110	Do not select					
111	Do not select					

Battery Voltage ADC Measurement

The battery voltage is sampled making use of the device supply VBB−pin. This measurement is also used by the boost controller for the closed loop voltage regulation to set the maximum duty cycle depending on the battery level: the lower the level, the higher the maximum duty cycle allowed.

The (8 bit) conversion ratio is 40/255 (V/dec) = 0.157 (V/dec) typical. The external MCU can make use of the measured VBB value to monitor the status of the module supply and also for a different or more complex power de−rating algorithm than the one embedded in the NCV78663 (see Section Automatic Power De−rating).

LED String Voltage ADC Measurement

The voltage at the pins VLEDx (1, 2) is measured. Their 8 bit conversion ratio is 80/255 (V/dec) = 0.318 (V/dec) typical.

This is also used by the diagnostics controller to detect OpenLEDx, ShortLEDx and IndShortLEDx.

The external MCU can use the measured VLED value for a dedicated individual short LED algorithm, more complex than the threshold decision based embedded in the LED DRIVER.

LED Temperature Feedback / ADC General Purpose Inputs Measurement

Measures the voltage at the pins VTEMP/AGPx (1,2). The typical application would be sensing the transducer voltage related to LED modules’ temperature, so that the external MCU can use the information for protecting the LED strings from overheating, or to adapt the luminous flux to the temperature. A common technique is to use an NTC pulled up to the chip VDD.

The VTEMP/AGPx typical sample rate is 4 ms. Please note that these pins are ADC *general purpose* and can be also used to sample references, or other application−related relatively slowly varying voltages.

The VTEMP/AGPx input dynamic range is given by the VDD voltage and no higher value can be forced to these pins.

Their (8 bit) conversion ratio is 3/255 (V/dec) = 11.76 (mV/dec) typical.

Boost Voltage ADC Measurement

This measure refers to the boost voltage at the VBOOST−pin, with an 8bit conversion ratio of 80/255 (V/dec) = 0.318 (V/dec) typical. This measurement is also used by the boost controller and by the diagnostics controller to detect Boost under−voltage (BoostUV).

BOOST CONTROLLER

The NCV78663 features one common booster stage for the two integrated buck current regulators. In addition, optional external buck regulators belonging to other devices can be cascaded to the same boost voltage source as well as exemplified in the picture below.

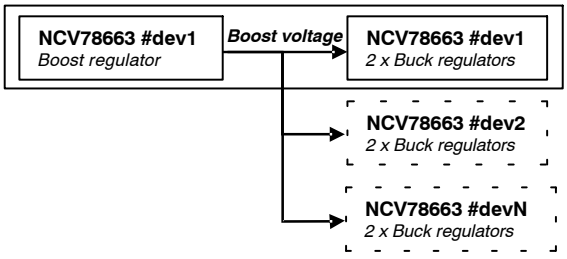


Figure 7. Cascade of Multiple NCV78663 Buck Channels on a Common Boost Voltage Source

The booster stage provides the required voltage source for the LED string voltages out of the available battery voltage. Moreover, it filters out the variations in the battery input current in case of LED strings PWM dimming.

For nominal loads, the boost controller will regulate in *continuous mode* of operation, in order to maximize system power efficiency and to have the lowest possible input ripple current (with “continuous mode” it is meant that the supply current does not go to zero while the load is activated).

In case of low loads or low dimming duty cycle values, *discontinuous mode* can occur: this means the supply current can swing from zero when the load is off to the required peak value when the load is on, while keeping the required input average current through the cycle. In such situations, the total efficiency ratio may be lower than the theoretical optimal. However, as also the total losses will at the same time be lower, there will be no impact on the thermal design.

Booster Voltage Range Selection

The boost voltage can be programmed in one of the sixteen (16) available ranges by means of the SPI register booster output range [3:0] (or OTP in NCV78663 stand alone mode). Each of the ranges has its typical regulation level, called target (V_{BOOST_TRGT}) and a so defined normal regulation region, or “window 1”, whose limits are NREGL and NREGH.

In normal regulation mode, the boost voltage V_{BOOST} time average will always match the target, while its instantaneous value is free to swing between NREGL and NREGH.

The absolute maximum voltage for each range is defined as shutdown level ($V_{SHUTDOWN}$). For $V_{BOOST} \geq V_{SHUTDOWN}$, the MOSFET PWM (VGATE) will be switched off. The shutdown level can be chosen to minimize the needed voltage rating (size/cost) of the externals.

The range should be selected with the appropriate NREG levels for the application. In particular, for proper operation of the LED strings, the selected boost voltage range “xx” must be such that NREGL_xx is higher than the maximum LED string voltage used.

More information about the boost control loop is given in the following section.

Booster Regulation Closed Loop Details

The NCV78663 features a digital voltage mode controller designed to regulate the boost voltage around the target defined by the selected range. This closed loop system samples feedback signals and drives the boost MOSFET gate by PWM as shown in the next figure.

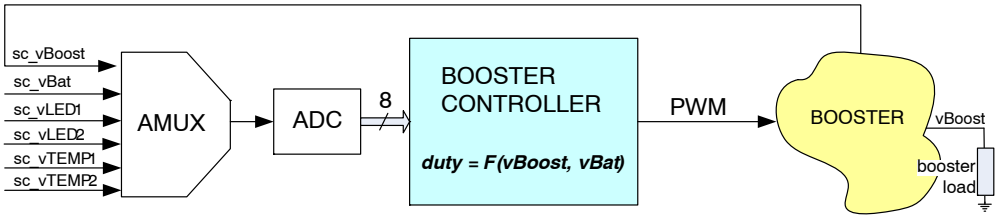


Figure 8. NCV78663: Boost Voltage Regulation Closed Loop

The regulation feedback is mainly based on the V_{BOOST} sampled value itself and only partially on the battery value seen at the device pin (VBB). Both signals are sampled by the NCV78663 internal ADC in the way described in the relative section. The boost voltage is regulated with a fixed frequency / variable duty cycle scheme.

The duty cycle (DC) is obtained internally out of a 6−bit counter (DC = 0 ÷ 63). DC = 63 corresponds to duty cycle 100% and DC = 0 corresponds to duty cycle 0%. However, 100% is never allowed and the maximum duty cycle corresponds to a parameter defined as DC_{max}. In addition, except in case of shutdown, the duty cycle is low−bounded to a value called DC_{min}, which is hard coded to value of “4” (4/63 = 6.3%) and is the same for all selectable booster ranges.

DC_{max} is fetched from an internal ROM table and depends on the sampled battery voltage, this last divided in ranges. The general rule is the higher the battery voltage, the lower the DC_{max} allowed. This is intended to reduce boost voltage and input current overshoots when the battery voltage goes too high. For low battery voltages, the DC_{max} is increased to permit more current inflow to allow achieving the required output power. The DC_{max} value 61 (96.8%) is never exceeded even in case of ultra−low battery.

Eight battery ranges are available as shown below:

Table 24. NCV78663 BATTERY RANGES FOR BOOST CONTROLLER

VBB_RNG0	VBB_RNG1	VBB_RNG2	VBB_RNG3	VBB_RNG4	VBB_RNG5	VBB_RNG6	VBB_RNG7
0 ÷ 5 V	5 ÷ 10 V	10 ÷ 16 V	16 ÷ 20 V	20 ÷ 24 V	24 ÷ 30 V	30 ÷ 35 V	35 ÷ 40 V

Each Vboost ADC sample is compared within voltage sections called “windows”. For each selected range, four different windows, plus a shutdown safety level, are present:

A. **Window 0**. This is one of the “normal modes” of the control law. When the sampled Vboost falls in this region, there is no change in the PWM duty cycle. For all boost ranges, the width of this window is 2 V. The central value of this window is corresponding to V_{BOOST_TRGT}, reported in the middle column of Table 11.

B. **Window 1**. This is the most frequent status of the control law and this is what we refer to simply as general “normal mode”. When in this region, the PWM is corrected by “±1dec” (= ±1.58%) with a cadency corresponding to the *boost control rate*. The sign of the correction will be “plus” if the voltage is below window 0; “minus” otherwise. Each correction is intended to bring Vboost towards the V_{BOOST_TRGT}. The size of any window 1, ranging in Table 11 from NREGL to NREGH, is typically about 10 V.

C. **Window 2**. When in this region, the PWM duty is adapted by “±2” (= ±3.17%) with a cadency corresponding to the *boost control rate*, with the intention to bring Vboost towards the target. As the distance from the target is higher than in point B., the correction is stronger.

D. **Window 3**. When in this range the controller works in limitation mode. The PWM duty cycle is rapidly modified every two PWM periods: in the upper threshold, the duty cycle is decreased towards the DC_{max} trying to avoid reaching the shutdown level, whereas in the lower threshold side the duty cycle is ramped up towards the DC_{min} “pumping in” energy from the supply to avoid LED blank out because of lack of voltage headroom.

E. **Shutdown**. This is a safety level to avoid overvoltage at which the MOSFET gate is shut off (duty cycle = 0%, or DC = 0). This is corresponding to column “MAX” rating in Table 11. Note: this “MAX rating” corresponds also to the maximum booster output voltage in case of unloaded stage (buck regulators off).

A graphical explanation is given in the figure below by referring to boost range 06 as an example.

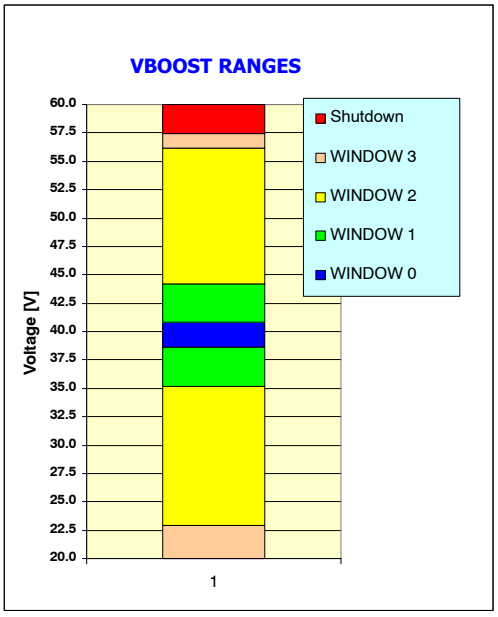


Figure 9. NCV78663: Boost Controller Voltage Segments When Boost_RNG = 6 is Selected

REMARKS and PRACTICAL CONSIDERATIONS

For a well sized booster system with the NCV78663, the controller will operate inside window 1 (or window 0), thus:

$$V_{BOOST_TRGT} - 5\ V < V_{BOOST} < V_{BOOST_TRGT} + 5\ V$$

An exception might be at booster load start−up, when its output power passes for the first time from zero (unloaded) to maximum (application target). In this case, the voltage is allowed to drop in the low threshold of window 3 and after a first settling transient, the regulation will enter normal mode (window 1).

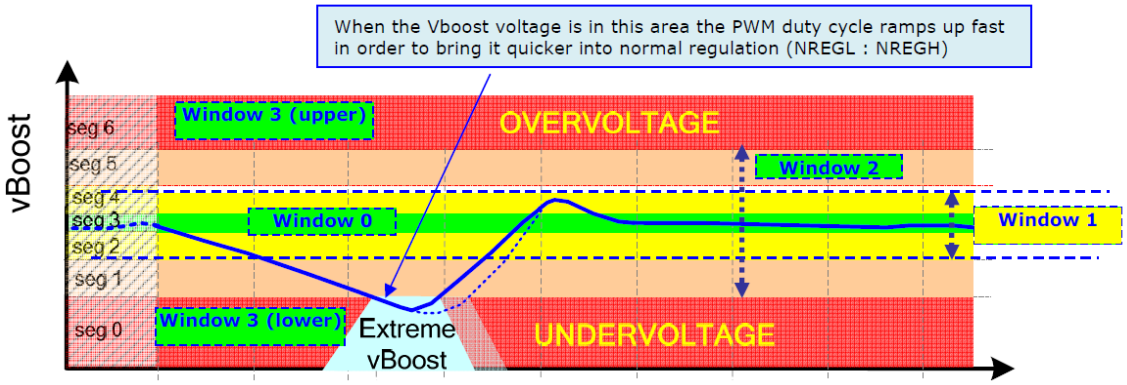


Figure 10. NCV78663: Boost Voltage Possible Behavior at First Full Power Load Activation

In order to guarantee the regulation in WINDOW 1 throughout operating conditions and dimming, a total boost capacitance Cboost ≥ 50 μF is recommended for medium to high application power. For further details about capacitance sizing, please refer to application notes.

Please note that the boost voltage regulation loop is not affected whether a continuous or discontinuous mode of operation (E.G. low dimming duty cycle) is taking place.

Booster PWM Frequency

The booster controller is working with a constant frequency and variable duty cycle to control the booster voltage.

The operating frequency is user selectable with three SPI/OTP setting bits (Section OSC16M Clock), in order to optimize the booster inductor's size and EMC aspects.

Booster Disable Function

In some cases, it is useful to disable the booster by means of the BOOSTER_DIS bit. For instance if:

- the NCV78663 uses a shared booster from another device,
- it is desired to start the hardware module from a complete off state, or to minimize energy consumption in some particular operating modes.

External Boost FET Pre−driver

The external boost MOSFET is directly controlled by the integrated pre−driver with slope−control to attenuator EMC emissions. Due to the cycle by cycle current limitation, the peak−currents in the MOSFET are reduced, resulting in optimized system efficiency. Also for efficiency reasons, it is important to select a MOSFET with low gate−charge.

The pre−driver is supplied by the VDRIVE supply (typical 10 V) supporting standard FETs.

Buck Regulator

The buck regulator is the current source to the LED string. This block controls the peak current and also incorporates a constant ripple control circuit to ensure also stable average current through the LED string.

The formula that defines the total ripple current over the buck inductor is hereby reported:

$$\Delta I_{BUCK_pkpk} = \frac{T_{OFF} \times (V_{LED} + V_{DIODE})}{L_{BUCK}}$$

$$\cong \frac{T_{OFF} \times V_{LED}}{L_{BUCK}} = \frac{T_{OFF_V_BUCK}}{L_{BUCK}}$$

In the formulas above T_{OFF} represents the buck switch off time, V_{LED} is the LED voltage feedback sensed at the NCV78663 pin and L_{BUCK} is the buck inductor value.

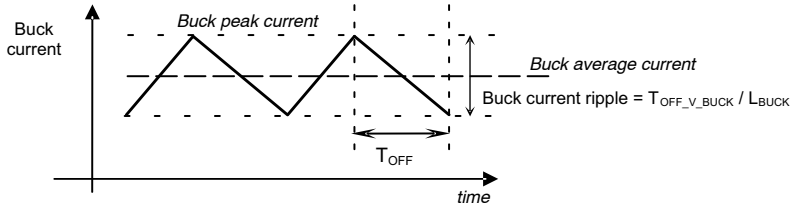


Figure 11. Buck Regulator Controlled Average Current

In order to achieve a constant ripple current value, the NCV78663 varies the T_{OFF} time inversely proportional to the V_{LED} sensed at the device pin, according to the factor $T_{OFF_V_BUCK}$ programmable by SPI/OTP (see Table 16).

As a consequence to the constant ripple control and variable off time, the buck switching frequency is dependent on the boost voltage and LED voltage in the following way:

$$f_{BUCK} = \frac{V_{BOOST} - V_{LED}}{V_{BOOST}} \cdot \frac{1}{T_{OFF}} =$$

$$= \frac{V_{BOOST} - V_{LED}}{V_{BOOST}} \times \frac{V_{LED}}{T_{OFF_V_BUCK}}.$$

The buck average current is described by the formula:

$$I_{BUCK_AVG} = I_{BUCK_peak} - \frac{\Delta I_{BUCK_pkpk}}{2}.$$

The parameter I_{BUCK_peak} is programmable through the device by means of the internal comparator threshold (Table 16) over the external sense resistor RSENSE:

$$I_{BUCK_peak} = \frac{V_{Threshold}}{R_{SENSE}},$$

where $V_{threshold}$ is the current comparator internal set−point reference (Table 16).

$$V_{Threshold} = V_{Threshold_MIN} + Delta_V_{Threshold} \times$$

$$\times \text{ Current_Setting_SPI(dec)}.$$

The item “Current_setting_SPI (dec)” corresponds to the value written in the related for the “x” string, programmable from 0 to 127 (7bits). Please refer to Tables 26 and 27 for more information.

The full buck circuit diagram follows:

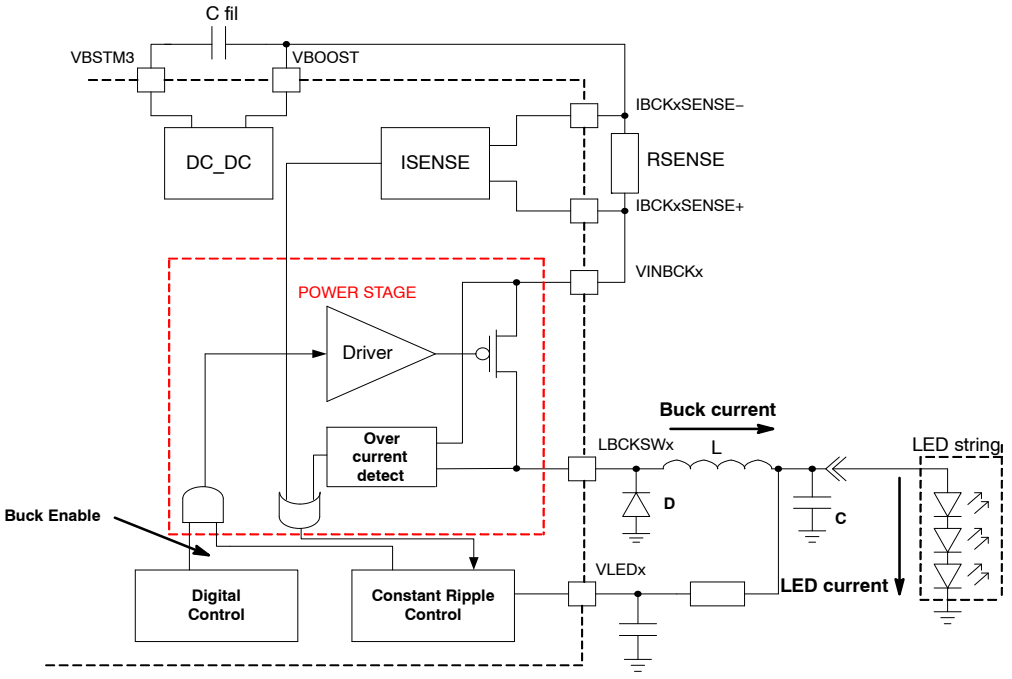


Figure 12. Buck Regulator Complete Schematics

Independently from the peak current setting, there is also an overcurrent detection (fixed threshold) which is measured over the internal buck MOSFET. See Table 15.

The LED average current in time is equal to the buck time average current. Therefore, to achieve a given LED current target, it is sufficient to know the buck peak current and the buck current ripple.

For what concerns the LED ripple current, this is defined by the Buck inductor ripple current, the buck capacitor and the total LED string equivalent impedance. A rule of thumb is to count a minimum of 50% ripple reduction by means of the capacitor C_{BUCK} and this is normally obtained with a ceramic component ranging from 100 nF to 470 nF. The following figure reports a typical example. The use of C_{BUCK} is a cost effective way to improve EMC performances without the need to increase the value of L_{BUCK}, which would be certainly a more expensive action.

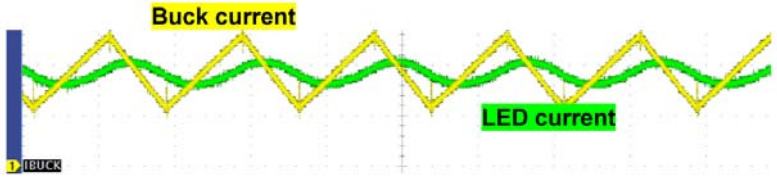


Figure 13. LED Current AC Components Filtered Out By the Output Impedance (scope snapshot)

DIMMING

The chip supports both analog and digital or PWM dimming. Analog dimming is done by controlling the LED current during operation. This can be done by means of changing the peak current level and/or the Toff_V constants (see Buck Regulator − Current regulation) by SPI commands.

In this section, we only describe the PWM dimming as this is the preferred method to maintain the desired LED color temperature for a given current rating.

In digital dimming, the LED current waveform frequency is constant and the duty cycle is set according to the required light intensity. The two independent control inputs LEDCTRLx handle the dimming signals for the related channel. More details in the following section.

Dimming Control Scheme

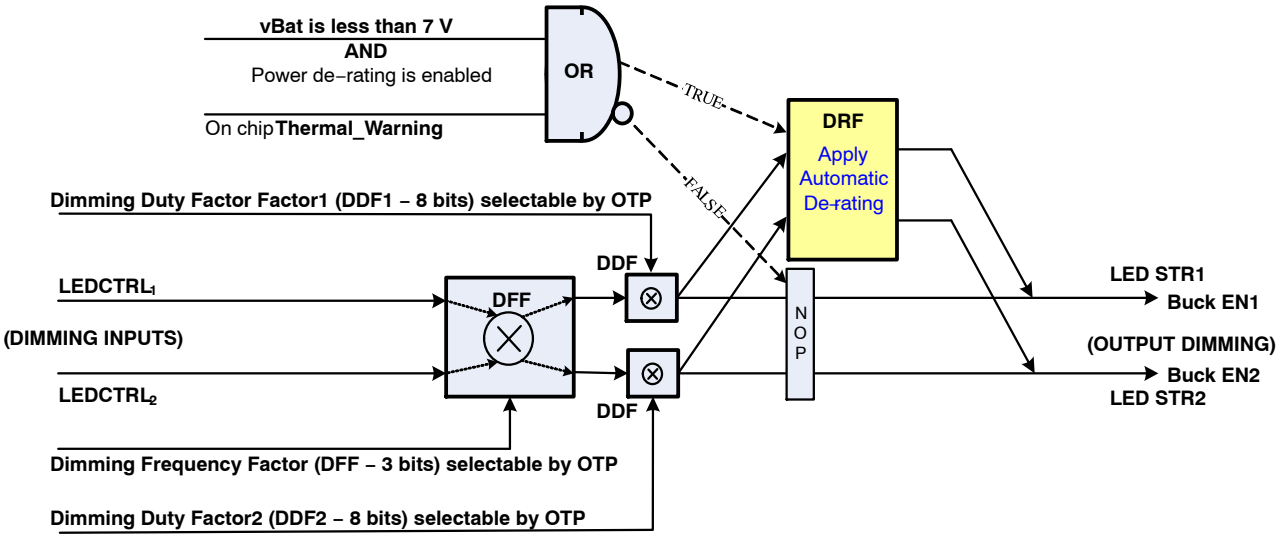


Figure 14. NCV78663 Internal Digital (PWM) Dimming Structure

The dimming signal of each LED string is controlled via the respective LEDCTRLx input; the PWM there applied is sampled and converted into an output PWM signal used for enabling the buck channel driving the LEDx string (the internal buck MOSFET enabled signal is called BUCK_ENx).

The BUCK_ENx signal frequency is obtained multiplying the input frequency by the Dimming Frequency Factor (DFF). Increasing the dimming frequency is very useful to avoid the *beats effect*. In addition, higher dimming frequency reduce the dimming boost voltage swings for a given output booster capacitor.

The BUCK_ENx duty cycle is equal to the input duty cycle times the internal scaling factors: the Dimming Duty Factor (DDF) and the Dimming Derating Factor (DRF). This last is automatically set by the device in case a power de−rating condition is occurring (see section Automotive Power De−rating). The DRF is applied to both channels simultaneously.

The DDFx is instead individually programmable for each buck channel and can range from 0% to 100%. The default DDFx value is written in OTP, while a microcontroller can vary the present value via SPI when the application is running. The formula which links the output dimming duty factor for the channel "x" to the internal SPI register is:

$$\text{DutyFactor}_x = 100 \times \frac{255 - \text{DDF}_{\text{SPI_REGx}}}{255}$$

or equivalently:

$$\text{DDF}_{\text{SPI_REGx}} = 255 \times \frac{100 - \text{DutyFactor}_x}{100}$$

The following formula summarizes the effects on the dimming duty cycle for the LED STRING "x":

$$\text{BuckENx}_{\text{DUTY}} = \text{DutyIN}_{\text{LEDCTRLx}} \times \text{DutyFactor}_x \times \text{DRF}$$

Where $\text{DutyIN}_{\text{LEDCTRLx}}$ represents the input duty cycle provided by the external logic (or MCU) at the LEDCTRLx input.

As the input signal at the LEDCTRLx is sampled by the NCV78663 digital, a delay must elapse for each change in frequency and/or duty cycle before the device can reconstruct a new valid BUCK_ENx. The maximum delay for a frequency change is four periods of the input signal, whereas for a duty cycle change only, with any given frequency, up to two periods of the input signal can be needed.

To detect an input duty cycle of 100% ("long one" = LEDx continuously ON), an input period higher than 40 ms is

required. Vice versa, starting from a 100% duty cycle condition, in order to detect a 0% input signal (LEDx continuously OFF), up to 2 ms may be required.

Using a 100% input duty cycle will by nature remove the external dimming frequency reference to the device. In such a case, if a duty cycle scaling (DDFx or DRF) is active, the internal frequency dimmer timer is used. Its base frequency is 500 Hz x DFF. This feature can be exploited as a method to avoid the use of an external frequency generator even when dimming is really intended: an hint for the application is then to tie (or pull up) the LEDCTRLx pins to the VBB pin and to set the wanted dimming parameters just by means of SPI. A DDFx = 0% (255dec) will always secure to turn off the LEDx strings across operating conditions.

To note how the time resolution of both the input LEDCTRLx sampler and the BUCK_ENx output reconstructed signals is 10 μs nominal (see Table 22): this value corresponds to the smallest resolution obtainable for digital dimming.

Automatic Power De−rating

The LED output power can be automatically de−rated by decreasing the calculated output duty cycle in case of detected extreme conditions: either low battery voltage or active on−chip Thermal Warning.

The NCV78663 features an embedded automatic power derating function based on the battery voltage which can be enabled or disabled by OTP/SPI (PWRDERATE_DIS bit, see SPI map). The battery voltage measurement is automatically performed by the device sampling of the VBB pin. In case a protection diode in front of the VBB is used, its voltage drop and the discharge delay of the external capacitor in parallel to the pin have to be taken into account. The V_BAT power derating is implemented according to the graph below:

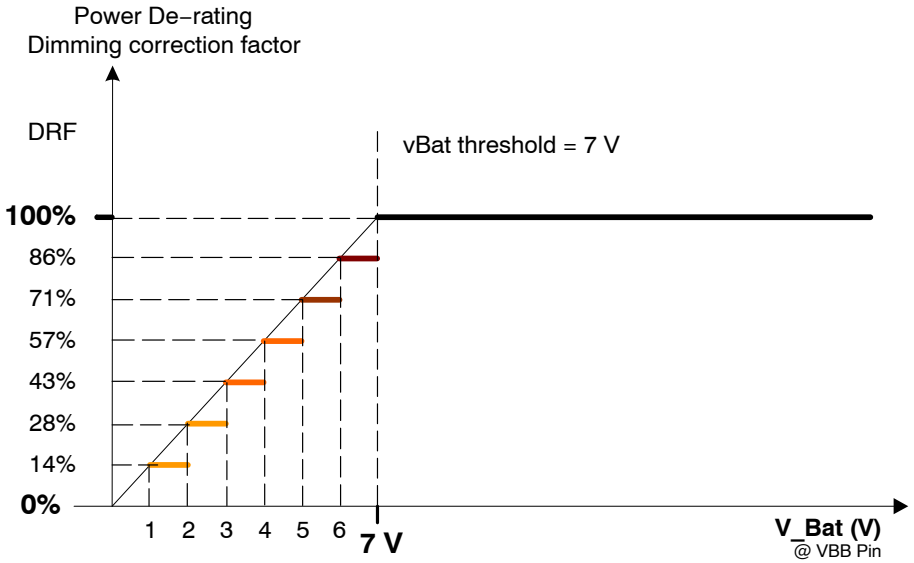


Figure 15. NCV78663 Internal V_Bat Power Derating Profile

When the de−rating condition disappears the output duty will go back to 100% of the calculated output duty. The de−rating process is applied on both led channels simultaneously.

In case of on−chip Thermal Warning, the calculated output duty cycle is further scaled to 75% of its previous calculated value (*thermal derating*). Then when the junction temperature falls below the Thermal Warning level, the thermal de−rating condition is automatically exited. The warning bit in SPI status register remains activated until reset via an SPI read−command.

Example: V_Bat de−rating and thermal derating occurring at the same time. For instance, 6 V < VBB < 7 V and thermal warning: the total de−rating factor would be 86% x 75% = 64.5%.

SPI INTERFACE

Description

The serial peripheral interface (SPI) is used to program the default start−up operating parameters in OTP via the ZAP! operation. Optionally, it allows an external microcontroller (MCU) to communicate with the device to read−out status information and to change operating parameters after power−up.

The NCV78663 SPI transfer packet size is 16 bits. During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines: SDO and SDI.

The DO signal is the output from the Slave, and the SDI signal is the output from the Master. A slave select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple−slave system. The CSB line is active low. If an NCV78663 is not selected, SDO is in high impedance state and it does not interfere with SPI bus activities. Since NCV78663 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation. The SPI CLK idles low between transferred frames. The diagram below is both a master and a slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

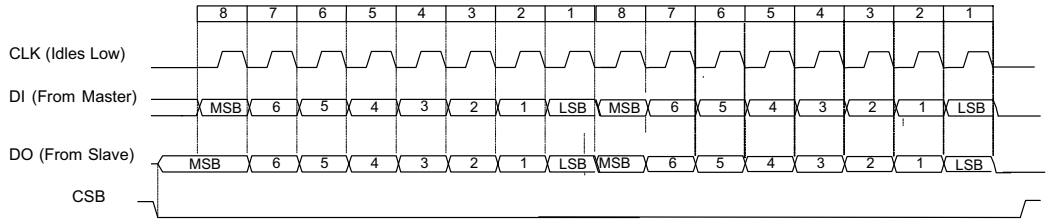


Figure 16. NCV78663 SPI Transfer Format

Note: The data transfer from the shift register into the locally used registers, interpretation of the data is only done at the rising edge of CSB.

The Data that is send over to the shift register to be transmitted to the external MCU is sampled at the falling edge of CSB, just at the moment the transmission starts.

The implemented SPI block allows interfacing with standard MCUs from several manufacturers. When interfaced, the NCV78663 acts always as a Slave and it cannot initiate any transmission. The MCU is instead the master, able to send read or write commands. The NCV78663 SPI allows connection to multiple slaves by means of both star connection (one individual CSB per Slave, while SDI, SDO, CLK are common) or by means of daisy chain (common CSB signal and clock, while the data lines are cascaded as in the figure). An SPI *star connection* requires a bus = (3 + N) total lines, where N is the number of Slaves used, the SPI frame length is 16 bits per communication. Regarding the SPI *daisy chain connection*, the bus width is always four lines independently on the number of slaves. However, the SPI transfer frame length will be a multiple of the base frame length so N x 16 bits per communication: the data will be interpreted and read in by the devices at the moment the CSB rises.

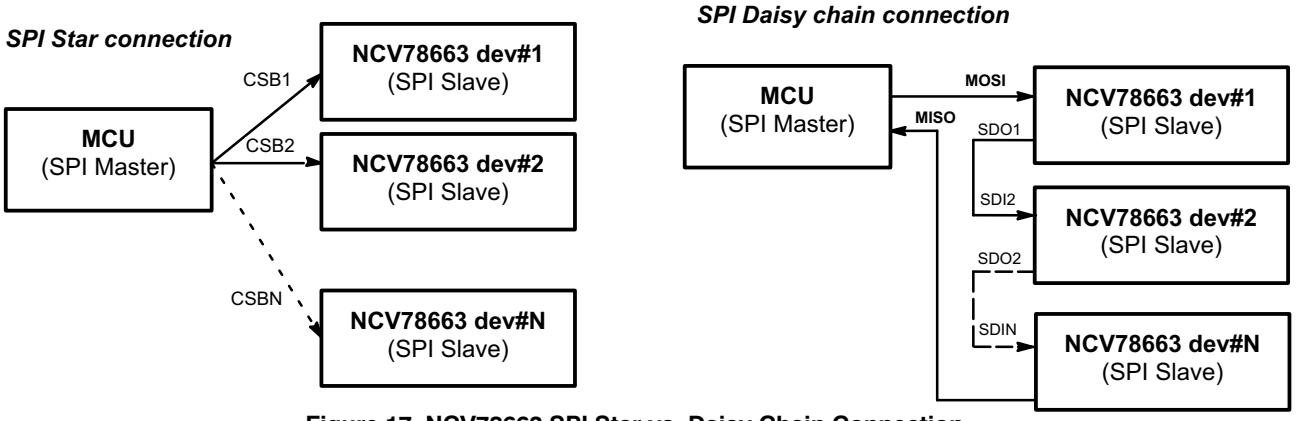


Figure 17. NCV78663 SPI Star vs. Daisy Chain Connection

Transfer Format

All SPI commands (to SDI pin of NCV78663) from the Master consist of one “address/command byte” (MSByte or MSB) and one “data byte” (LSByte or LSB).

The address/command byte is the MSB and is divided into two nibbles (2 x 4 bits). Each nibble is an address pointing to the 16 bytes address space of the NCV78663 SPI register map (see related section) and in the same time it is interpreted also as a command (explanation given below). Two types of registers exist in the SPI address space: Control and Status registers. Control registers are read/write accessible whereas Status registers are only read accessible. The type of the register is determined by the address decoder of the SPI and depends on its position in the address space.

Three command−types can be distinguished: “Write to a control register”, “Read from a control register” and “Read from a status register”.

- Writing to a control register is accomplished only if the address of the target register appears in the upper address/command nibble. The contents of the data−byte will be copied in the control register.

- Reading from a control register is accomplished by putting its address in the lower address/command nibble. The data byte has no function for this command.
- Reading from a status register is accomplished by putting its address either in the upper or in the lower address/command nibble. The data byte has no function for this command.

The response (SDO) on the commands from the first frame is always two bytes long and is located in the subsequent SPI frame. The possible combinations of SDI/SDO and their use are summarized in the following table:

Table 25. SPI FRAME FORMAT TRANSFER

	NCV78663 received input: SDI			NCV78663 response: SDO		
	SPI 16bit Frame 01 MSB *high−nibble*	SPI 16bit Frame 01 MSB *low−nibble*	SPI 16bit Frame 01 LSB	SPI 16bit Frame 02 MSB	SPI 16bit Frame 02 LSB	
ID	ADDR_CMD [7:4]	ADDR_CMD [3:0]	DATA[7:0]	ADDR_CMD[7:0]	DATA[7:0]	Comments
1	ACR1	ACR2	DICR1	DOCR1	DOCR2	Write to CR1 content of data field (DICR1) and read CR2
2	ACR1	ASR1	DICR1	DOCR1	DOSR1	Write to CR1 content of data field (DICR1) and read ASR1
3	ASR1	ACR1	XXh	DOSR1	DOCR1	Read both ASR1 and ACR1
4	ASR1	ASR2	XXh	DOSR1	DOSR2	Read both ASR1 and ASR2

LEGENDA:

- ACRx = Address of Control Register x
- ASRx = Address of Status Register x
- DICRx = Data Input of Control Register x
- DOCRx/DOSRx = Data Output of corresponding Register.
- XXh = any byte

SPI Command Example: Write “data value 255” (= 0xFF hex) to control register at “address 1” (= 0x01 hex) and read control register at “address 4” (= 0x04 hex)

SDI Line (binary representation)

Frame 01 (16bit)																Frame 02 (16bit)															
MSB: High Nibble				MSB: Low Nibble				LSB								MSB (dummy/NOP)								LSB (dummy/NOP)							
0	0	0	1	0	1	0	0	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDO Line

Frame 01 (16bit)		Frame 02 (16bit)								
MSB	LSB	MSB								LSB (dummy/NOP)
Response from past command or not valid data out−of−reset	Response from past command or not valid data out of reset	1	0	1	0	1	0	1	1	Content of register 0x04

NOTE: In any SPI communication transfer a frame which is not multiple of 16 bits is considered as an error and is discarded by the device. In case of SPI error, the specific error flag in STATUS REGISTER 2 is raised (see SPI address map).

SPI ADDRESS MAP

Table 26. SPI BANK REGISTER SUMMARY

SPI Address	POR Value	Access	7	6	5	4	3	2	1	0
0x00	0x00	–	NOP							
0x01	0x00	R/W	**Control Register 1**							
			Dimming Duty Factor LED string 1 [7:0]							
0x02	0x00	R/W	**Control Register 2**							
			Dimming Duty Factor LED string 2 [7:0]							
0x03	0x00	R/W**	**Control Register 3**							
			OTPLockInt**	Current setting LED string 1 [6:0]						
0x04	0x00	R/W**	**Control Register 4**							
			OTPLockExt**	Current setting LED string 2 [6:0]						
0x05	0x00	R/W	**Control Register 5**							
			LED string 1 diagnostics individual short threshold [7:0]							
0x06	0x00	R/W	**Control Register 6**							
			LED string 2 diagnostics individual short threshold [7:0]							
0x07	0x00	R/W	**Control Register 7**							
			BOOSTER_DIS	Booster oscillator frequency [2:0]			Booster output range [3:0]			
0x08	0x00	R/W	**Control Register 8**							
			Toff 1 range selection [3:0]				PWRDERATE_DIS	Dimming frequency factor [2:0]		
0x09	0x00	R/W (*TEST)	**Control Register 9 / OTP_Ctrl [7:0]**							
			OTP_Start*	OTP_Cmd [1:0]*		Reserved*	OTP_Addr [3:0]*			
0x0A	0x00	R/W (*TEST)	**Control Register 10**							
			OTP_Data [7:0]*							
0x0B	0x00	R/W (*TEST)	**Control Register 11 / AdcCtrl [7:0]**							
			Reserved*	Toff 2 range selection [3:0]				ADC_Sel [2:0]		
0x0C	0x00	R	**Status Register_1**							
			Parity bit	BoostUV	DCmax	PWRderate	OpenLED1	ShortLED1	IndShortLED1	OCLED1
0x0D	0x00	R	**Status Register_2**							
			Parity bit	TW	TSD	SpiErr	OpenLED2	ShortLED2	IndShortLED2	OCLED2
0x0E	0x00	R	**Status Register_3**							
			ADC [7:0]							
0x0F	0x00	R/W (*TEST)	**Test Command(write) / RevID(read)**							
			RevID [7:0] (Note 20)							

Mapped in both, SPI and OTP address maps (with different address)

*Registers with write possibility only in TEST mode (TEST1 pin = high)
**Read−only registers as exception
A detailed description of the SPI registers follows in the next section.
20. RevID = 7dec (= [111] bin) for QAA silicon, RevID =6dec (= [110] bin) for PAA silicon (register 0x0F).

SPI REGISTERS DETAILS

Name	Control Register 1 /CR1: Dimming Duty Factor String 1 (DDF1)						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**01h**		**Access:**	**R/W**			
Bit	**Name**		**Description**				
7...0	DDF1[7:0]		Dimming Duty factor configuration for LED string 1.				

Name	Control Register 2 /CR2: Dimming Duty Factor String 2 (DDF2)						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**02h**		**Access:**	**R/W**			
Bit	**Name**		**Description**				
7...0	DDF2[7:0]		Dimming Duty factor configuration for LED string 2.				

Name	Control Register 3 /CR3: Current Setting LED String 1						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OTP LockInt	Current Setting LED string 1						
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**03h**		**Access:**	**R/W**			
Bit	**Name**		**Description**				
7	OTPLockInt		Read only register, part also of the OTP memory space. Write access only in test mode via OTP zap operation. If high, certain (indicated by the “*” symbol) set of OTP registers are protected against write/load access.				
6...0	DCS1[6:0]		Current Setting for LED String 1.				

Name	Control Register 4 /CR4: Current Setting LED String 2						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OTP LockExt	Current Setting LED String 2						
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**03h**		**Access:**	**R/W**			
Bit	**Name**		**Description**				
7	OTPLockExt		Read only register, part also of the OTP memory space. Write access only in test mode via OTP zap operation. If high, all OTP registers are protected against write/load access.				
6...0	DCS2[6:0]		Current Setting LED string 2.				

Name	Control Register 5 /CR5 : LED String 1 Diagnostics Individual Short Threshold						
7	6	5	4	3	2	1	0
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	05h		Access:	R/W			

Bit	Name	Description
7...0	ShortThr1[7:0]	LED String 1 diagnostics individual short threshold.

Name	Control Register 6 /CR6 : LED String 2 Diagnostics Individual Short Threshold						
7	6	5	4	3	2	1	0
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	06h		Access:	R/W			

Bit	Name	Description
7...0	ShortThr2[7:0]	LED String 2 diagnostics individual short threshold.

Name	Control Register 7 /CR7 : Booster Output Range / Booster Oscillator Frequency						
7	6	5	4	3	2	1	0
Booster DIS	Booster oscillator frequency			Booster output range			
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	07h		Access:	R/W			

Bit	Name	Description
7	BOOSTER_DIS	Booster Disable. Default value comes from OTP memory – bit[108].
6...4	BoostOscAppCnfg[2:0]	Booster oscillator frequency (related to resulting booster PWM frequency).
3...0	BoostOutRng[3:0]	Booster output range.

Name	Control Register 8 /CR8: Toff Range Selection / Dimming Freq. Factor						
7	6	5	4	3	2	1	0
Toff range selection				PWRDERATE_DIS	Dimming freq. factor		
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	08h		Access:	R/W			

Bit	Name	Description
7...4	ToffRngSel[3:0]	Toff range selection.
3	PwrDerate_DIS	When ‘0’ (default state) power derating is enabled.
2...0	DimFreqScl[2:0]	Dimming frequency factor.

Name	Control Register 9 /CR9/ : OTP Control						
7	6	5	4	3	2	1	0
OTP_Start	–	OTP_Cmd[1:0]		OTP_Addr[3:0]			
Reset Value:							
0	x	0	0	0	0	0	0
Reset Source: nReset/TEST							
Address:	09h		Access:	R/W* (in Test mode)			

Bit	Name	Description
7	OTP_Start	To write in this registers TEST pin needs to be set to ’1’. Set of OTP_Start bit executes the selected command – written in OTPCtrl [1:0] bits.
6...5	OTP_Cmd[1:0]	To write in this registers TEST pin needs to be set to ’1’. “00” – Point to OTP cell (read OTP without SPI registers refresh) “01” – Read OTP. Refresh OTP/SPI and provides for reading from OTP_DATA [7:0] “10” – Load OTP. Take data from OTP_DATA [7:0] and shift them in the OTP chain at the OTP_Addr [3:0] address, for emulation. “11” – Zap OTP. Take data from OTP_DATA [7:0] and zaps! the OTP, one bit at a time at OTP_Addr [3:0] address.
4	Reserved	Reserved bit. To be kept to zero in the application.
3...0	OTP_Addr[3:0]	Pre−defined OTP address to be accessed by the OTP_Cmd [1:0] command.

Name	Control Register 10 /CR10/ : OTP Data						
7	6	5	4	3	2	1	0
OTP_Data[7:0]							
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	0Ah		Access:	R/W			

Bit	Name	Description
7...0	OTP_Data [7:0]	Data used in case of OTP Load/Zap operation. In case the register is accessed for reading, data is taken directly from OTP_Addr [3:0] address.

Name	Control Register 11 /CR11: ADC Control						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADC_Tst_En	Toff 2 range selection [3:0]				ADC_Sel [2:0]		
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**0Bh**		**Access:**	**R/W**			

Bit	Name	Description
7	Reserved	Reserved bit. Can be written only with test1 = high and must be kept to zero in the application.
6...3	Toff 2 range selection [3:0]	Toff range selection.
2...0	ADC_Sel [2:0]	Control value to the mux, selecting the channel to be measured.

Name	Status Register 1 /SR1: LED1 Status						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAR	BoostUV,L	DCmax,L	PWRderate,L	OpenLED1, L	ShortLED1, L	IndShortLED1, L	OCLED1, L
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	**0Ch**		**Access:**	**R&C**			

Bit	Name	Description
7	PAR	Parity bit.
6	BoostUV	Booster is in undervoltage: Vboost_ADC_Value < Vboost_UNDERVOLTAGE. A filter time of 2ms is used in booster state machine before rising BoostUV flag to SPI and the rest of the logic.
5	DCmax	The duty cycle (DC) in Booster has reached DC_max limit.
4	PWRderate	Dimming module is in de−rating mode.
3	OpenLED1	Open line detected at LED1 string.
2	ShortLED1	Short circuit detected at LED1 string.
1	IndShortLED1	Individual short circuit detected at LED1 string.
0	OCLED1	Over−current detected at LED1 string.

Name	Status Register 2 /SR2: LED2 Status						
7	6	5	4	3	2	1	0
PAR	TW, L*	TSD, L	SPI_ERR, L	OpenLED2, L	ShortLED2, L	IndShortLED2, L	OCLED2, L
Reset Value:							
0	0	0	1	0	0	0	0
Reset Source: nReset							
Address:	0Dh		Access:	R&C			
Bit	Name	Description					
7	PAR	Parity bit.					
6	TW	Thermal warning event detected.					
5	TSD	Thermal shut event down detected.					
4	SPI_ERR	SPI frame not multiple of 16bits detected.					
3	OpenLED2	Open circuit detected at LED2 string.					
2	ShortLED2	Short circuit detected at LED2 string.					
1	IndShortLED2	Individual short circuit detected at LED2 string.					
0	OCLED2	Over−current detected at LED1 string.					

NOTE: Flags have “L” for latched information or “R” for real time information. All latched flags are “cleared upon read”.

Name	Status Register 3 /SR3/ : ADC						
7	6	5	4	3	2	1	0
ADC[7:0]							
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset							
Address:	0Eh		Access:	Read only			
Bit	Name	Description					
7...0	ADC [7:0]	SAR value loaded at the end of the conversion. In Normal mode read only access. In special Test mode, write access possible. In that Test mode, the value of the register is output to the Analog instead of the SAR register value.					

Name	Test Command − TstCmd / Revision ID − RevID						
7	6	5	4	3	2	1	0
Test Command Register / Revision ID							
Reset Value:							
0	0	0	0	0	0	0	0
Reset Source: nReset/TEST							
Address:	0Fh		Access:	R (W* in Reserved in TEST Mode)			
Bit	Name	Description					
7...0	TstCmd [7:0]	Special write test command in case of TEST1= high. ONSEMI reserved.					
7...0	RevID [7:0]	Reads the device revision ID (silicon mask release). RevID = 7dec (= [111] bin) for QAA silicon, RevID =6dec (=[110] bin) for PAA silicon.					

OTP

Description

The OTP (One Time Programmable) Memory contains 109 bits; 37 bits are for trimming purposes and are programmed at the end of the silicon manufacturing line at ON Semiconductor. The remaining 72 bits are system dependent parameters and are user programmable via the SPI interface and the “ZAP!” operation: these should be considered as the power−up default operating parameters and are typically programmed at the end of the module manufacturing line.

The OTP−bits, as the name suggests, can be programmed only once. However, this is not a limiting factor as the system dependent parameters can be updated after power−up via the SPI−interface (the only two exceptions are the boost control rate and the DIAGx response mode, see OTP address map).

The OTP Controller operates:

1. either at Startup, to load the default values from OTP to the SPI registers,
2. or when the chip is set in Test mode, to get full OTP access depending on the status of the OTPLock−bits.

OTP Interface

The OTP memory is controlled via 2 SPI control registers (CR9 and CR10) and the TEST1−pin, which must be high during OTP operations.

Control Register

SPI−CR9 acts as the OTP Control register **OTP_CTRL [7:0]**:

OTP_CTRL [7] START bit: Set of START bit starts execution of the selected command;

OTP_CTRL [6:5] Command to be executed. The CMD [1:0] list is reported in the table below;

OTP_CTRL [3:0] OTP Address to be accessed.

OTP_CMD	Bit Code	Name	Description
CMD_01	“00”	Point to OTP cell	Copies selected OTP cell value into OTP DATA register. No start bit is needed.
CMD_02	“01”	Read OTP cell & refresh	Copies selected OTP cell value into OTP DATA register and load all OTP data registers into SPI registers, generating a complete refresh. WARNING: as a consequence, all previously contained values in the SPI registers are overwritten with the OTP content.
CMD_03	“10”	Load OTP	Shifts OTP_DATA [7:0] in the OTP chain at the corresponding OTP address, ready for zapping. As OTP_CMD_01, this operation generates a full SPI registers refresh.
CMD_04	“11”	Zap! OTP	The loaded OTP data is zapped in the corresponding OTP register (1 bit by 1). As CMD_01 and CMD_10, this operation generates a full SPI registers refresh. Once zapped to “1”, a single bit may not be zapped to “0” anymore.

Data Register

SPI−CR10 acts as the OTP Data register **OTP_DATA [7:0]:**

- When accessed for write (through the SPI), that register keeps the data to be used in a “Load OTP” operation
- When accessed for read (through the SPI), the data is taken directly from the OTP registers.

Programming OTP or “Zap!”

Set of OTP_Start bit starts execution of the selected command, written in OTP_CTRL [6:5] bits. At that very moment the OTP address to be accessed, written in OTP_CTRL [3:0] bits, is latched and is kept there until the operation finishes. When OTP state machine completes the command, it clears automatically OTP_Start bit. This allows monitoring the status of the operation by polling of the OTP_Start via SPI.

Important Note 1: at the end of the execution of every OTP command (Read, Load, Zap), all the values in the OTP banks are refreshed loaded into the corresponding registers of the SPI. That is to say, the SPI registers are reset to power−up default. The only exception is “Point to OTP Cell” command.

Important Note 2: in order to insure successful OTP programming, VBB input must be higher than 12 V and the maximum ambient temperature is 30°C (see Table 3). It is recommended to launch OTP ZAP! only when the LED outputs are off, ensuring minimum application noise.

OTP Lock

To prevent unwanted OTP zapping, there is the possibility to the OTP in 2 stages. Once a lock is set, it cannot be released anymore. Prior to any lock operation the correct content of the OTP bank must be checked.

Factory Trimming OTP Lock

The bit *OTPLockInt* will be set at the end of the silicon manufacturing line at ON Semiconductor, after device trimming. By doing so, the factory trimming parameters can never be changed by the user as a safety feature.

User OTP Lock

The bit OTPLockExt allows the user to protect the system dependant parameters which are typically programmed at the end of the module manufacturing line. These parameters will be the system default parameters after power−up. We strongly recommend making use of this lock to avoid unwanted setting changes in the application and to keep TEST1 to GND.

Table 27. OTP ADDRESS MAP

OTP Address	Bit N	7	6	5	4	3	2	1	0
0x00	7	Dimming duty factor LED string 1 [7:0]							
0x01	15	Dimming duty factor LED string 2 [7:0]							
0x02	23	OTPLockInt*	Current setting LED string 1 [6:0]						
0x03	31	OTPLockExt	Current setting LED string 2 [6:0]						
0x04	39	LED String 1 diagnostics individual short threshold [7:0]							
0x05	47	LED String 2 diagnostics individual short threshold [7:0]							
0x06	55	Toff 1 range selection [3:0]				Booster output range [3:0]			
0x07	63	Booster oscillator frequency [2:0]			Booster oscillator accuracy trimming[4:0]*				
0x08	71	Bandgap accuracy trimming [2:0]*			System oscillator accuracy trimming [4:0]*				
0x09	79	Toff 1 accuracy trimming [3:0]*				Bandgap accuracy trimming [6:3]*			
0x0A	87	DIAGx response mode	Boost control rate [2:0]			TSD accuracy trimming [3:0]*			
0x0B	95	Toff 2 accuracy trimming [3:0]*				Toff 2 range selection [3:0]			
0x0C	103	BandGap opamp N−trimming [2:0]*			BandGap opamp P−trimming[4:0]*				
0x0D	111	Not used			BOOSTER_DIS	PWRDERATE_DIS	Dimming freq. factor [2:0]		
0x0E	119	Not used							

Mapped in both, SPI and OTP address maps (same naming but different address)

*Only for ON Semiconductor trimming purpose. Locked if OTPLockInt−bit is set.

DIAGNOSTICS

The NCV78663 offers a wide range of device−integrated diagnostic features. Their description follows.

Diagnostics Description

- **Thermal Warning**: this mechanism detects a junction temperature which is close but lower to the chip maximum allowed, providing the information that some action is required to prevent overheating causing Thermal Shutdown. The thermal warning condition will automatically generate a power derating action by reducing the output duty cycle to 75% of the original value. See Section Automatic Power de−rating.
- **Booster reached maximum duty cycle**: the booster controller has set the maximum duty cycle to the gate PWM. This means that the booster is not capable to deliver the required energy to the output. Reasons could be either:
  - input current limit is insufficient;
  - input current line to the inductor or MOSFET open;
  - too high load required by the booster and/or too low supply level V_BAT.
- **Thermal Shutdown**: The junction temperature has reached the TSD level (see Table at 4.9). The booster and the LED outputs are immediately disabled to prevent device overheating. The TSD flag is latched in the SPI SR2 (State 2) register and stays set until the SR2 register is read by the SPI Master. On the other hand, booster and buck converters disable logic is using the real time TSD and TW signals (not the SPI flags), so that only after both TSD and TW real internal signals disappear, booster and buck converters will be again automatically enabled. This is done to make sure that device can recover also in stand−alone mode (no MCU or SPI Master in the system). The normal operation of booster and buck converters is restored only after the temperature drops below the TW level − thus providing hysteresis for the TSD recovery process.
- **Power derating warning**: Indicates that the power de−rating function has been activated. See Section Automatic Power De−rating.
- **SPI Error**: SPI frame detected with a length not equal to a multiple of 16 bits.
- **Boost under voltage error**: Detects a boost under voltage by raising the related bit and lowering both DIAGx pins to zero. The Boost voltage error bit in SPI status register is cleared in case of being read or in case of longer than 50 ms low pulse at LEDCTRLx pin. A 50 ms low pulse on the LEDCTRLx releases the relative DIAGx pin as well.
- **Detection of 'open' LED−string**: detects if the LED output voltage has reached the reference minimum booster voltage for the specific range as defined in the table below. The DIAGx pin remains zero as long as low pulse longer than 50 ms is not detected at LEDCTRLx pin. The Open LED−string error bit in SPI status register is cleared in case of being read or in case of longer than 50 ms low pulse at LEDCTRLx pin.

Table 28. OPEN LOAD DIAGNOSTIC DETECTION LEVEL AND BOOST UNDERVOLTAGE DETECTION LEVELS

Open load detection VLED (V) / Vboost under voltage (V)	13	13	13	15	18	20	23	25	28	30	33	35	38	40	45	55
Boost selected RANGE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Another way to detect the open load condition is to compare the VLEDx voltage to the Vboost voltage by means of the internal NCV78633 SPI and ADC. If the LED voltage goes in a range comparable with the boost voltage (E.G. difference of less than 2 V), it means that the load is open as the boost voltage transfers directly at the output.

- **Detection of 'shorted' LED−string**: the corresponding error bit is set when the LED voltage is below the threshold level, fixed at 1.9V, with absolute ADC value 06hex typical. The DIAGx pin remains to low value until a low state longer than 50 ms is detected at LEDCTRLx pin. The short error bit in SPI status register is cleared in case of being read or in case of longer than 50 ms low level at LEDCTRLx pin.
- **Detection of individual shorted LED**: the absolute LED−string voltage is monitored and compared to an user−programmable threshold level:

$$\mathrm{IndShortThres_x[V]} = 80 \times \frac{\mathrm{IndShortThres_{SPI_REGx}(dec)}}{255}.$$

The default value is fixed in OTP and can be overwritten in a volatile register by a specific SPI command. If the LED−string voltage drops below that absolute level, the chips recognizes single or more shorted LEDs and the error bit is raised in the relative STATUS register (1 or 2). No specific action taken on the DIAGx pins based on this detection.

Note: depending on the total number of LED in the string, their forward voltage tolerance and temperature drift, it might happen that this simple detection scheme will detect the error after at least two series LEDs are shorted. If necessary, a more complex single shorted LED algorithm can then be implemented directly by an external

microcontroller, taking direct advantage of the measured LED voltage via the SPI interface.

- **Buck regulator over−current error (OCLEDx)**: this error condition is triggered if the buck current is higher than the OCD level (see Table 15) for 16 consecutive buck periods and the responsible channel is switched off. The conditions for clearing the OCLEDx bits is reading the related SPI STATUSx or keeping LEDCTRLx = 0 for 50 ms.

Diagnostics Feedback

Any error which leads to a non−functional LED string is reported via the DIAGx (1, 2) pins.

Each LED output driver has its own diagnostics output DIAGx. Depending on the DIAGx response mode option (OTP map register 0x0A − bit 7), the behavior of the DIAGx can be either “static” (default, bit = 0) or “pulsed” (bit = 1). In the default case, when the LEDx line is active, the DIAGx is continuously high, providing there is no error detected in the respective LEDx string. Otherwise, if the DIAGx response mode is programmed to “one”, the pulse starts typically at the beginning of LED turn−on and is one−shot high for a duration of 500 ms if no errors are detected.

All LED string related errors and boost under voltage error are latched and get cleared when the inputs (LEDCTRLx) are disabled for a time longer than 50 ms.

The DIAGx is continuously low if there is any of the responsible errors detected in the respective LED string persists, as summarized in the Diagnostics Summary Table.

Table 29. DIAGNOSTICS SUMMARY TABLE

Diagnose		Detection Level Setting	DIAGx Feedback	LED Output	Reset Via:		SPI Register
Abbreviation	Description				LEDTRLx	SPI	
BoostUV	Boost undervoltage	Fixed to boost range	DIAG1 & 2	No change	Y	Y	SR1.[6]
TW	Thermal Warning	See Section On−chip temperature sensor	No	See Section Automatic Power De−rating	N	N	SR2.[6]
DCmax	Booster reached Maximum Dutycycle	f(boost range, vBat).	No	No change	N	Y	SR1.[5]
TSD	Thermal Shutdown	See Section On−chip temperature sensor	DIAG1 & 2	Disabled. (Re−enabled automatically below TW level)	N	Y	SR2.[5]
PWRderate	Power de−rating	f(V_bat, TW, PwrDerate_Enb)	No	See Automatic Power De−rating	N	Y	SR1.[4]
SpiErr	SPI frame not multiple of 16 bits	N.A.	No	No change	No	Y	SR2.[4]
OpenLED**x***	LED string open circuit	V_LED**x** > VLED_OpenThres	DIAG**x***	No change	Y	Y	SR**x.**[3]*
ShortLED**x***	LED string short circuit	V_LED**x** < 1.9 V	DIAG**x***	No change	Y	Y	SR**x.**[2]*
IndShortLED**x***	Individual LED shorted	V_LEDx < individual short threshold	No	No change	Y	Y	SR**x.**[1]*
OCLED**x***	LED string Over Current	I_Buckswitch > OCD See Section Buck Regulator − Switch	DIAG**x***	Disabled	Y	Y	SR**x.**[0]*

*...**x** = ...1 or ...2
** See Table 28

PCB LAYOUT RECOMMENDATIONS

This section contains instructions for the NCV78663 PCB layout application design. Although this guide does not claim to be exhaustive, these directions can help the developer to reduce application noise impact and insuring the best system operation.

The areas which are most critical for a layout point of view are highlighted in the following picture:

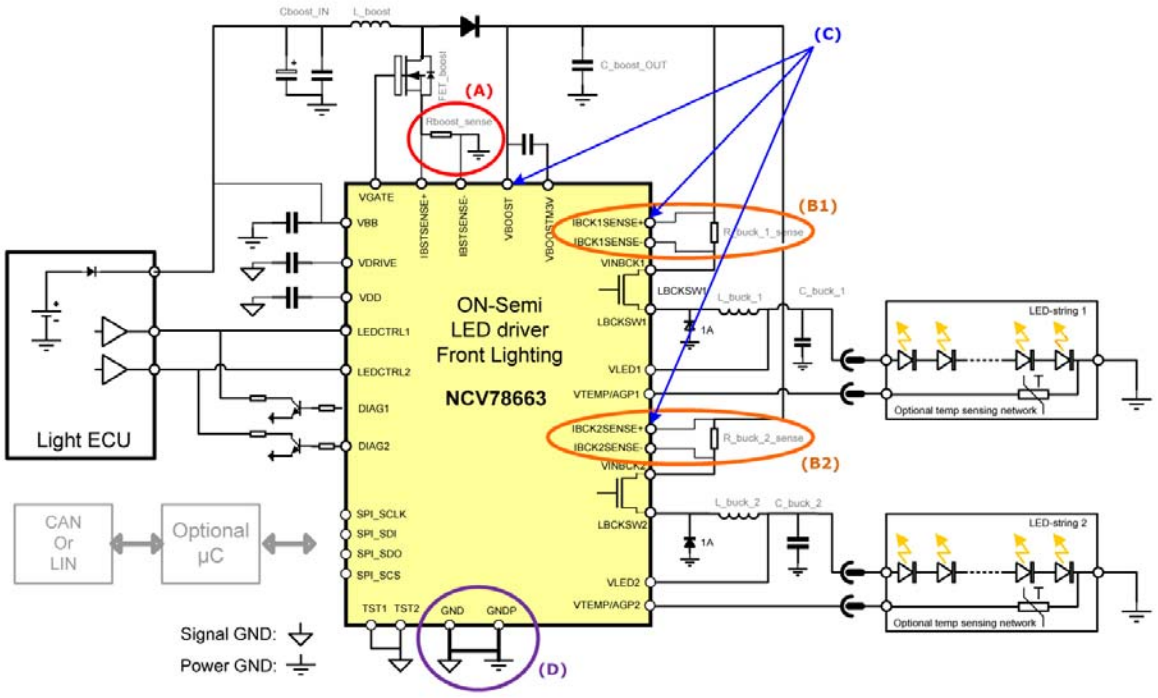


Figure 18. NCV78663: Application Critical Areas at PCB Level

Booster Current Limitation Circuit: AREA (A)

The booster limitation circuit relies on a low voltage comparator, which triggers with respect to the sense voltage across the external resistor Rboost_sense. In order to maximize power efficiency, the threshold voltage is set to a rather low value by design (typical 100 mV, see Table 13) and this area may be affected by the MOSFET switching noise if no specific care is taken. The following recommendations are given:

A. Use a four terminals current sense method as depicted in the figure below. The measurement PCB tracks should run in parallel and as close as possible to each other, trying to have the same length. The number of vias along the measurement path should be minimized;
B. Place Rboost_sense sufficiently close to the MOSFET source terminal;
C. The MOSFET's dissipation area should be stretched in a direction away from the sense resistor to minimize resistivity changes due to heating;
D. Possibly reduce to the least the distance between Rboost_sense and the NCV78663 boost limitation comparator's inputs (IBSTSENSE+ and IBSTSENSE−);
E. If the current sense measurement tracks are interrupted by series resistors or jumpers (once as a maximum) their value should be matched and low ohmic (pair of 0 Ω to 47 Ω max) to avoid errors due to the comparator input bias currents;
F. Avoid using the board GND as one of the measurement terminals as this would also introduce errors.

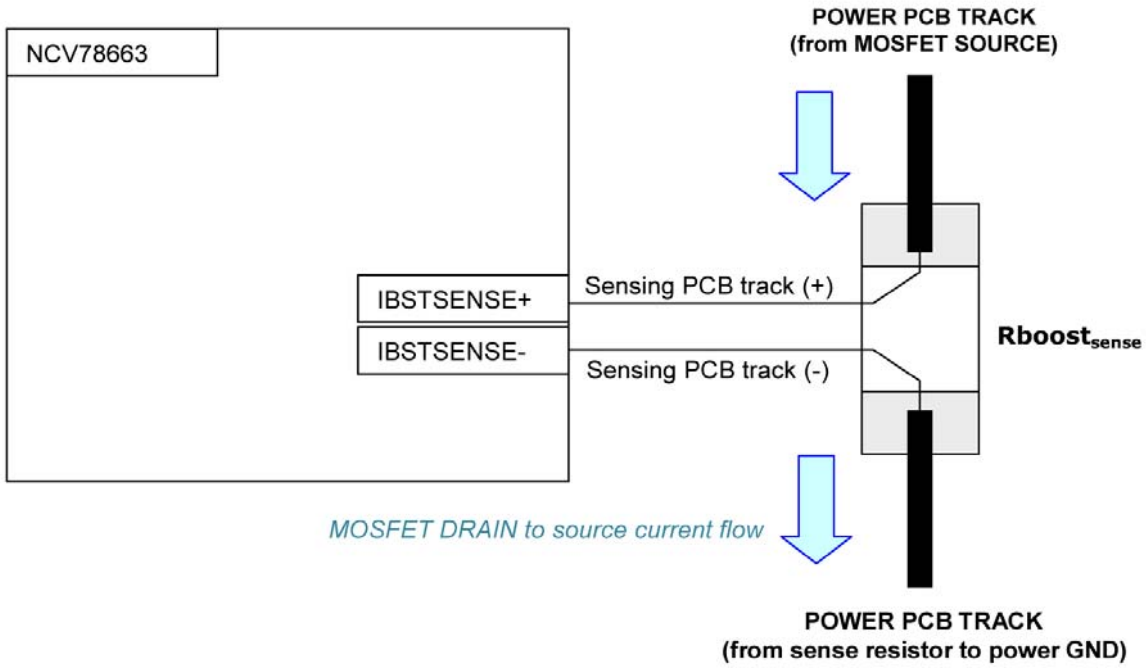


Figure 19. Four Wires Sensing Method for Boost Current Limitation Comparator

Buck Current Comparators: AREAs (B1) and (B2)

The blocks (B1) and (B2) control the buck peak currents by means, respectively, of the external sense resistors Rbuck_1_sense and R_buck_2_sense. As the regulation is performed with a comparator, the considerations explained in the previous section “Booster Current Limitation Circuit: AREA (A)” remain valid.

In particular, the use of a four terminals current sense method is required, this time applied on (IBCK1xSENSE+, IBCKxSENSE−). The sensing PCB tracks should be kept as short as possible, with the sense resistors close to the device, but preferably outside of its PCB heating area in order to limit measurement errors produced by temperature drifts.

Vboost Related Tracks: AREA (C)

The three NCV78663 device pins VBOOST, IBCK1SENSE+ and IBCK2SENSE+ must be at the same individual voltage potential to guarantee proper functioning of the internal buck current comparator (whose supply rails are Vboost and VboostM3V). In order to achieve this target, it is suggested to make a PCB star track connection between these three points close to the device pins. The width of the tracks should be large enough (>40 mils) and their length as balanced as possible (ideally all equal).

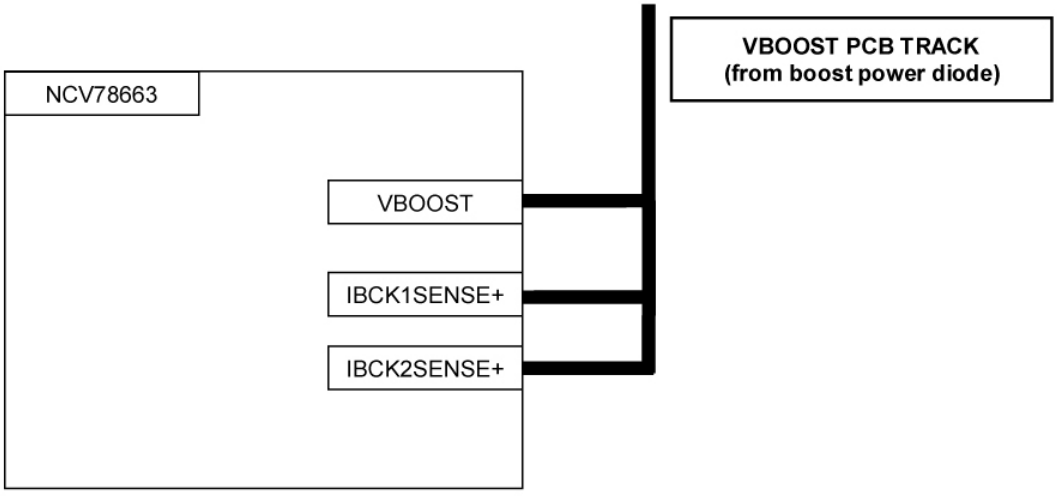


Figure 20. PCB Star Connection Between Vboost, IBCK1SENSE+ and IBCK2SENSE+ (simplified drawing)

GND Connection: AREA (D)

The NCV78663 GND and GNDP pins must be connected together. It is suggested to perform this connection directly close to the device, behaving also as the cross-junction between the signal GND (all low power related functions) and the power GND (related to all power switching areas). The device exposed pad should be connected to the GND plane for dissipation purposes.

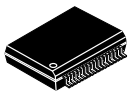
ORDERING INFORMATION

Device	Package	Shipping†
NCV78663DQ0G	SSOP36 EP (Pb−Free)	47 Units / Rail
NCV78663DQ0R2G	SSOP36 EP (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

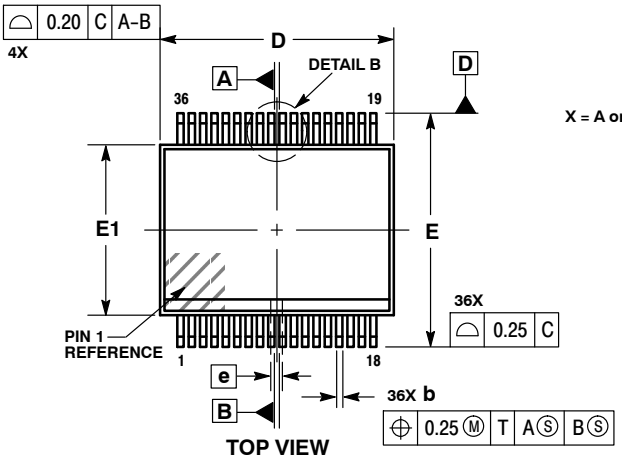
ON Semiconductor®

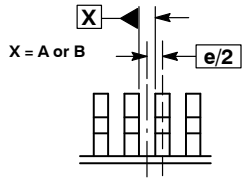


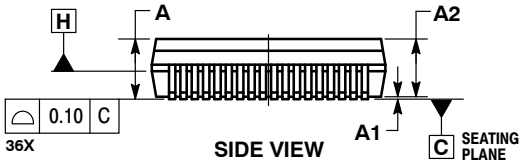
SCALE 1:1

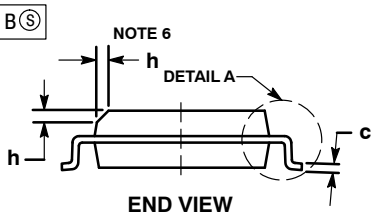
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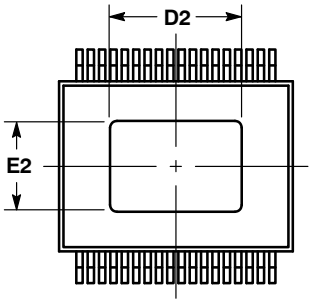


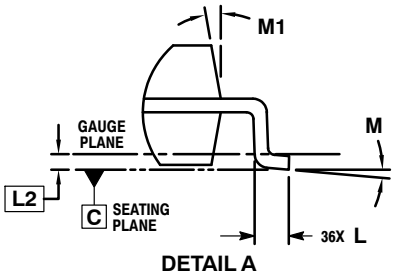




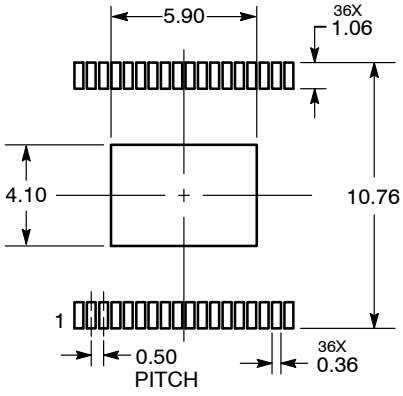
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICATED AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.65
A1	---	0.10
A2	2.15	2.60
b	0.18	0.30
c	0.23	0.32
D	10.30 BSC	
D2	5.70	5.90
E	10.30 BSC	
E1	7.50 BSC	
E2	3.90	4.10
e	0.50 BSC	
h	0.25	0.75
L	0.50	0.90
L2	0.25 BSC	
M	0°	8°
M1	5°	15°



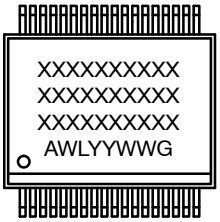


SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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