NLMD5820

2.65 W Filterless Class-D Audio Amplifier with Integrated Dual SPST Switch

The NLMD5820 is an integrated mono Class−D audio power amplifier and dual SPST switch capable of delivering 2.65 W of continuous average power to 4.0 Ω from a 5.0 V supply in a Bridge Tied Load (BTL) configuration. Under the same conditions, the output power stage can provide 1.4 W to a 8.0 Ω BTL load with less than 1% THD+N. For cellular handsets or PDAs it offers space and cost savings because no output filter is required when using inductive tranducers. The NLMD5820 incorporates a dual SPST switch which allows signals to bypass the amplifier. The integrated switch operates off a separate supply voltage and maintains a very low R_{ON} resistance, 0.5 Ω max @ 2.8 V V_{CC}.

The NLMD5820 processes analog inputs with a pulse width modulation technique that lowers output noise and THD when compared to a conventional sigma−delta modulator. The device allows independent gain while summing signals from various audio sources. Thus, in cellular handsets, the earpiece, the loudspeaker and even the melody ringer can be driven with a single NLMD5820. Due to its low 42 μV noise floor, A−weighted, clean listening is guaranteed no matter the load sensitivity.

Features

- Optimized PWM Output Stage: Filterless Capability
- Efficiency up to 90%
  Low 2.5 mA Typical Quiescent Current
- Large Output Power Capability: 1.4 W with 8.0 Ω Load (CSP) and THD + N < 1%
- Dual SPST with 0.5 Ω Max R_{ON} @ V_{CC} = 2.8 V
- High Performance, THD+N of 0.03% @ V_p = 5.0 V,
  R_L = 8.0 Ω, P_{out} = 100 mW
- Excellent PSRR (−65 dB): No Need for Voltage Regulation
- Surface Mounted Package UDFN16
- Fully Differential Design. Eliminates Two Input Coupling Capacitors
- Very Fast Turn On/Off Times with Advanced Rising and Falling Gain Technique
- External Gain Configuration Capability
- Internally Generated 250 kHz Switching Frequency
- Short Circuit Protection Circuitry
- “Pop and Click” Noise Protection Circuitry
- This is a Pb−Free Device

Applications

- Cellular Phone
- Portable Electronic Devices
- PDAs and Smart Phones

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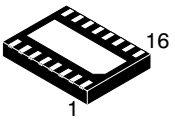
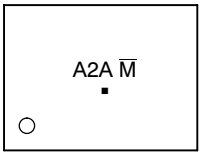
MARKING DIAGRAM

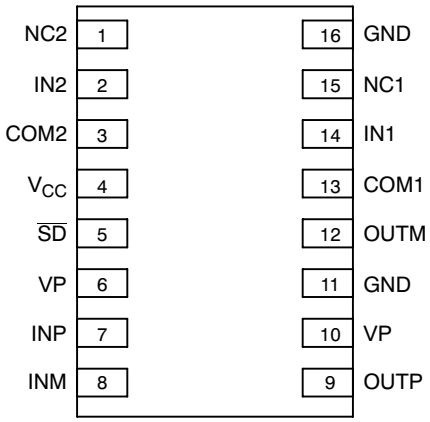


16 PIN UDFN
CASE 517AL



A2A = Specific Device Code
M = Date Code/Assembly Location
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NLMD5820MUTAG	16 PIN UDFN (Pb−Free)	3000/Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

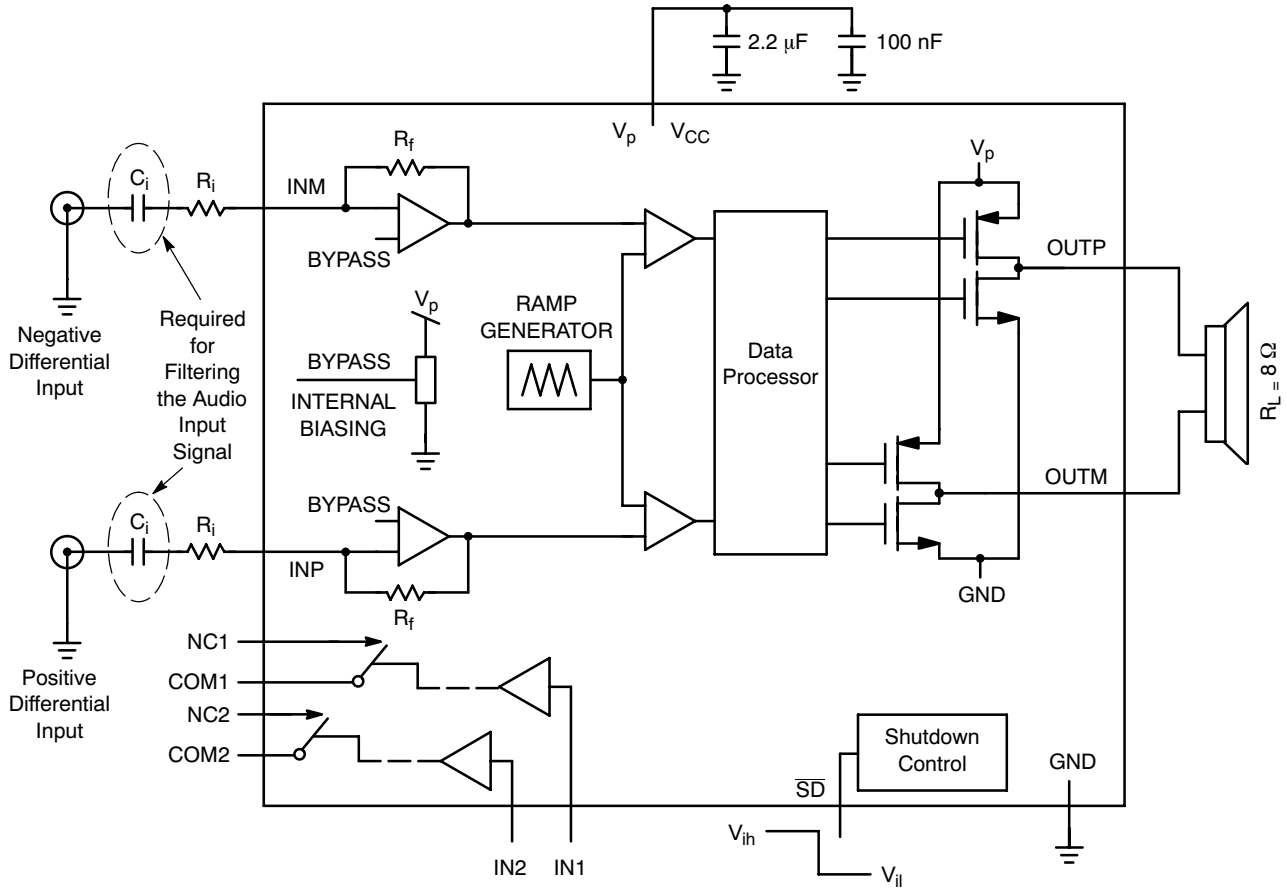


Figure 1. Functional Block Diagram

FUNCTION TABLE

IN 1, 2	NC 1, 2
0	ON
1	OFF

PIN DESCRIPTION

Pin No.	Symbol	Type	Description
1	NC2	I/O	Normally Closed Signal Line for Switch #2.
2	IN2	I	Control Input for Switch #2.
3	COM2	I/O	Common Signal Line for Switch #2.
4	V_{CC}	I	Analog Supply for Switches. Range: 1.65 V – 4.5 V.
5	$\overline{SD}$	I	The device enters in Shutdown Mode when a low level is applied on this pin. An internal 300 kΩ resistor will force the device in shutdown mode if no signal is applied to this pin. It also helps to save space and cost.
6	V_p	I	Power Analog Positive Supply. Range: 2.5 V – 5.5 V.
7	INP	I	Positive Differential Input.
8	INM	I	Negative Differential Input.
9	OUTP	O	Positive BTL Output.
10	V_p	I	Analog Positive Supply. Range: 2.5 V – 5.5 V.
11	GND	I	Analog Ground.
12	OUTM	O	Negative BTL Output.
13	COM1	I/O	Common Signal Line for Switch #1.
14	IN1	I	Control Input for Switch #1.
15	NC1	I/O	Normally Closed Signal Line for Switch #1.
16	GND	I	Analog Ground.

MAXIMUM RATINGS

Symbol	Rating		Max	Unit
V_p	Supply Voltage for Amplifier	Active Mode Shutdown Mode	6.0 7.0	V
V_{in}	Input Voltage for Amplifier		−0.3 to V_{CC} +0.3	V
V_{CC}	Supply Voltage for Switches		−0.5 to +5.5	V
V_{IS}	Analog Signal Voltage for Switches (V_{NC}, or V_{COM})		$-0.5 \le V_{IS} \le V_{CC} + 0.5$	V
V_{IN}	Control Input for Switches		$-0.5 \le V_{IN} \le +5.5$	V
I_{out}	Max Output Current of Amplifier (Note 1)		1.5	A
I_{anl1}	Continuous DC Current from COM to NC		±300	mA
$I_{anl-pk1}$	Peak Current from COM to NC, 10 Duty Cycle		±500	mA
I_{clmp}	Continuous DC Current into COM/NC with Respect to V_{CC} or GND		±100	mA
P_d	Power Dissipation (Note 2)		Internally Limited	–
T_J	Max Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	UDFN16	50	°C/W
– –	ESD Protection Human Body Model (HBM) (Note 3) Machine Model (MM) (Note 4)		> 2000 > 200	V
–	Latchup Current @ T_A = 85°C (Note 5)	UDFN16	±100	mA
MSL	Moisture Sensitivity (Note 6)		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The device is protected by a current breaker structure. See “Current Breaker Circuit” in the Description Information section for more information.
2. The thermal shutdown is set to 160°C (typical) avoiding irreversible damage to the device due to power dissipation.
3. Human Body Model: 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
4. Machine Model: 200 pF discharged through all pins following specification JESD22/A115.
5. Latchup Testing per JEDEC Standard JESD78.
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Unit
V_P	Supply Voltage for Amplifier	2.5 to 5.5	V
V_{CC}	Supply Voltage for Switches	1.65 to 4.5	V
V_{IS}	Analog Signal Voltage for Switches	GND to V_{CC}	V
V_{IN}	Control Input for Switches	GND to V_{CC}	V
T_A	Operating Ambient Temperature	−40 to +85	°C

ELECTRICAL CHARACTERISTICS OF AMPLIFIER (Limits apply for T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Supply Quiescent Current	I_{dd}	V_p = 3.6 V, R_L = 8.0 Ω	–	2.15	–	mA
		V_p = 5.5 V, No Load	–	2.61	–	
		V_p from 2.5 V to 5.5 V, No Load				
		T_A = −40°C to +85°C	–	–	3.8	
Shutdown Current	I_{sd}	V_p = 4.2 V				μA
		T_A = +25°C	–	0.42	0.8	
		T_A = +85°C	–	0.45	2.0	
		V_p = 5.5 V				μA
		T_A = +25°C	–	0.8	1.5	
		T_A = +85°C	–	0.9	–	
Shutdown Voltage High	V_{sdih}	–	1.2	–	–	V
Shutdown Voltage Low	V_{sdil}	–	–	–	0.4	V
Switching Frequency	F_{sw}	V_p from 2.5 V to 5.5 V	180	240	300	kHz
		T_A = −40°C to +85°C				
Gain	G	R_L = 8.0 Ω	$\frac{285\ k\Omega}{R_i}$	$\frac{300\ k\Omega}{R_i}$	$\frac{315\ k\Omega}{R_i}$	$\frac{V}{V}$
Output Impedance in Shutdown Mode	Z_{SD}	–	–	20	–	kΩ
Resistance from $\overline{SD}$ to GND	Rs	–	–	300	–	kΩ
Output Offset Voltage	Vos	V_p = 5.5 V	–	6.0	–	mV
Turn On Time	Ton	V_p from 2.5 V to 5.5 V	–	1.0	–	μs
Turn Off Time	Toff	V_p from 2.5 V to 5.5 V	–	1.0	–	μs
Thermal Shutdown Temperature	Tsd	–	–	160	–	°C
Output Noise Voltage	Vn	V_p = 3.6 V, f = 20 Hz to 20 kHz				μVrms
		no weighting filter	–	65	–	
		with A weighting filter	–	42	–	
RMS Output Power	Po	R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 1%				W
		V_p = 2.5 V	–	0.22	–	
		V_p = 3.0 V	–	0.33	–	
		V_p = 3.6 V	–	0.45	–	
		V_p = 4.2 V	–	0.67	–	
		V_p = 5.0 V	–	0.92	–	
		R_L = 8.0 Ω, f = 1.0 kHz, THD+N < 10%				W
		V_p = 2.5 V	–	0.36	–	
		V_p = 3.0 V	–	0.53	–	
		V_p = 3.6 V	–	0.76	–	
		V_p = 4.2 V	–	1.07	–	
		V_p = 5.0 V	–	1.49	–	
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 1%				W
		V_p = 2.5 V	–	0.24	–	
		V_p = 3.0 V	–	0.38	–	
		V_p = 3.6 V	–	0.57	–	
		V_p = 4.2 V	–	0.83	–	
		V_p = 5.0 V	–	1.2	–	
		R_L = 4.0 Ω, f = 1.0 kHz, THD+N < 10%				W
		V_p = 2.5 V	–	0.52	–	
		V_p = 3.0 V	–	0.8	–	
		V_p = 3.6 V	–	1.125	–	
		V_p = 4.2 V	–	1.58	–	
		V_p = 5.0 V	–	2.19	–	
Efficiency	–	R_L = 8.0 Ω, f = 1.0 kHz				%
		V_p = 5.0 V, P_{out} = 1.2 W	–	87	–	
		V_p = 3.6 V, P_{out} = 0.6 W	–	87	–	
		R_L = 4.0 Ω, f = 1.0 kHz				
		V_p = 5.0 V, P_{out} = 2.0 W	–	79	–	
		V_p = 3.6 V, P_{out} = 1.0 W	–	78	–	

ELECTRICAL CHARACTERISTICS OF AMPLIFIER (Limits apply for T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	THD+N	V_p = 5.0 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W V_p = 3.6 V, R_L = 8.0 Ω, f = 1.0 kHz, P_{out} = 0.25 W	 – –	 0.05 0.06	 – –	%
Common Mode Rejection Ratio	CMRR	V_p from 2.5 V to 5.5 V V_{ic} = 0.5 V to V_p – 0.8 V V_p = 3.6 V, V_{ic} = 1.0 V_{pp} f = 217 Hz f = 1.0 kHz	 – – –	 –62 –56 –57	 – – –	dB
Power Supply Rejection Ratio	PSRR	$V_{p\_ripple\_pk-pk}$ = 200 mV, R_L = 8.0 Ω, Inputs AC Grounded V_p = 3.6 V f = 217 kHz f = 1.0 kHz	 – –	 –62 –65	 – –	dB

DC ELECTRICAL CHARACTERISTICS OF SWITCHES

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Control Input High Voltage	V_{IH}	VCC = 3.0 V VCC = 4.2 V	1.4 2.0			V
Control Input Low Voltage	V_{IL}	VCC = 3.0 V VCC = 4.2 V			0.7 0.8	V
Control Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		±0.1	±1.0	μA
ON State Leakage Current	$I_{COM(ON)}$	0 V < V_{COM}, V_{NC} < V_{CC}		±10	±100	nA
OFF State Leakage Current	$I_{NC(OFF)}$	0 V < V_{COM}, V_{NC} < V_{CC}		±5	±50	nA
Quiescent Current	I_{CC}	All Channels ON or OFF, V_{IN} = V_{CC} or GND, I_{OUT} =0		±1.0	±2.0	μA
ON Resistance	R_{ON}	VCC = 3.0 V VCC = 4.2 V		0.4 0.35	0.5 0.4	Ω Ω
R_{ON} Flatness	R_{FLAT}	VCC = 3.0 V VCC = 4.2 V		0.16 0.11	0.20 0.14	Ω Ω
R_{ON} Matching	ΔR_{ON}	VCC = 3.0 V VCC = 4.2 V		0.05 0.05	0.05 0.05	Ω Ω

AC ELECTRICAL CHARACTERISTICS OF SWITCHES (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{ON}	Turn−On Time	R_L = 50 Ω, C_L = 35 pF (Figures 43 and 44)		50		ns
t_{OFF}	Turn−Off Time	R_L = 50 Ω, C_L = 35 pF (Figures 43 and 44)		30		ns
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0 V		3.5		pF
C_{NC}	NC Port Capacitance	V_{CC} = 3.3 V, V_{IN} = 0 V		60		pF
C_{COM}	COM Port Capacitance When Switch is Enabled	V_{CC} = V_{IN} = 3.3 V		200		pF
BW	Maximum On−Channel −3 dB Bandwidth or Minimum Frequency Response	V_{IN} centered between V_{CC} and GND (Figure 45)		19		MHz
V_{ONL}	Maximum Feed−through On Loss	V_{IN} = 0 dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 45)		−0.06		dB
V_{ISO}	Off−Channel Isolation	f = 100 kHz; V_{IS} = 1 V RMS; C_L = 5.0 pF V_{IN} centered between V_{CC} and GND (Figure 45)		−68		dB
Q	Charge Injection Select Input to Common I/O	V_{IN} = V_{CC} to GND, R_{IS} = 0 Ω, C_L = 1.0 nF Q = C_L x DV_{OUT} (Figure 46)		38		pC
THD	Total Harmonic Distortion THD + Noise	F_{IS} = 20 Hz to 20 kHz, R_L = R_{gen} = 600 Ω, C_L = 50 pF, V_{IS} = 2.0 V RMS		0.08		%
VCT	Channel−to−Channel Crosstalk	f = 100 kHz; V_{IS} = 1.0 V RMS, C_L = 5.0 pF, R_L = 50 Ω V_{IN} centered between V_{CC} and GND (Figure 45)		−70		dB

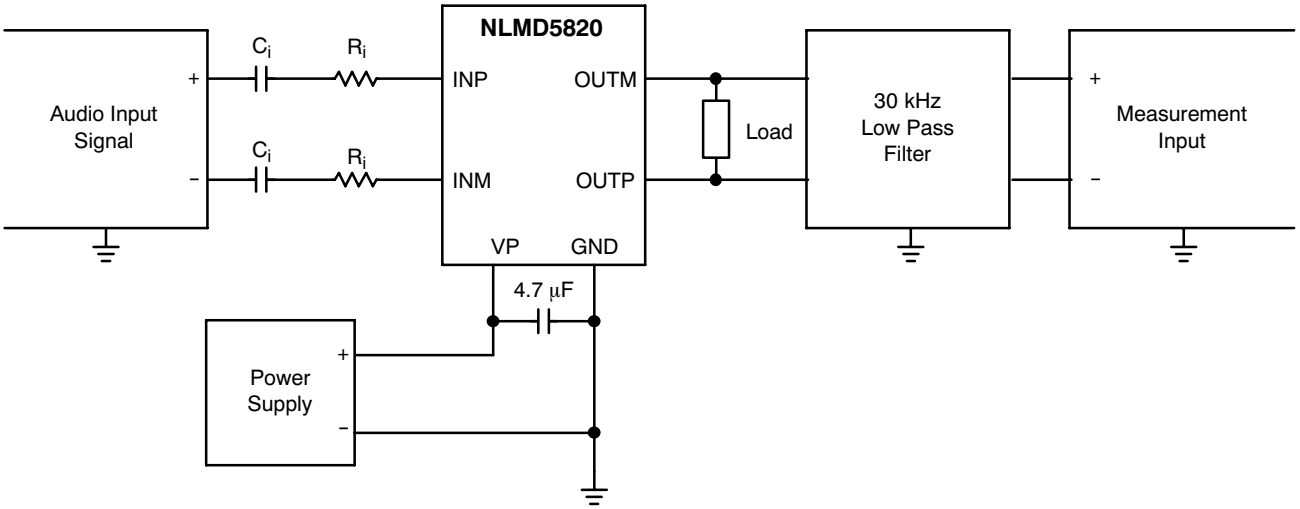


Figure 2. Test Setup for Typical Characteristics (Figures 3 − 34)

NOTES:

1. Unless otherwise noted, C_i = 100 nF and R_i= 150 kΩ. Thus, the gain setting is 2 V/V and the cutoff frequency of the input high pass filter is set to 10 Hz. Input capacitors are shorted for CMRR measurements.
2. To closely reproduce a real application case, all measurements are performed using the following loads:
   R_L = 8 Ω means Load = 15 μH + 8 Ω + 15 μH
   R_L = 4 Ω means Load = 15 μH + 4 Ω + 15 μH
   Very low DCR 15 μH inductors (50 mΩ) have been used for the following graphs. Thus, the electrical load measurements are performed on the resistor (8 Ω or 4 Ω) in differential mode.
3. For Efficiency measurements, the optional 30 kHz filter is used. An RC low−pass filter is selected with (100 Ω, 47 nF) on each PWM output.

TYPICAL CHARACTERISTICS OF AMPLIFIER

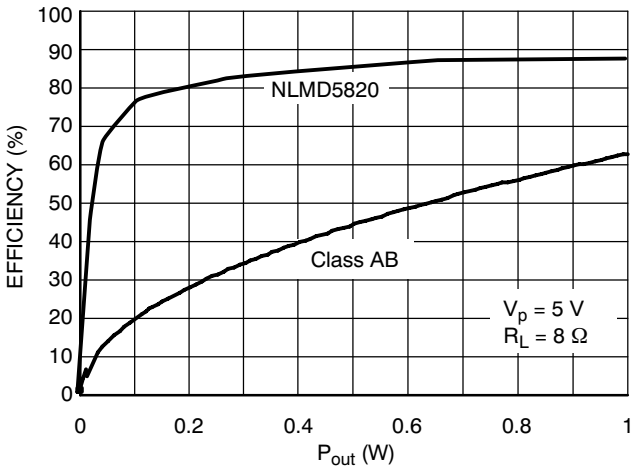


Figure 3. Efficiency vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz

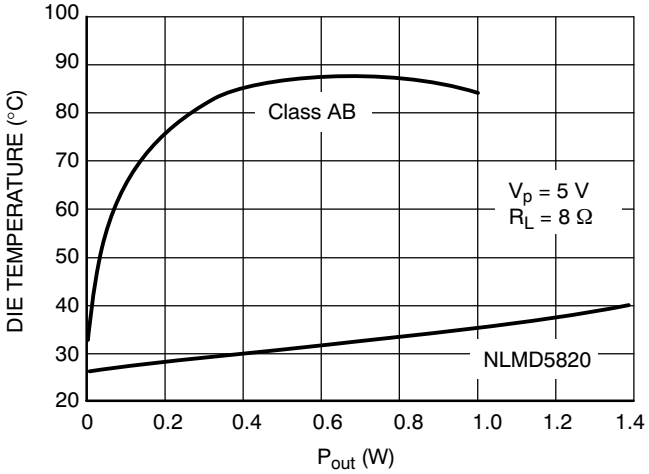


Figure 4. Die Temperature vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz @ T_A = +25°C

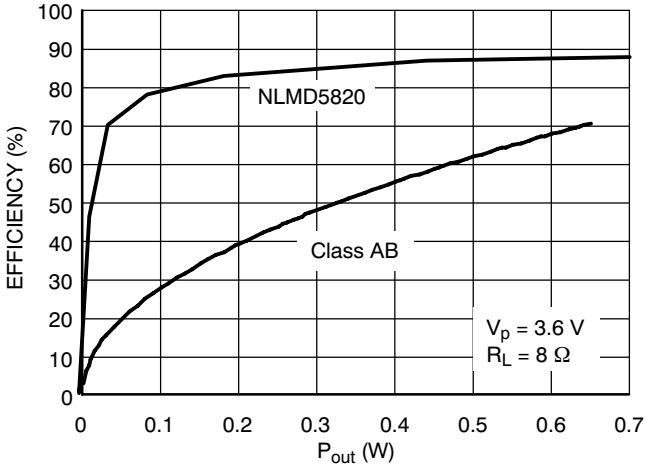


Figure 5. Efficiency vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz

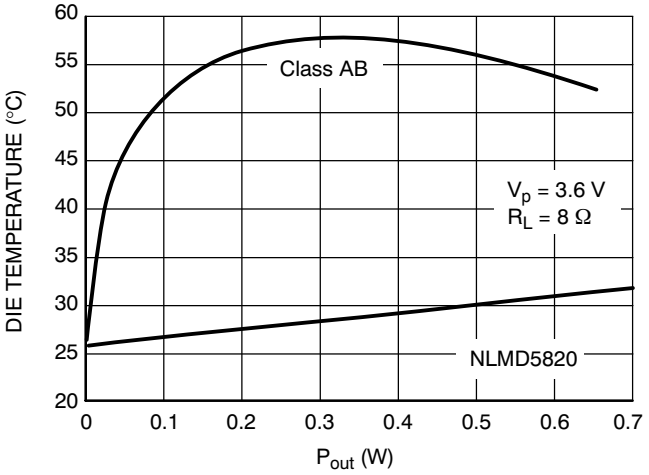


Figure 6. Die Temperature vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz @ T_A = +25°C

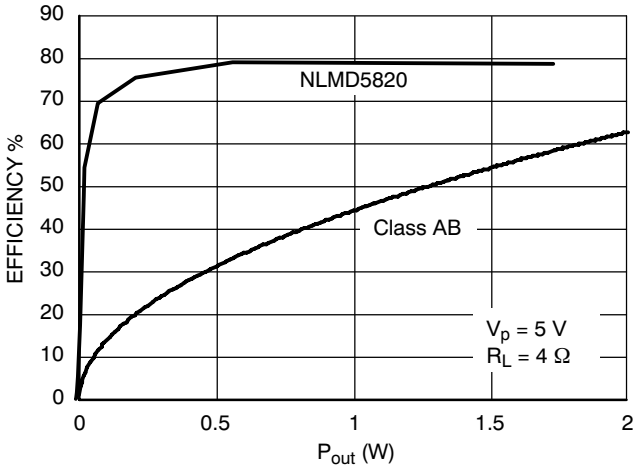


Figure 7. Efficiency vs. P_{out}
V_p = 5 V, R_L = 4 Ω, f = 1 kHz

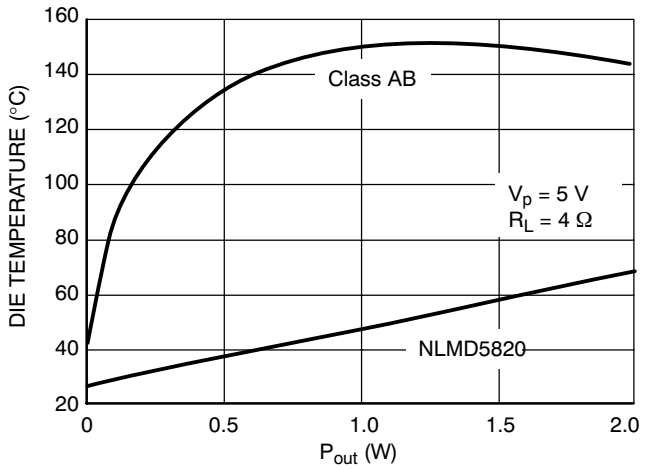


Figure 8. Die Temperature vs. P_{out}
V_p = 5 V, R_L = 4 Ω, f = 1 kHz @ T_A = +25°C

TYPICAL CHARACTERISTICS OF AMPLIFIER

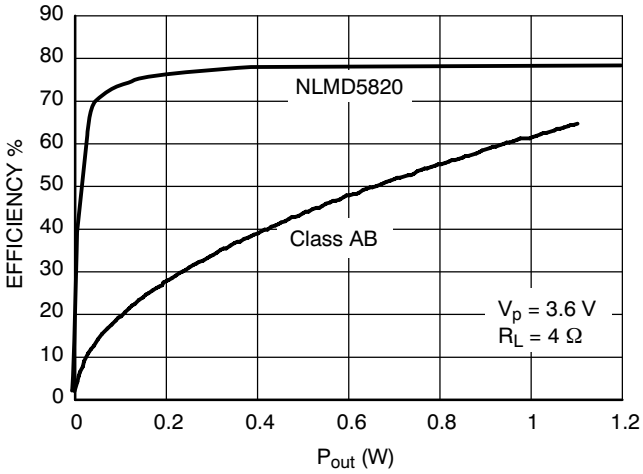


Figure 9. Efficiency vs. P_{out}
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz

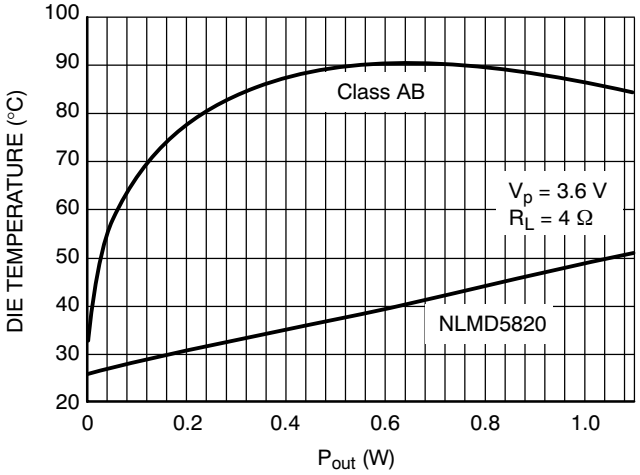


Figure 10. Die Temperature vs. P_{out}
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz @ T_A = +25°C

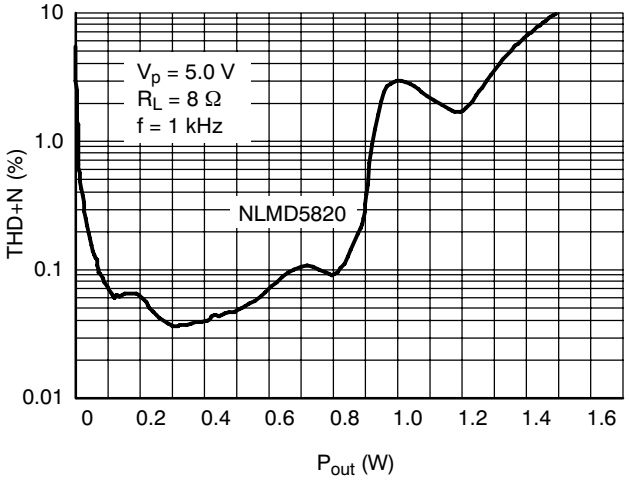


Figure 11. THD+N vs. P_{out}
V_p = 5 V, R_L = 8 Ω, f = 1 kHz

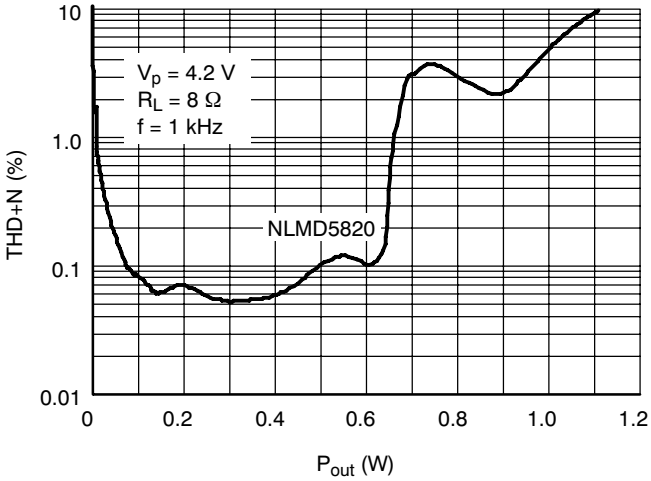


Figure 12. THD+N vs. P_{out}
V_p = 4.2 V, R_L = 8 Ω, f = 1 kHz

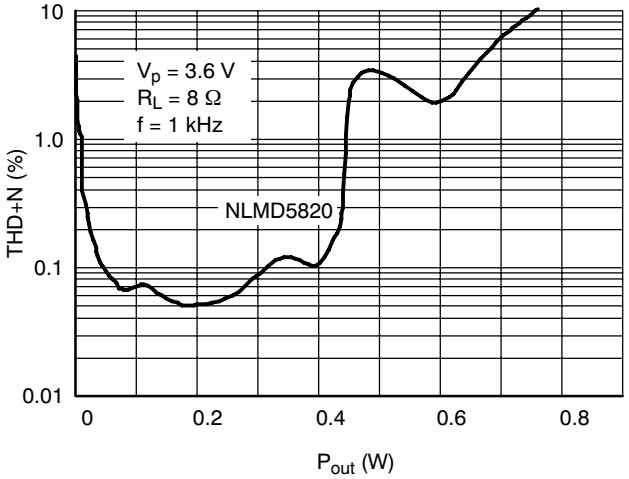


Figure 13. THD+N vs. P_{out}
V_p = 3.6 V, R_L = 8 Ω, f = 1 kHz

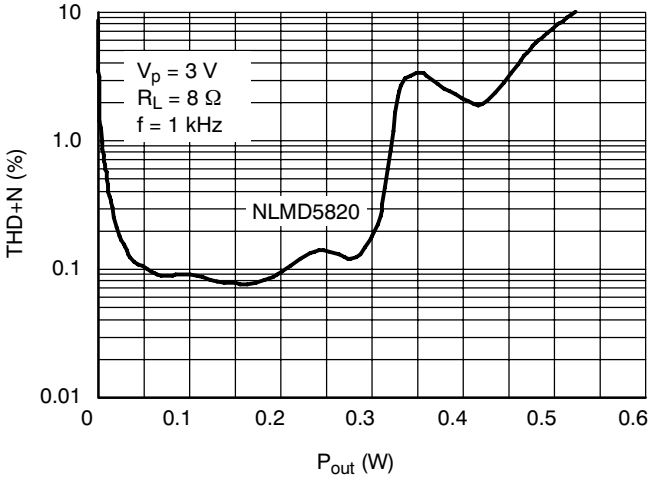


Figure 14. THD+N vs. P_{out}
V_p = 3 V, R_L = 8 Ω, f = 1 kHz

TYPICAL CHARACTERISTICS OF AMPLIFIER

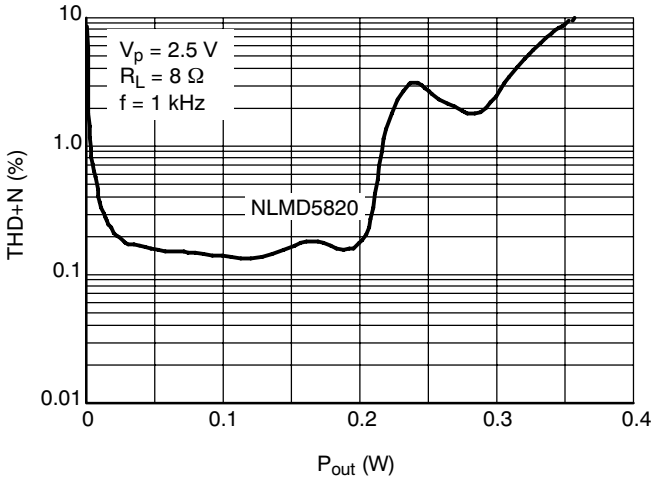


Figure 15. THD+N vs. Pout
V_p = 2.5 V, R_L = 8 Ω, f = 1 kHz

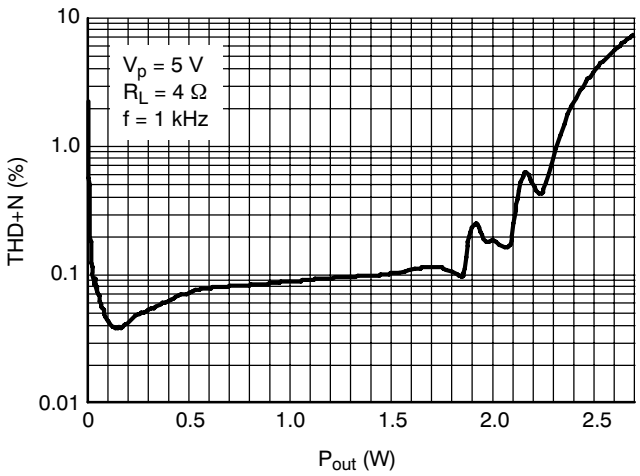


Figure 16. THD+N vs. Pout
V_p = 5 V, R_L = 4 Ω, f = 1 kHz

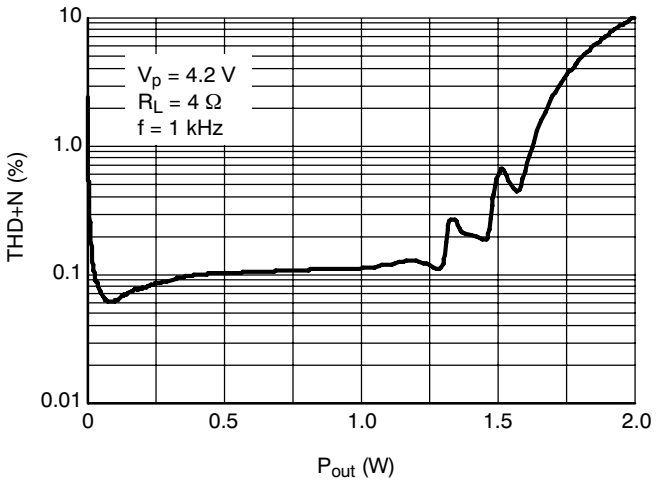


Figure 17. THD+N vs. Pout
V_p = 4.2 V, R_L = 4 Ω, f = 1 kHz

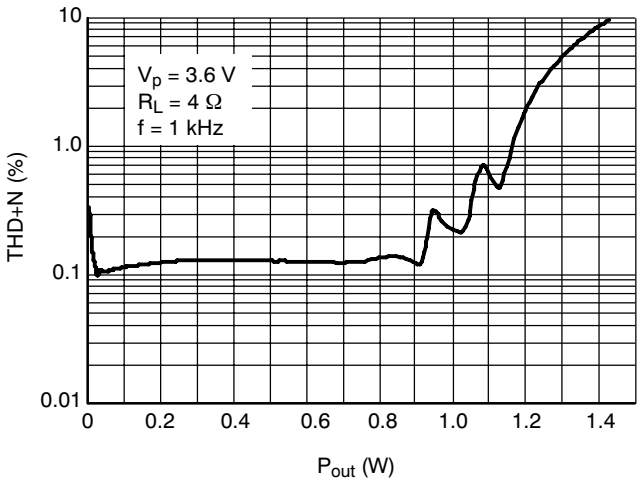


Figure 18. THD+N vs. Pout
V_p = 3.6 V, R_L = 4 Ω, f = 1 kHz

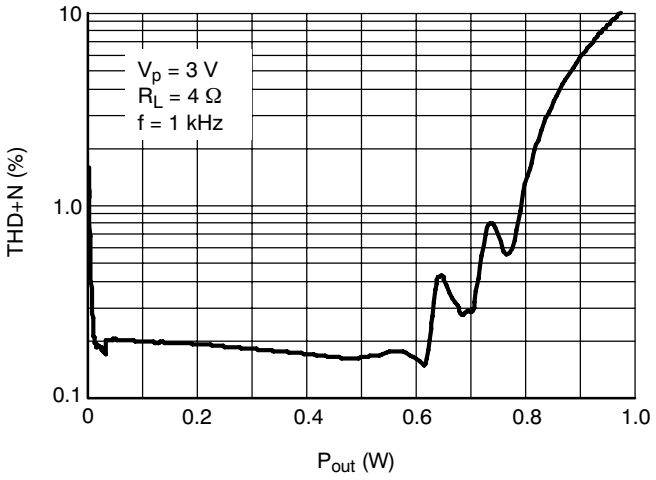


Figure 19. THD+N vs. Power Out
V_p = 3 V, R_L = 4 Ω, f = 1 kHz

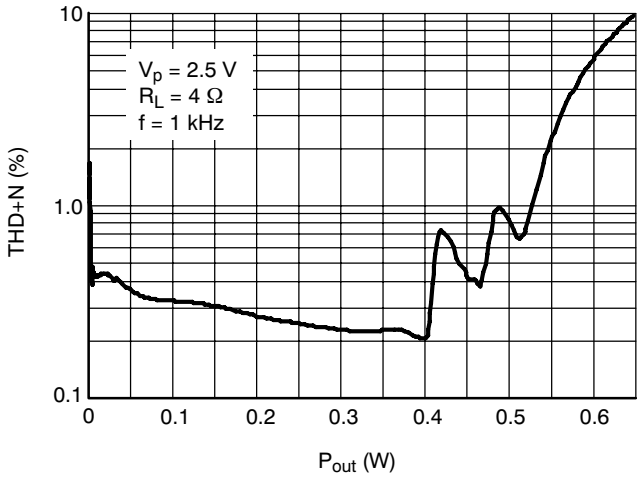


Figure 20. THD+N vs. Power Out
V_p = 2.5 V, R_L = 4 Ω, f = 1 kHz

TYPICAL CHARACTERISTICS OF AMPLIFIER

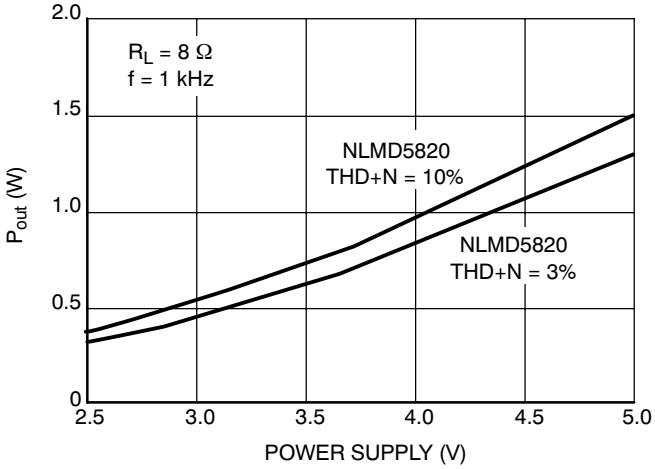


Figure 21. Output Power vs. Power Supply
R_L = 8 Ω @ f = 1 kHz

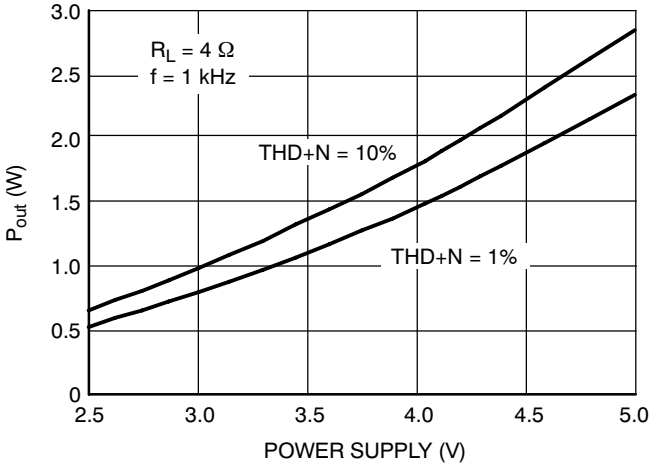


Figure 22. Output Power vs. Power Supply
R_L = 4 Ω @ f = 1 kHz

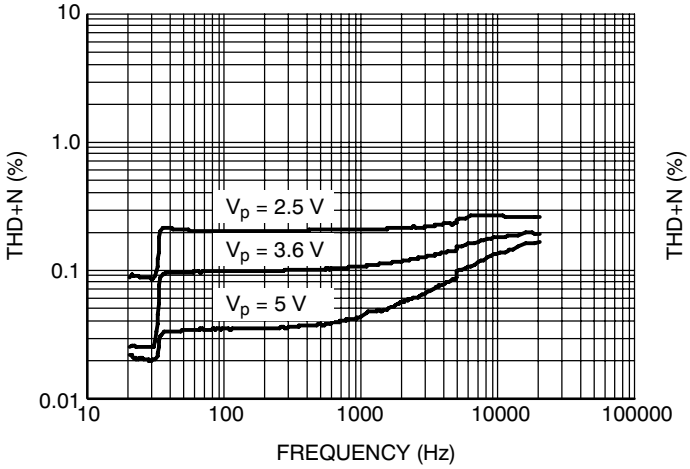


Figure 23. THD+N vs. Frequency
R_L = 8 Ω, P_{out} = 250 mW @ f = 1 kHz

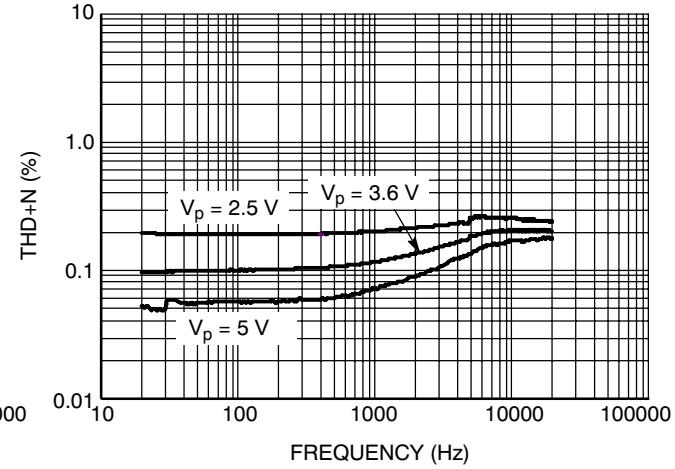


Figure 24. THD+N vs. Frequency
R_L = 4 Ω, P_{out} = 250 mW @ f = 1 kHz

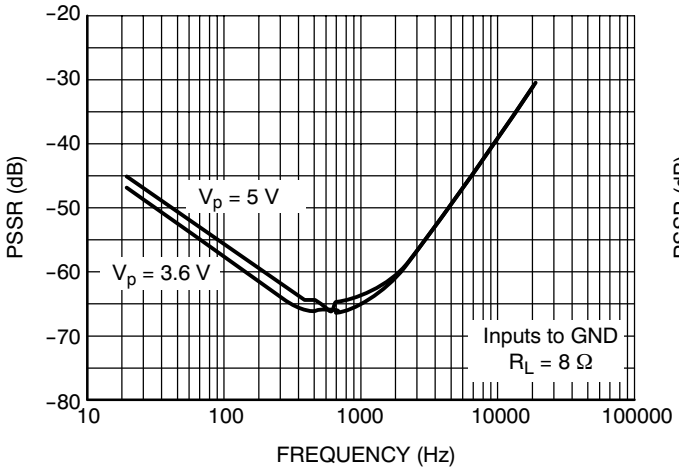


Figure 25. PSRR vs. Frequency
Inputs Grounded, R_L = 8 Ω, Vripple = 200 mvpkpk

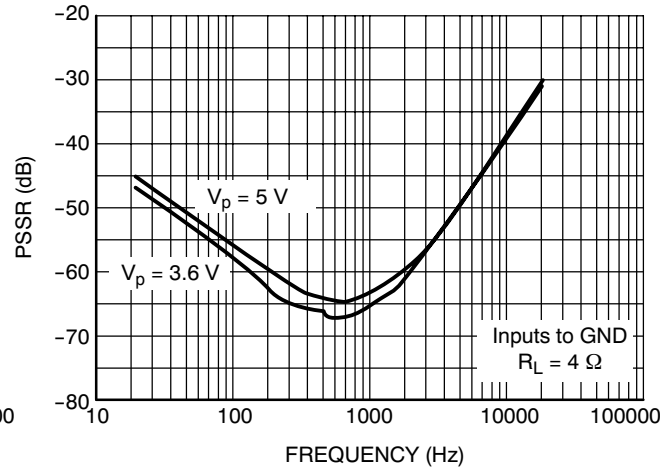


Figure 26. PSRR vs. Frequency
Inputs grounded, R_L = 4 Ω, Vripple = 200 mVpkpk

TYPICAL CHARACTERISTICS OF AMPLIFIER

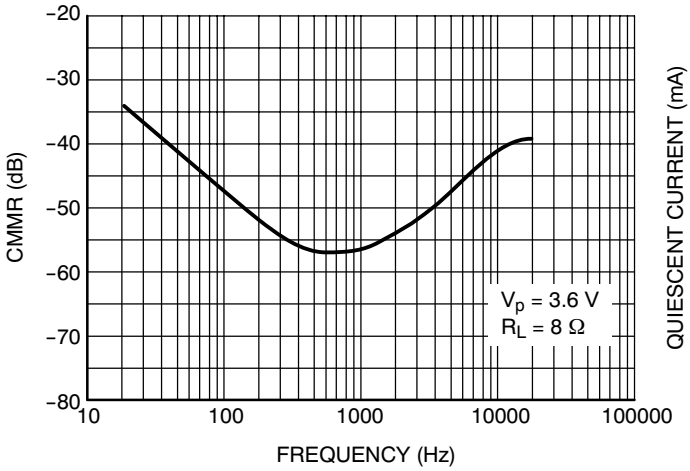


Figure 27. PSRR vs. Frequency
V_p = 3.6 V, R_L = 8 Ω, Vic = 200 mvpkpk

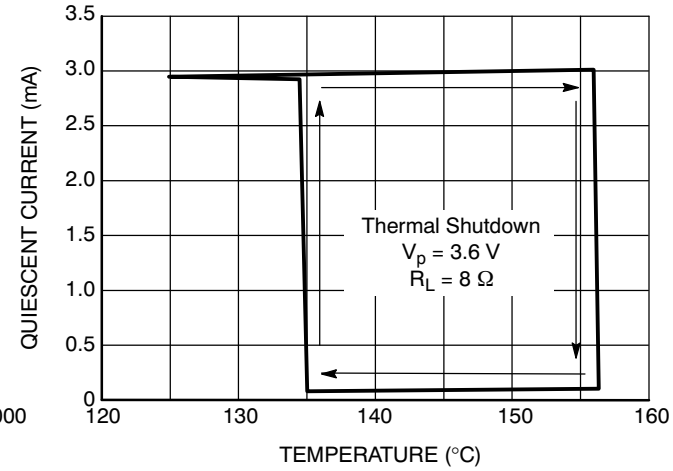


Figure 28. Thermal Shutdown vs. Temperature
V_p = 5 V, R_L = 8 Ω,

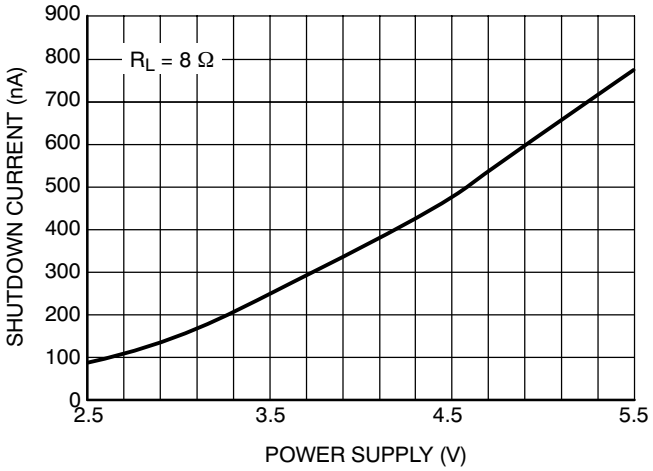


Figure 29. Shutdown Current vs. Power Supply
R_L = 8 Ω

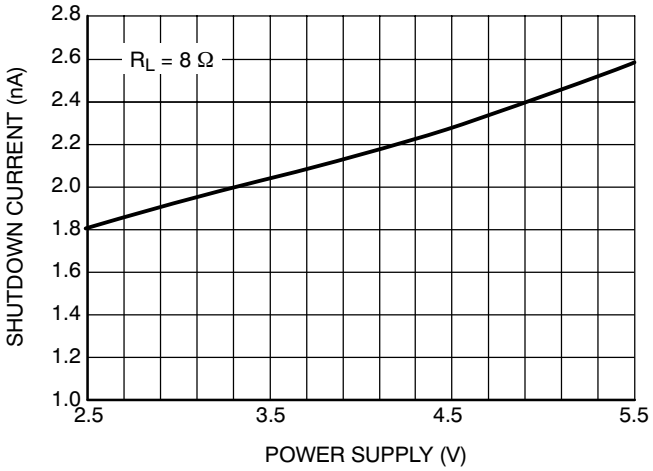


Figure 30. Quiescent Current vs. Power Supply
R_L = 8 Ω

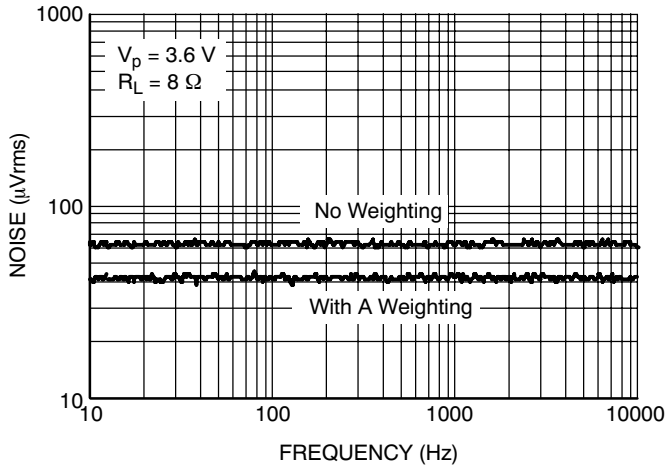


Figure 31. Noise Floor, Inputs AC Grounded
with 1 μF V_p = 3.6 V

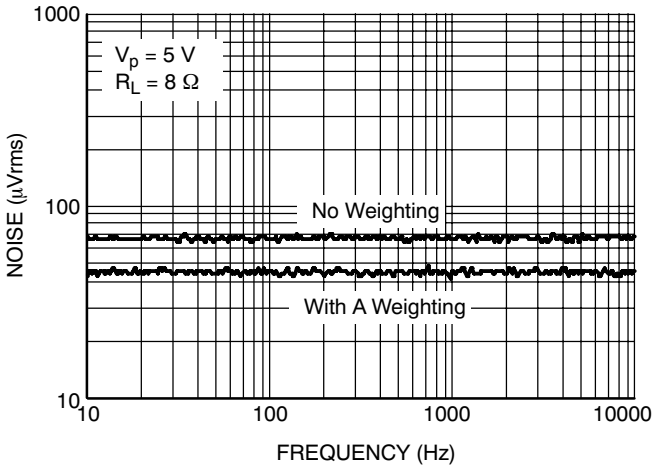


Figure 32. Noise Floor, Inputs AC Grounded
with 1 μF V_p = 5 V

TYPICAL CHARACTERISTICS OF AMPLIFIER

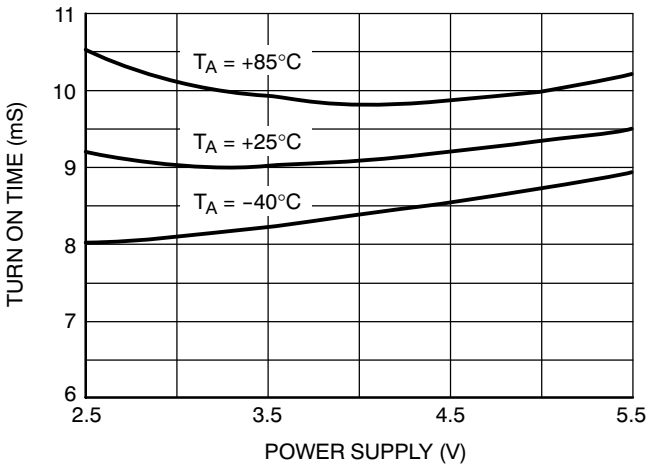


Figure 33. Turn on Time

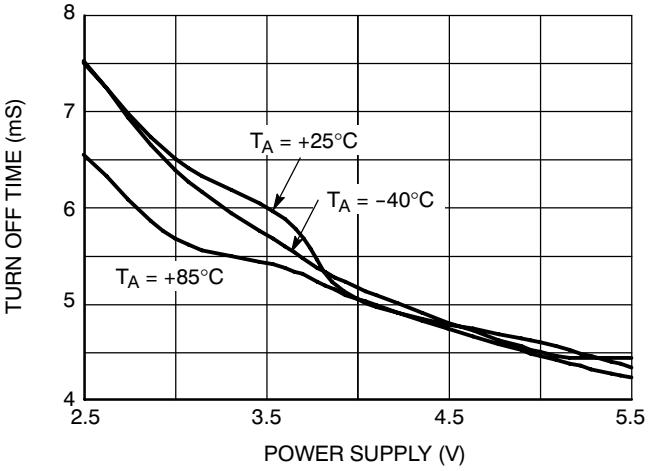


Figure 34. Turn off Time

TYPICAL CHARACTERISTICS OF SWITCHES

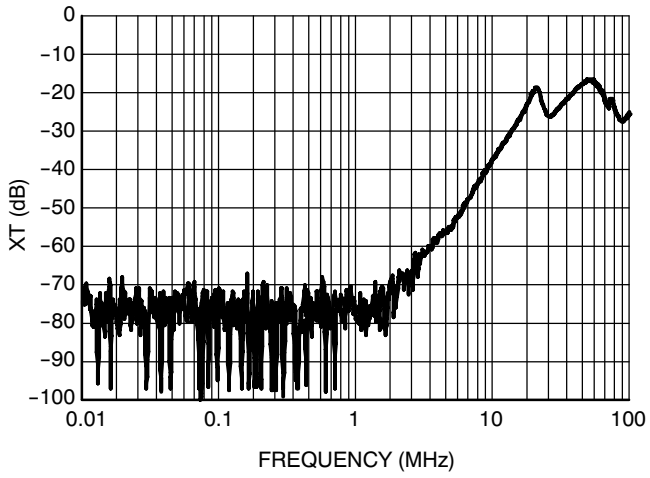


Figure 35. Cross Talk vs. Frequency @ V_{CC} = 4.2 V

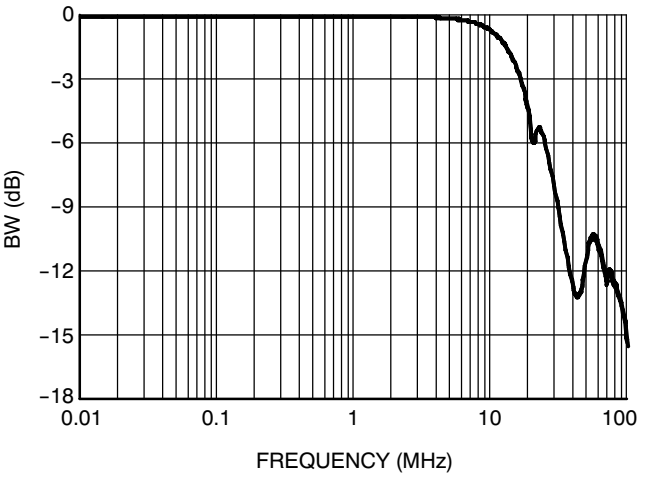


Figure 36. Bandwidth vs. Frequency

TYPICAL CHARACTERISTICS OF SWITCHES

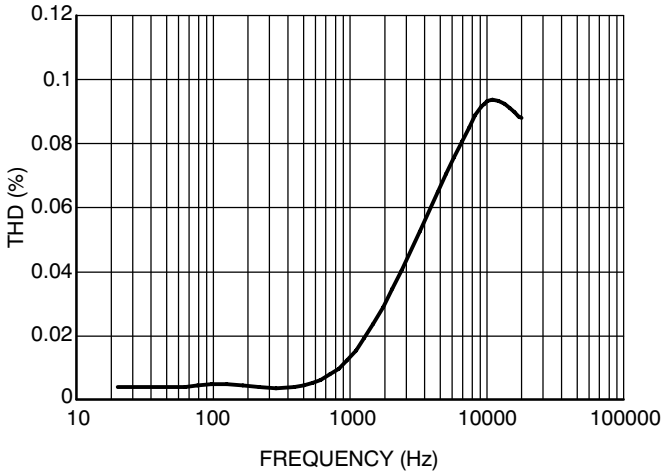


Figure 37. Total Harmonic Distortion

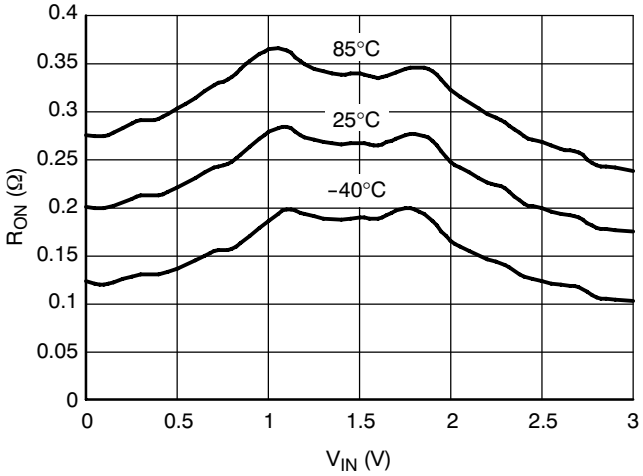


Figure 38. On−Resistance vs. Input Voltage @ V_{CC} = 3.0 V

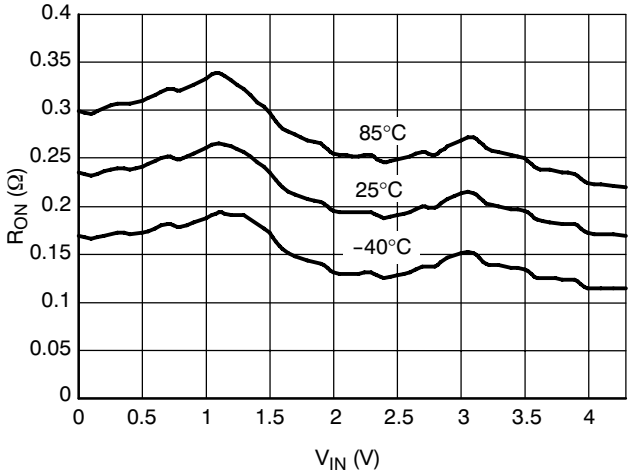


Figure 39. On−Resistance vs. Input Voltage @ V_{CC} = 4.2 V

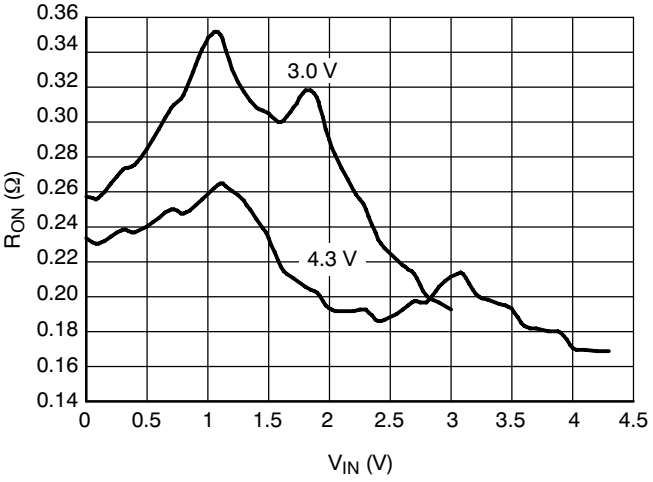


Figure 40. On−Resistance vs. Input Voltage

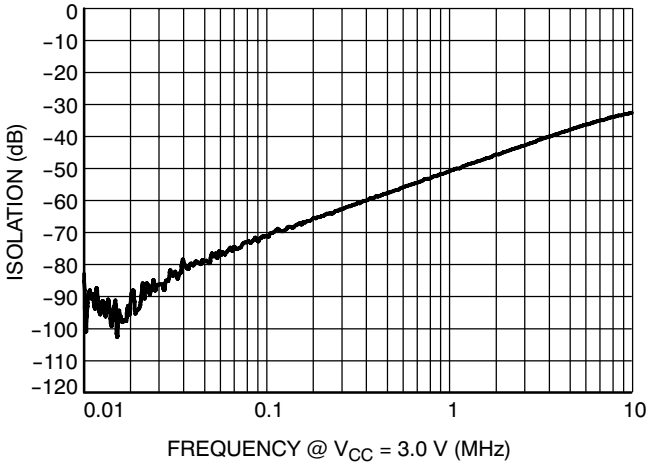


Figure 41. Isolation vs. Frequency

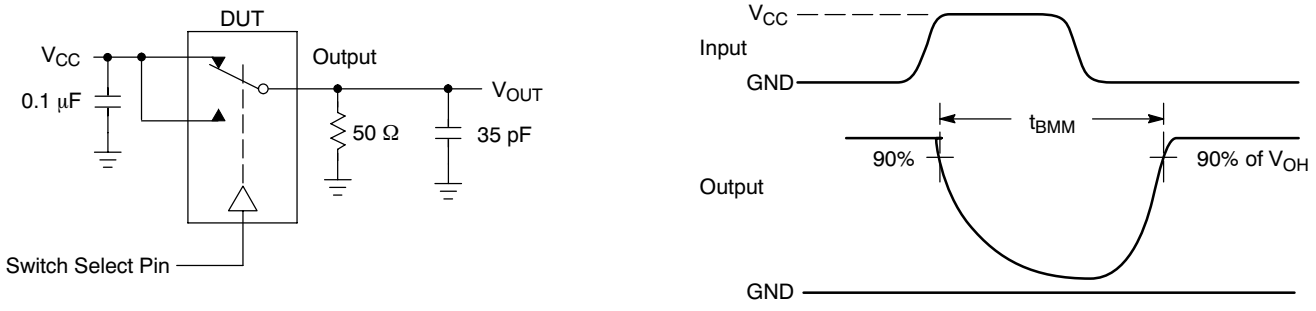


Figure 42. t_{BBM} (Time Break−Before−Make)

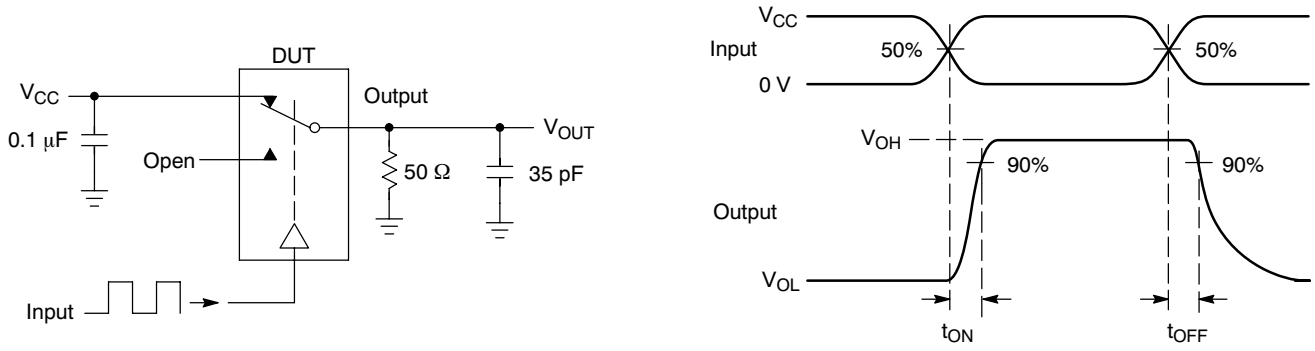


Figure 43. t_{ON}/t_{OFF}

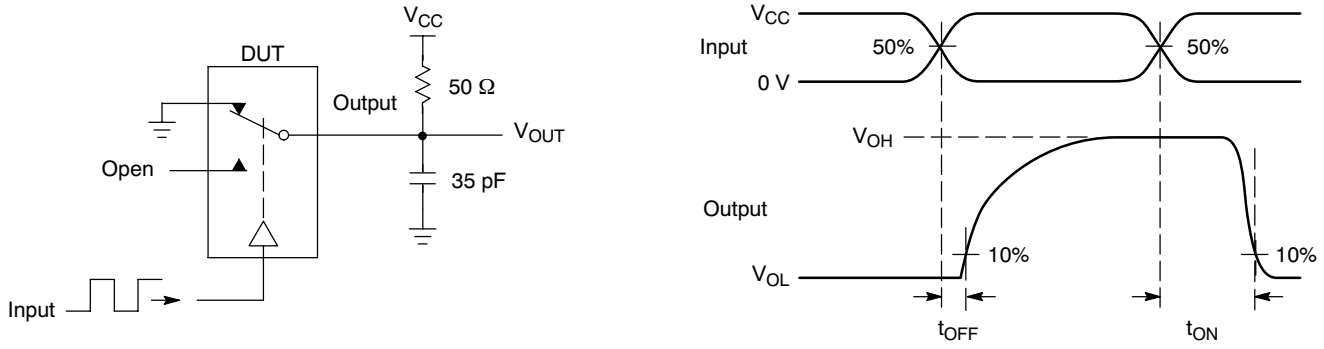
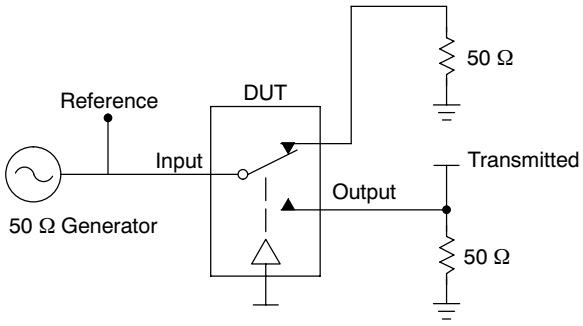


Figure 44. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.

V_{ISO} = Off Channel Isolation = 20 Log$\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz

V_{ONL} = On Channel Loss = 20 Log$\left(\frac{V_{OUT}}{V_{IN}}\right)$ for V_{IN} at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 45. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

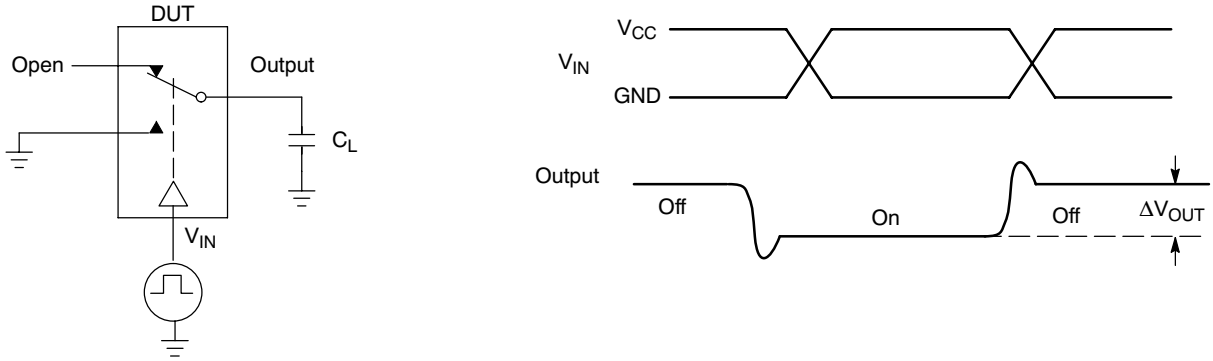


Figure 46. Charge Injection: (Q)

DESCRIPTION INFORMATION

Detailed Description

The basic structure of the amplifier portion of the NLMD5820 is composed of one analog pre−amplifier, a pulse width modulator and an H−bridge CMOS power stage. The first stage is externally configurable with gain−setting resistor R_i and the internal fixed feedback resistor R_f (the closed−loop gain is fixed by the ratios of these resistors) and the other stage is fixed. The load is driven differentially through two output stages.

The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, the typical values of which are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors is typically 0.4 Ω.

Turn On and Turn Off Transitions in Case of 9 Pin Flip−Chip Package

In order to eliminate “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When a logic high is applied to the shutdown pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly (5.0 ms). This method to turn on the device is optimized in terms of rejection of “pop and click” noises. Thus, the total turn on time to get full power to the load is 9 ms (typical).

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. No power is delivered to the load 5 ms after a falling edge on the shutdown pin. Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

Turn On and Turn Off Transitions in Case of UDFN8

In case of UDFN8 package, the audio signal is established instantaneously after the rising edge on the shutdown pin. The audio is also suddenly cut once a low level is sent to the amplifier. This way to turn on and off the device in a very fast way also prevents from “pop & click” noise.

Shutdown Function

The device enters shutdown mode when the shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 1.5 μA.

Current Breaker Circuit

The maximum output power of the circuit corresponds to an average current in the load of 820 mA.

In order to limit the excessive power dissipation in the load if a short−circuit occurs, a current breaker cell shuts down the output stage. The current in the four output MOS transistors are real−time controlled, and if one current exceeds the threshold set to 1.5 A, the MOS transistor is opened and the current is reduced to zero. As soon as the short−circuit is removed, the circuit is able to deliver the expected output power.

This patented structure protects the NLMD5820. Since it completely turns off the load, it minimizes the risk of the chip overheating which could occur if a soft current limiting circuit was used.

Dual SPST Switch

The NLMD5820 features an integrated dual SPST analog switch. The control for the switch is operated independently of the amplifier, allowing the audio system a choice between routing signals through the amplifier or letting them pass unaffected through the switch. When the switch is open, it maintains significant off isolation to minimize the effects of the amplifier output on the system.

APPLICATION INFORMATION

NLMD5820 PWM Modulation Scheme

The NLMD5820 uses a PWM modulation scheme with each output switching from 0 to the supply voltage. If V_{in} = 0 V outputs OUTM and OUTP are in phase and no current is flowing through the differential load. When a positive signal is applied, OUTP duty cycle is greater than 50% and OUTM is less than 50%. With this configuration, the current through the load is 0 A most of the switching period and thus power losses in the load are lowered.

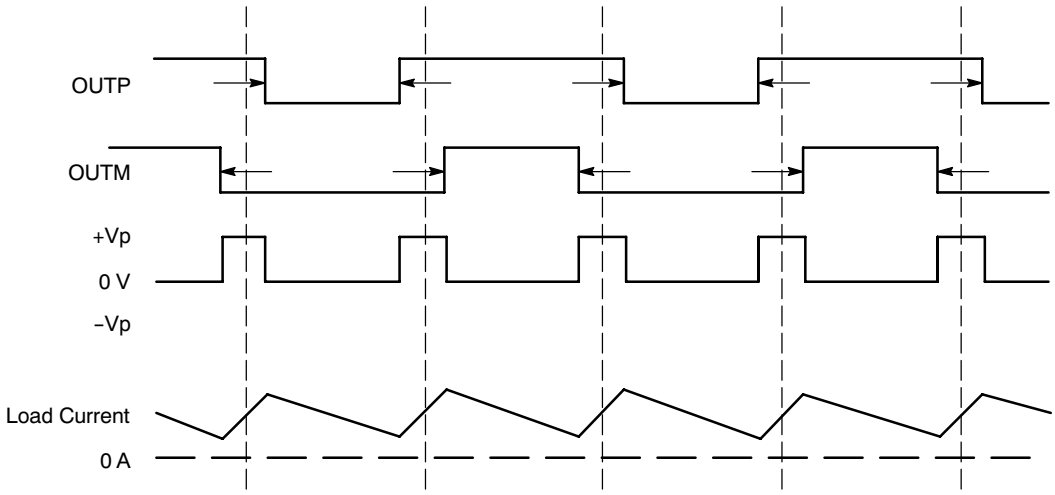


Figure 47. Output Voltage and Current Waveforms into an Inductive Loudspeaker DC Output Positive Voltage Configuration

Voltage Gain

The first stage is an analog amplifier. The second stage is a comparator: the output of the first stage is compared with a periodic ramp signal. The output comparator gives a pulse width modulation signal (PWM). The third and last stage is the direct conversion of the PWM signal with MOS transistors H−bridge into a powerful output signal with low impedance capability.

With an 8 Ω load, the total gain of the device is typically set to:

$$\frac{300\ k\Omega}{R_i}$$

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with R_{in}, the cut−off frequency is given by $Fc = \frac{1}{2 \times \pi \times R_i \times C_i}$.

When using an input resistor set to 150 kΩ, the gain configuration is 2 V/V. In such a case, the input capacitor selection can be from 10 nF to 1 μF with cutoff frequency values between 1 Hz and 100 Hz. The NLMD5820 also includes a built in low pass filtering function. It's cut off frequency is set to 20 kHz.

Optional Output Filter

This filter is optional due to the capability of the speaker to filter by itself the high frequency signal. Nevertheless, the high frequency is not audible and filtered by the human ear.

An optional filter can be used for filtering high frequency signal before the speaker. In this case, the circuit consists of two inductors (15 μH) and two capacitors (2.2 μF). The size of the inductors is linked to the output power requested by the application. A simplified version of this filter requires a 1 μF capacitor in parallel with the load, instead of two 2.2 μF connected to ground).

Cellular phones and portable electronic devices are great applications for Filterless Class−D as the track length between the amplifier and the speaker is short, thus, there is usually no need for an EMI filter. However, to lower radiated emissions as much as possible when used in filterless mode, a ferrite filter can often be used. Select a ferrite bead with the high impedance around 100 MHz and a very low DCR value in the audio frequency range is the best choice. The MPZ1608S221A1 from TDK is a good choice. The package size is 0603.

Optimum Equivalent Capacitance at Output Stage

If the optional filter described in the above section isn't selected. Cellular phones and wireless portable devices design normally put several Radio Frequency filtering capacitors and ESD protection devices between Filter less Class D outputs and loudspeaker. Those devices are usually connected between amplifier output and ground. In order to achieve the best sound quality, the optimum value of total equivalent capacitance between each output terminal to the ground should be less than or equal to 150 pF. This total equivalent capacitance consists of the radio frequency filtering capacitors and ESD protection device equivalent parasitic capacitance.

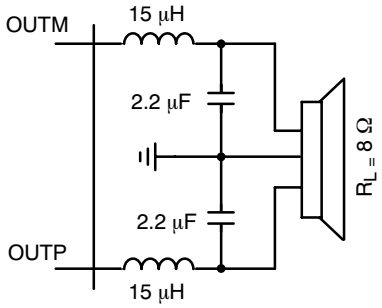


Figure 48. Advanced Optional Audio Output Filter

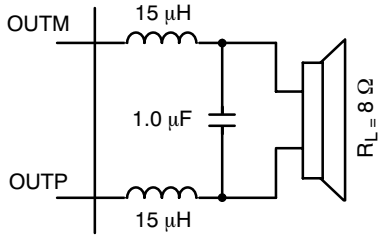


Figure 49. Optional Audio Output Filter

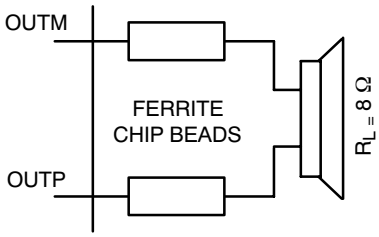


Figure 50. Optional EMI Ferrite Bead Filter

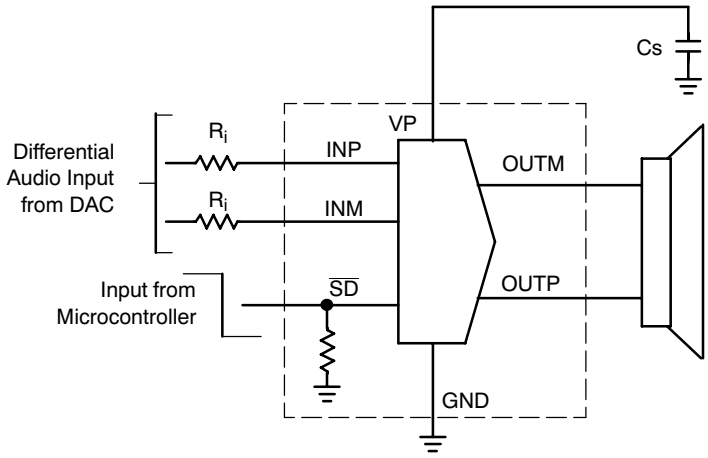


Figure 51. NLMD5820 Application Schematic with Fully Differential Input Configuration

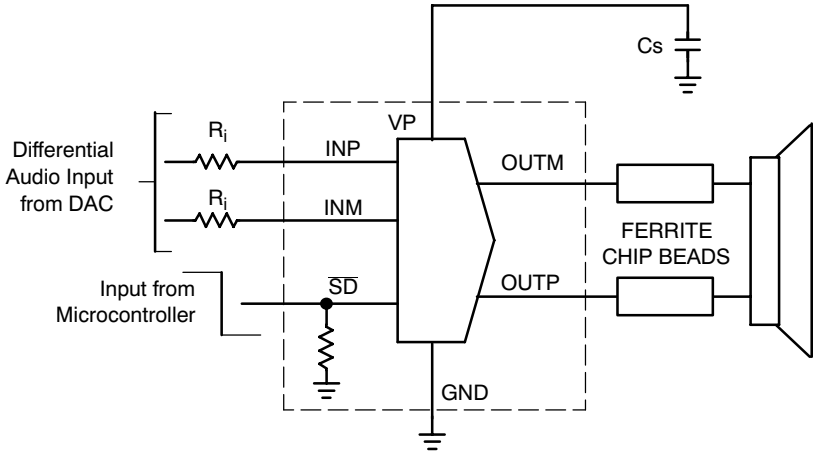


Figure 52. NLMD5820 Application Schematic with Fully Differential Input Configuration and Ferrite Chip Beads as an Output EMI Filter

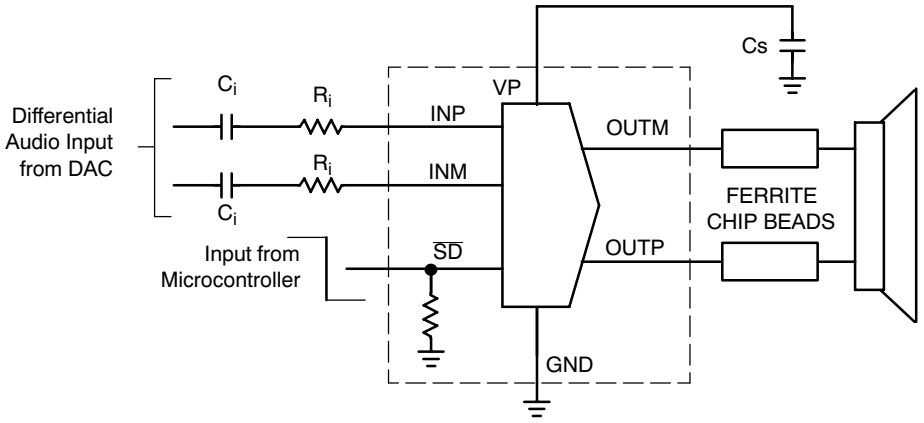


Figure 53. NLMD5820 Application Schematic with Differential Input Configuration and High Pass Filtering Function

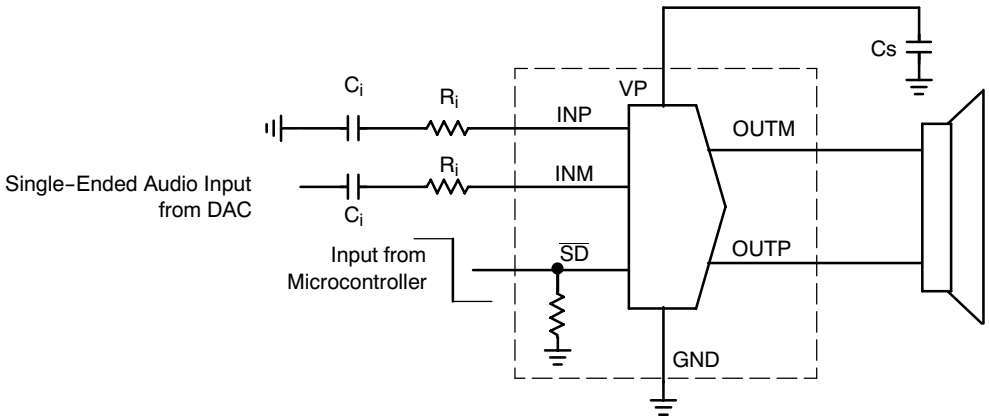


Figure 54. NLMD5820 Application Schematic with Single Ended Input Configuration

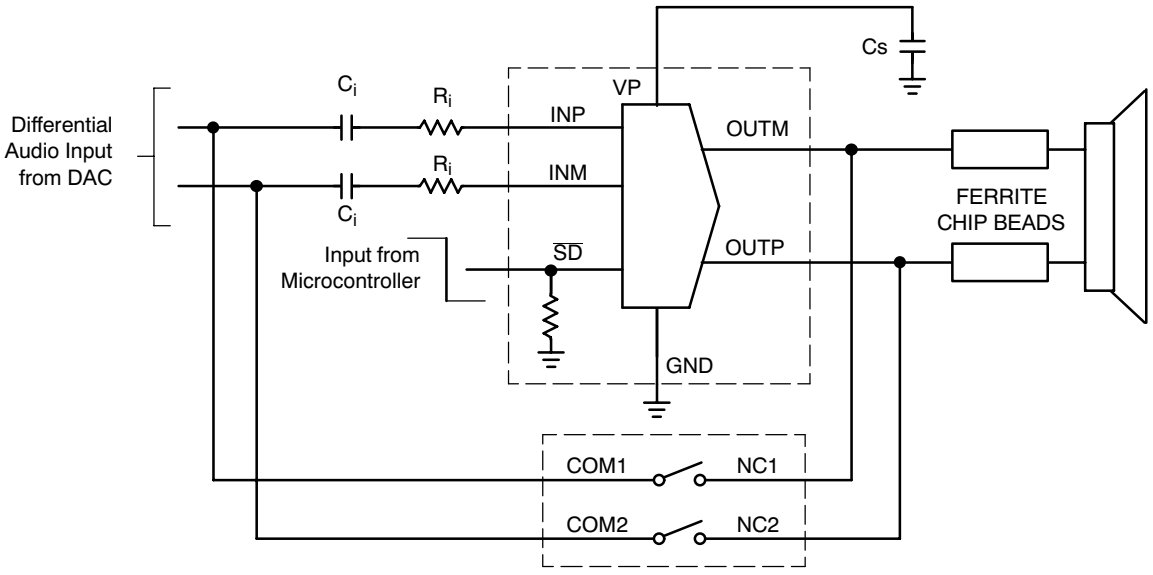


Figure 55. NLMD5820 Application Schematic Using Switches as Optional Bypass

UDFN16 3.2x2.4, 0.4P
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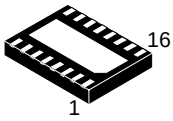
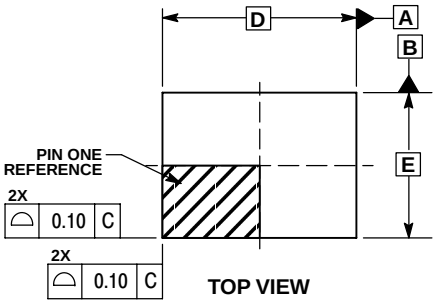
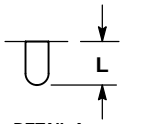
DATE 04 APR 2007



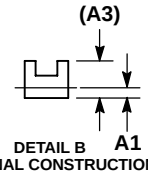
SCALE 4:1



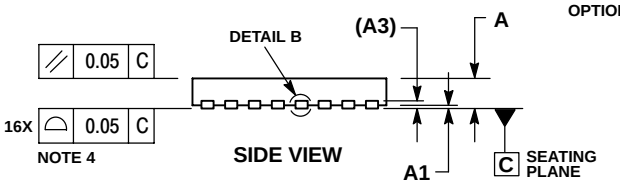
TOP VIEW



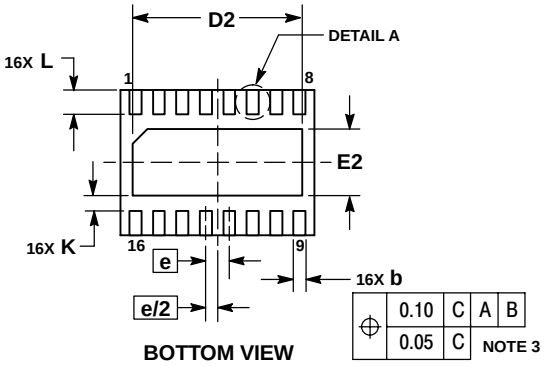
DETAIL A
OPTIONAL CONSTRUCTION
2X SCALE



DETAIL B
OPTIONAL CONSTRUCTION
4X SCALE



SIDE VIEW

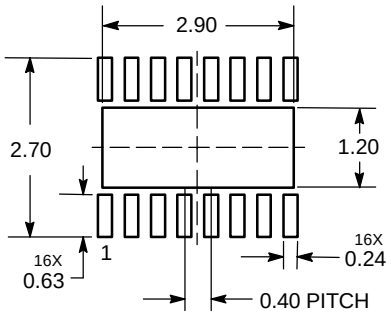


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.20 BSC	
D2	2.70	2.90
E	2.40 BSC	
E2	1.00	1.20
e	0.40 BSC	
K	0.20	−−−
L	0.30	0.50

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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