# NUS3116MT

# Main Switch Power MOSFET and Dual Charging BJT

## −12 V, −6.2 A, Single P−Channel with Dual PNP low $V_{ce(sat)}$ Transistors, 3x3 mm WDFN Package

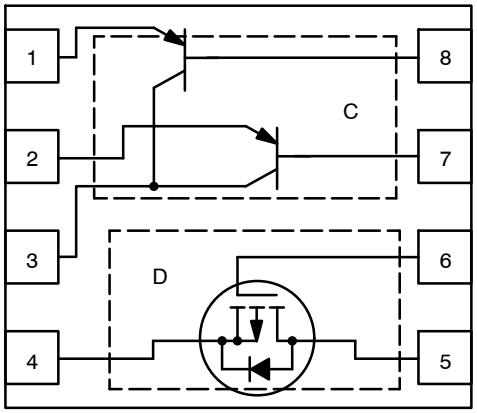
This device integrates one high performance power MOSFET and two low $V_{ce(sat)}$ transistors, greatly reducing the layout space and optimizing charging performance in the battery−powered portable electronics.

### Features

- High Performance Power MOSFET
- Dual−Low $V_{ce(sat)}$ Transistors as Charging Power Mux
- 3.0x3.0x0.8 mm WDFN Package
- Independent Pin−out Provides Circuit Flexibility
- Low Profile (<0.8 mm) for Easy Fit in Thin Environments
- This is a Pb−Free Device

### Applications

- Main Switch and Battery Charging Mux for Portable Electronics
- Optimized for Commercial PMUs from Top Suppliers (See Figure 2)




DFN8 3x3 Pin Connections
(Top View)

**Figure 1. Simple Schematic**

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**MOSFET**

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| −12 V | 32 mΩ @ −4.5 V | −6.2 A |
| | 44 mΩ @ −2.5 V | |

**Low $V_{ce(sat)}$ PNP (Wall)**

| $V_{CEO}$ MAX | $V_{EBO}$ MAX | $I_C$ MAX |
|---|---|---|
| −30 V | −8.0 V | −2.0 A |

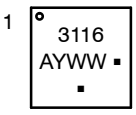
**Low $V_{ce(sat)}$ PNP (USB)**

| $V_{CEO}$ MAX | $V_{EBO}$ MAX | $I_C$ MAX |
|---|---|---|
| −30 V | −8.0 V | −2.0 A |

**MARKING DIAGRAM**




**DFN8**
**CASE 506BC**




| | |
|---|---|
| 3116 | = Device Code |
| A | = Assembly Location |
| Y | = Year |
| WW | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NUS3116MTR2G | WDFN8 (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Publication Order Number:
NUS3116MT/D

**P−Channel Power MOSFET Maximum Ratings** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Units |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −12 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±8.0 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | −5.47 | A |
| | | $T_A$ = 85°C | | −4.0 | |
| | t ≤ 5 s | $T_A$ = 25°C | | −6.2 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 1.7 | W |
| | t ≤ 5 s | | | 2.2 | |
| Continuous Drain Current (Note 2, Minimum Pad) | Steady State | $T_A$ = 25°C | $I_D$ | −4.4 | A |
| | | $T_A$ = 85°C | | −3.2 | |
| Power Dissipation (Note 2) | | $T_A$ = 25°C | $P_D$ | 1.14 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | −25 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode)[2] | | | $I_S$ | −2.8 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

**THERMAL RESISTANCE RATINGS**

| Parameter | Symbol | Max | Units |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 110 | °C/W |
| Junction−to−Ambient − t < 10 s (Note 2) | $R_{\theta JA}$ | 56 | °C/W |
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 72 | °C/W |
| Junction−to−Ambient − t < 10 s (Note 1) | $R_{\theta JA}$ | 40 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface−mounted on FR4 board using the minimum recommended pad size of 0.5 in sq, 1 oz. Cu.

**P−Channel MOSFET Electrical Characteristics** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −12.0 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D$ = −250 μA, ref to 25°C | | | −10.1 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −12 V | $T_J$ = 25°C | | | −1.0 | μA |
| | | | $T_J$ = 125°C | | | −10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±8 V | | | | ±200 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −0.45 | −0.67 | −1.1 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 2.68 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −4.5 V, $I_D$ = −3.0 A | | | 32 | 40 | mΩ |
| | | $V_{GS}$ = −2.5 V, $I_D$ = −3.0 A | | | 44 | 50 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −16 V, $I_D$ = −3.0 A | | | 5.9 | | S |

3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

**P−Channel MOSFET Electrical Characteristics** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = −12 V | | 1329 | | pF |
| Output Capacitance | $C_{OSS}$ | | | 200 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | 116 | | |
| Total Gate Charge | $Q_{G(tot)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −12 V, $I_D$ = −3.0 A | | 13 | | nC |
| Threshold Gate Charge | $Q_{G(th)}$ | | | 1.5 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | 2.2 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | 2.9 | | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = −4.5 V, $V_{DD}$ = −12 V, $I_D$ = −3.0 A, $R_G$ = 3.0 | | 8 | | ns |
| Rise Time | $t_r$ | | | 17.5 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | 80 | | |
| Fall Time | $t_f$ | | | 56.5 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| Forward Recovery Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −1.0 A, $T_J$ = 25°C | | −0.66 | −1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = −1.0 A, $T_J$ = 125°C | | −0.54 | | |
| Reverse Recovery Time | $t_{rr}$ | $V_{GS}$ = 0 V, dISD/dt = 100 A/μs, $I_S$ = −1.0 A | | 70.8 | | ns |
| Charge Time | $t_a$ | | | 14.3 | | |
| Discharge Time | $t_b$ | | | 56.4 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | 44 | | nC |

3. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

**Dual−PNP Transistors Maximum Ratings** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | −30 | V |
| Collector−Base Voltage | $V_{CBO}$ | −30 | V |
| Emitter−Base Voltage | $V_{EBO}$ | −8.0 | V |
| Collector Current, Continous | $I_C$ | −2.0 | A |
| Collector Current, Pulsed (Note 4) | $I_C$ | −6.0 | A |
| Operating Junction and Storage Temperature | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Thermal Resistance Dissipation | $P_D$ | 1.5 | W |
| Thermal Resistance (Note 5) | $R_{\theta JA}$ | 83 | °C/W |
| Thermal Resistance Dissipation | $P_D$ | 810 | mW |
| Thermal Resistance (Note 6) | $R_{\theta JA}$ | 155 | °C/W |

4. Single Pulse: Pulse Width = 1 ms
5. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
6. Surface−mounted on FR4 board using the minimum recommended pad size of 100 $mm^2$, 1 oz. Cu.

**Dual−PNP Transistors Electrical Characteristics** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Collector−Emitter Voltage | $V_{CEO}$ | $I_C$ = −10 mA, $I_B$ = 0 | −30 | | | V |
| Collector−Base Voltage | $V_{CBO}$ | $I_C$ = −0.1 mA, $I_E$ = 0 | −30 | | | V |
| Emitter−Base Voltage | $V_{EBO}$ | $I_E$ = −0.1 mA, $I_C$ = 0 | −8.0 | | | V |
| Collector−Emitter Cutoff Current | $I_{CES}$ | $V_{CES}$ = −30 V | | | −0.1 | μA |
| **ON CHARACTERISTICS** | | | | | | |
| DC Current Gain (Note 7) | $h_{FE}$ | $I_C$ = −1.0 A, $V_{CE}$ = −2.0 V | 100 | 200 | | − |
| DC Current Gain (Note 7) | $h_{FE}$ | $I_C$ = −2.0 A, $V_{CE}$ = −2.0 V | 100 | 200 | | − |
| Collector−Emitter Saturation Voltage | $V_{CE(sat)}$ | $I_C$ = −1.0 A, $I_B$ = −0.01 A | | | 0.22 | V |
| Collector−Emitter Saturation Voltage | $V_{CE(sat)}$ | $I_C$ = −1.0 A, $I_B$ = −0.1 A | | | 0.12 | V |
| Collector−Emitter Saturation Voltage | $V_{CE(sat)}$ | $I_C$ = −2.0 A, $I_B$ = −0.2 A | | | 0.24 | V |
| Input Capacitance | $C_{ibo}$ | $V_{EB}$ = −0.5 V, f = 1.0 MHz | | 240 | 400 | pF |
| Output Capacitance | $C_{obo}$ | $V_{CB}$ = −3.0 V, f = 1.0 MHz | | 50 | 100 | pF |

7. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

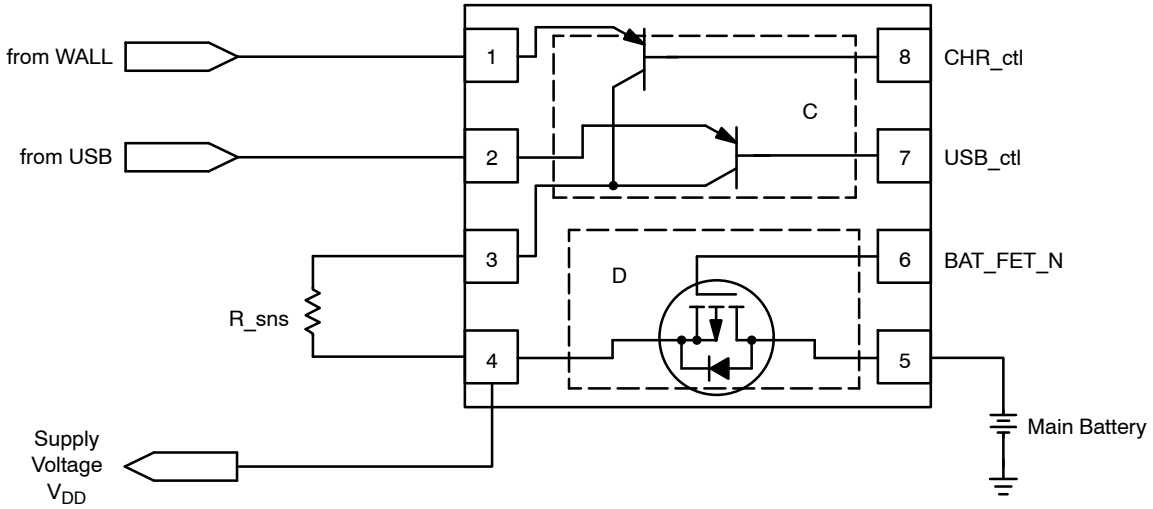



**Figure 2. Typical Application Circuit**

## TYPICAL CHARACTERISTICS – MOSFET

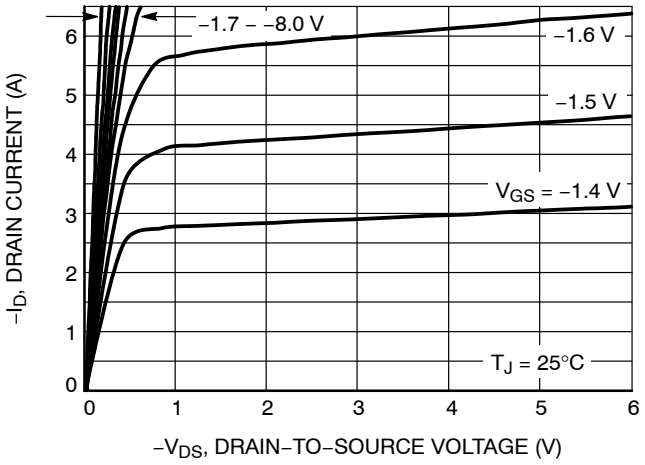



**Figure 3. On−Region Characteristics**

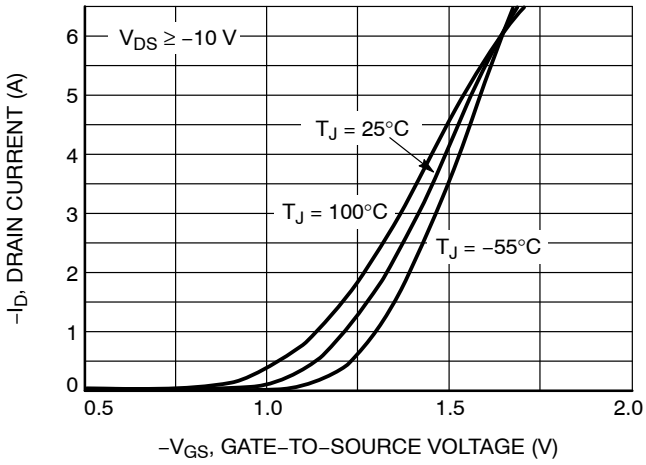



**Figure 4. Transfer Characteristics**

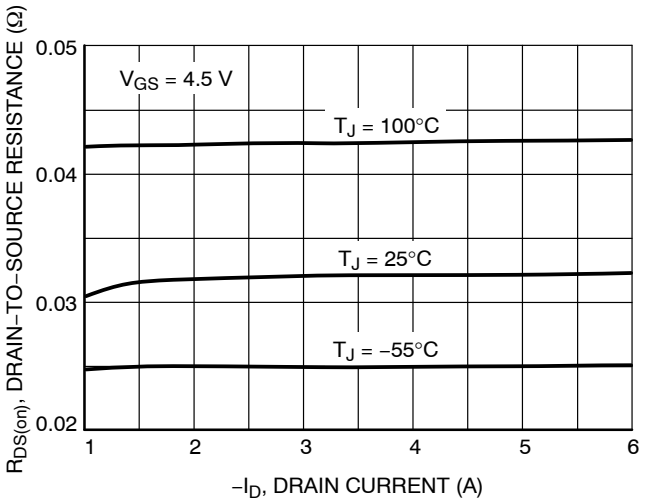



**Figure 5. On−Resistance vs. Drain Current**

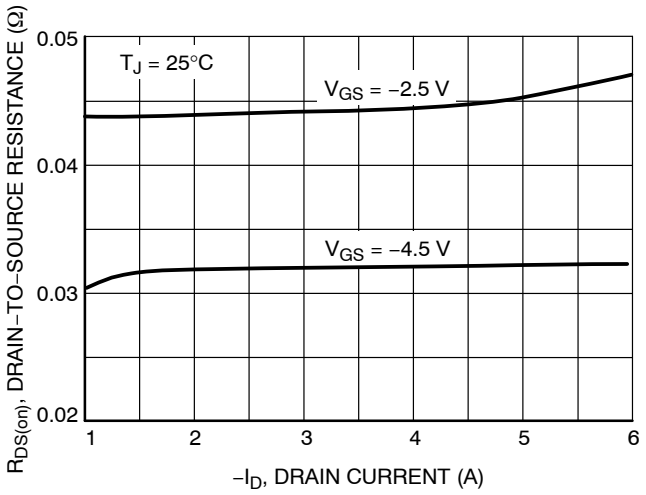



**Figure 6. On−Resistance vs. Drain Current and Gate Voltage**

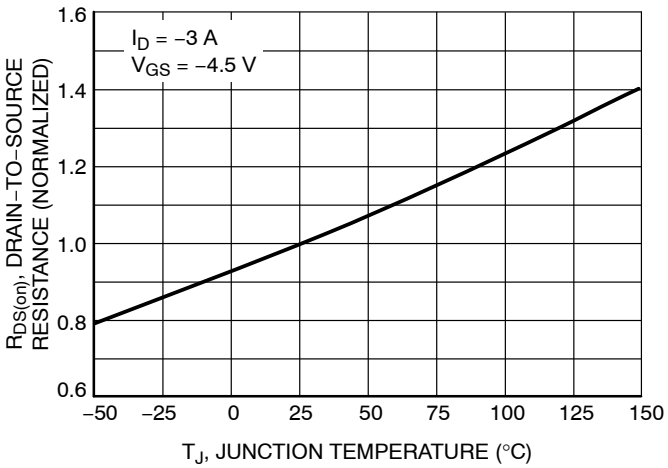



**Figure 7. On−Resistance Variation with Temperature**

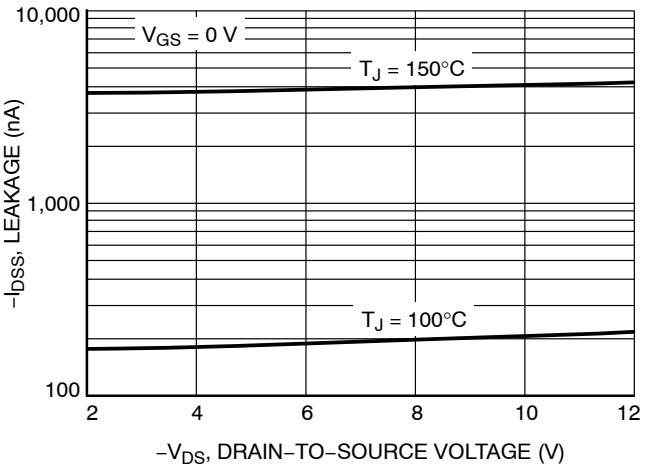



**Figure 8. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS – MOSFET

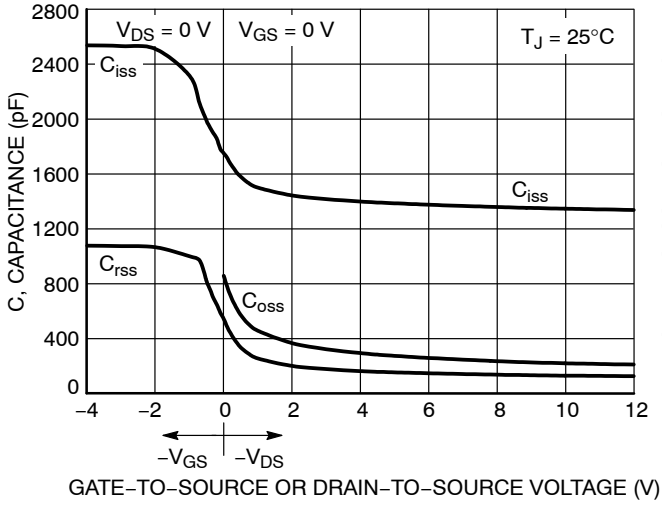



**Figure 9. Capacitance Variation**

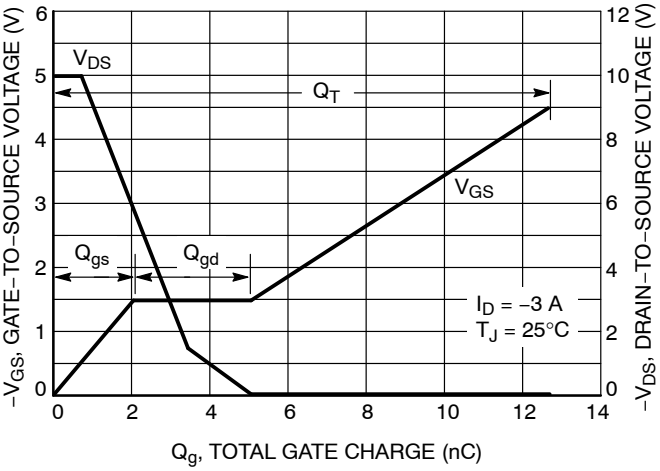



**Figure 10. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

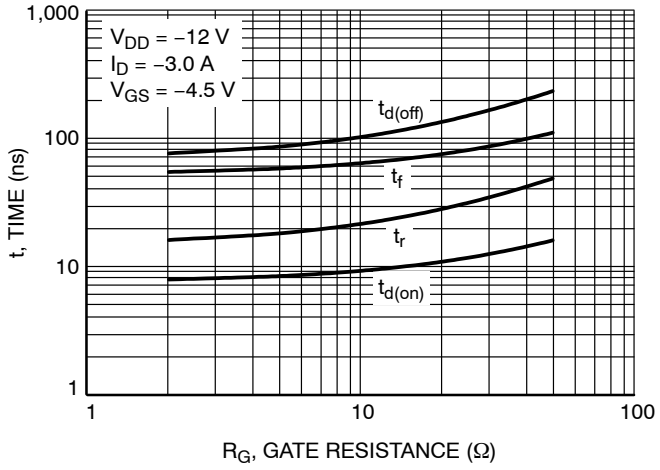



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**

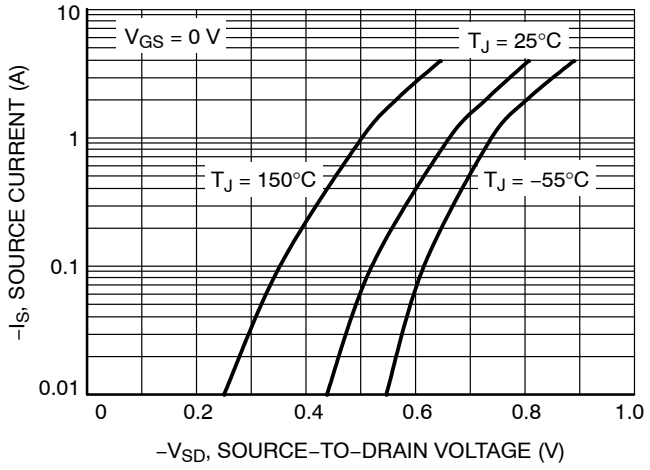
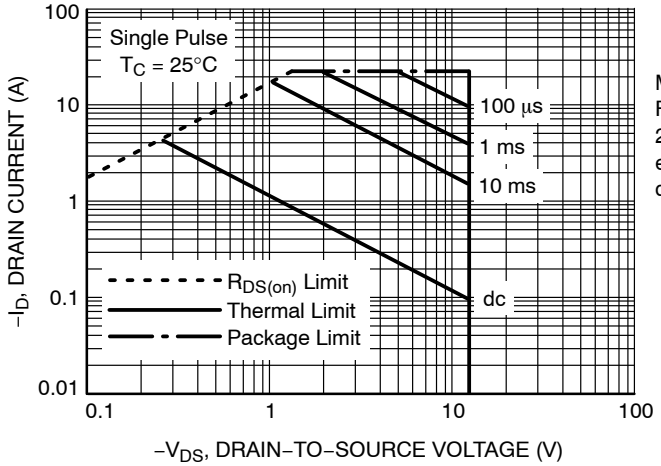



**Figure 12. Diode Forward Voltage vs. Current**




Mounted on 2″ sq. FR4 board (0.5″ sq. 2 oz. Cu single sided) with MOSFET die operating.

**Figure 13. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL CHARACTERISTICS − MOSFET

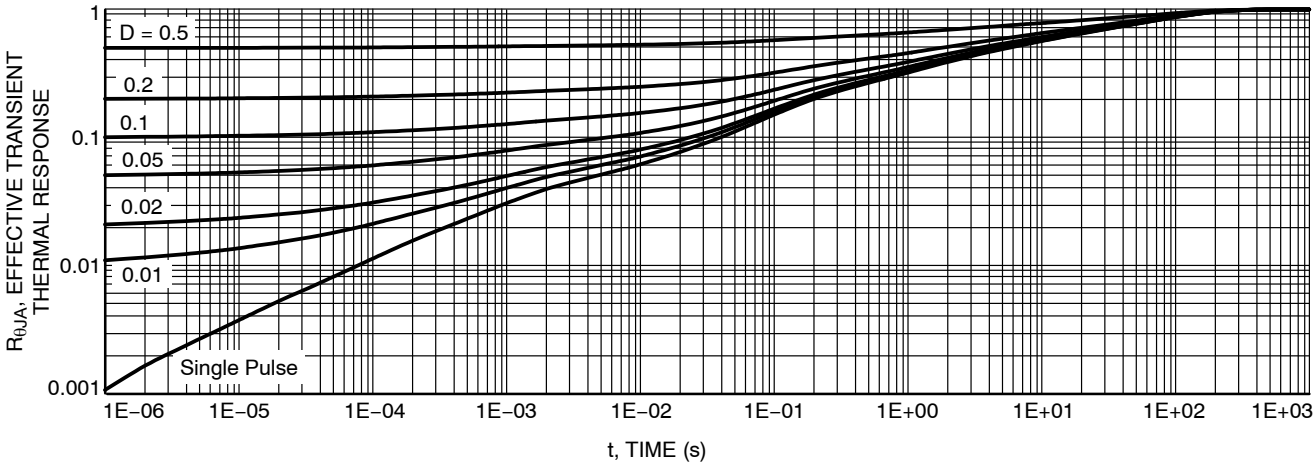



**Figure 14. FET Thermal Response**

## TYPICAL CHARACTERISTICS – BJT

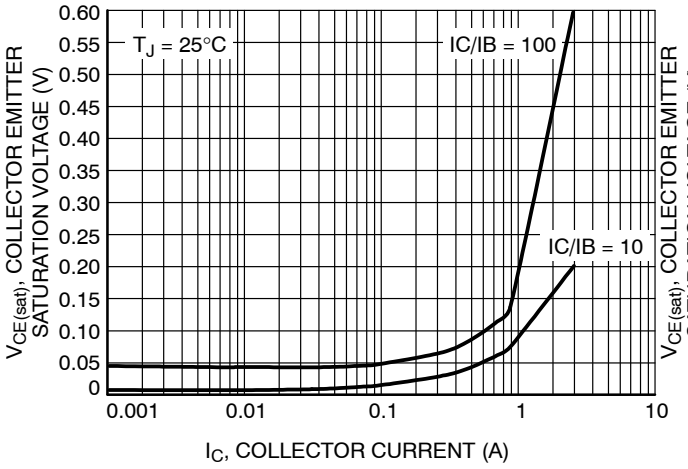



**Figure 15. Collector Emitter Saturation Voltage vs. Collector Current**

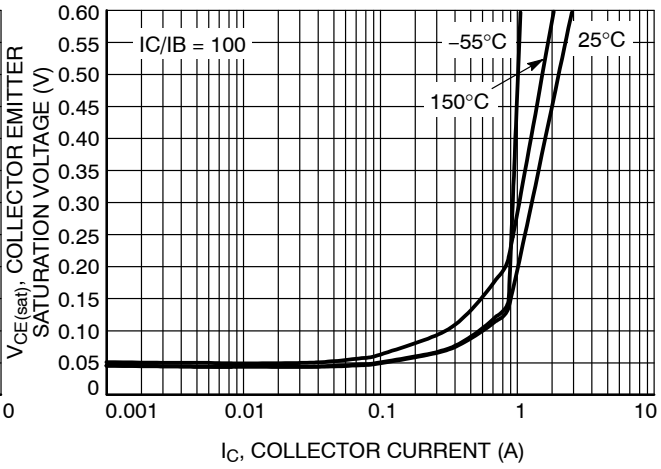



**Figure 16. Collector Emitter Saturation Voltage vs. Collector Current**

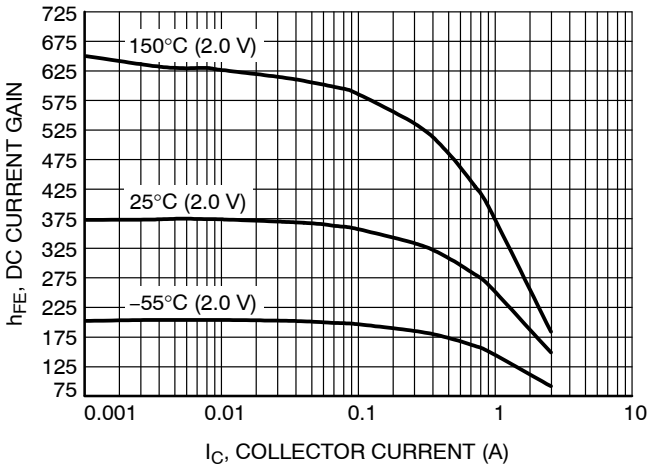



**Figure 17. DC Current Gain vs. Collector Current**

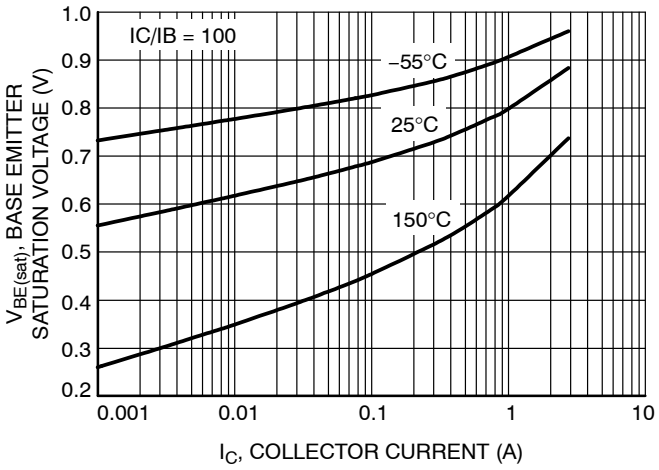



**Figure 18. Base Emitter Saturation Voltage vs. Collector Current**

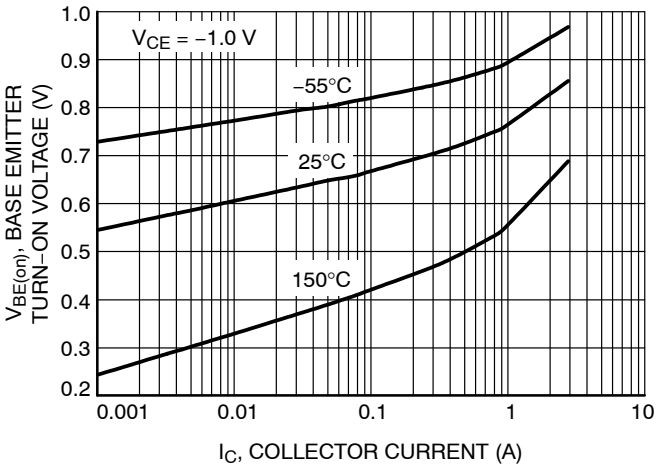



**Figure 19. Base Emitter Turn–On Voltage vs. Collector Current**

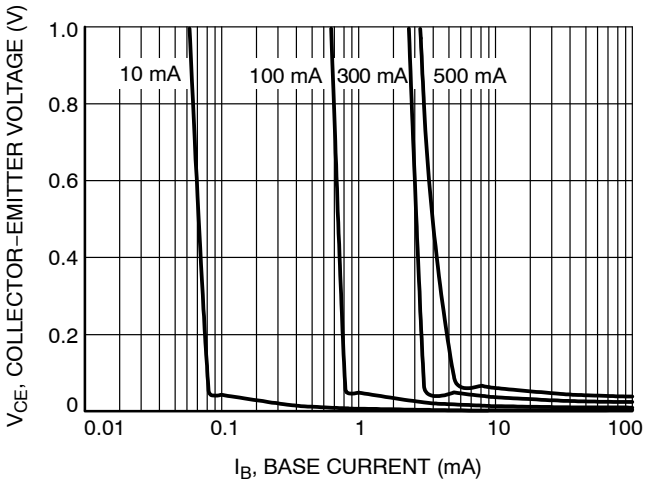



**Figure 20. Saturation Region**

## TYPICAL CHARACTERISTICS – BJT

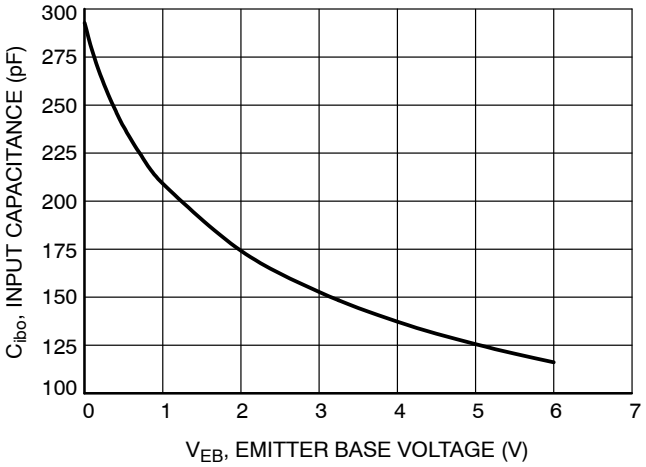



**Figure 21. Input Capacitance**

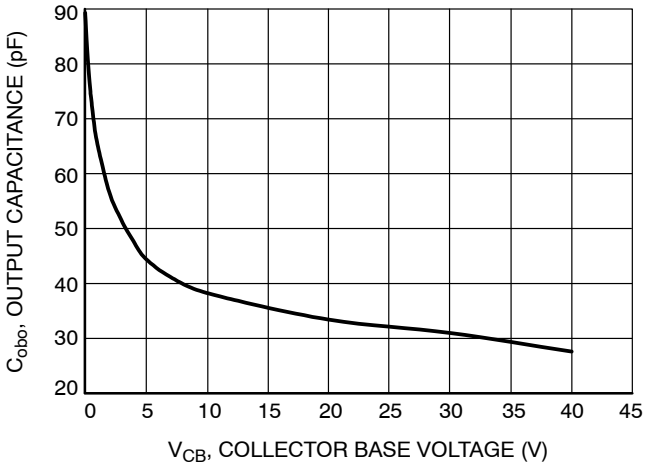



**Figure 22. Output Capacitance**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

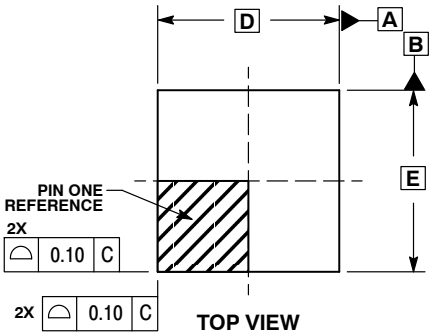
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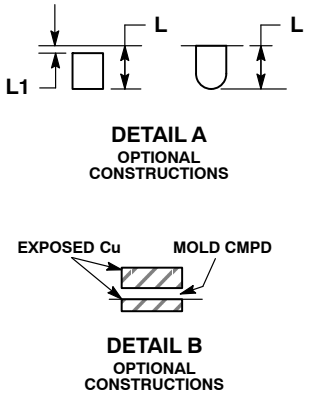



SCALE 2:1

**WDFN8, 3x3, 0.65P**
CASE 506BC−01
ISSUE A

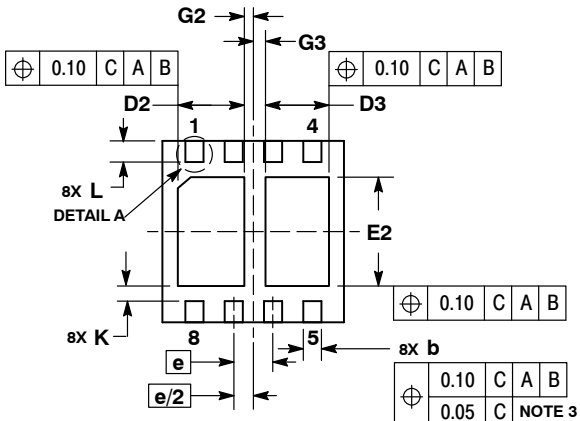
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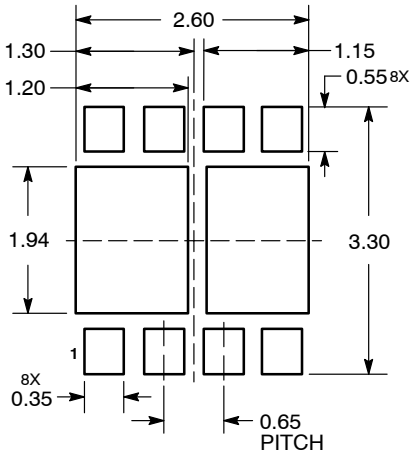




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 3.00 BSC | |
| D2 | 1.00 | 1.20 |
| D3 | 0.95 | 1.15 |
| E | 3.00 BSC | |
| E2 | 1.70 | 1.90 |
| e | 0.65 BSC | |
| G2 | 0.15 BSC | |
| G3 | 0.20 BSC | |
| K | 0.20 | --- |
| L | 0.25 | 0.45 |
| L1 | --- | 0.15 |




### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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|---|---|---|
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| **DESCRIPTION:** | **WDFN8, 3X3, 0.65P, DUAL FLAG** | **PAGE 1 OF 1** |

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