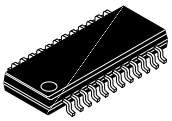
PACVGA200

VGA Port Companion Circuit

ON Semiconductor®

http://onsemi.com



QSOP24
QR SUFFIX
CASE 492B

MARKING DIAGRAM



PACVGA200QR = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
PACVGA200QR	QSOP24 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The PACVGA200 incorporates seven channels of ESD protection for all signal lines commonly found in a VGA port. ESD protection is implemented with current steering diodes designed to safely handle the high surge currents encountered with IEC−61000−4−2 Level−4 ESD Protection (±8 kV contact discharge). When a channel is subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into either the positive supply rail or ground where it may be safely dissipated. Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage Video Controller ICs and provide design flexibility in multi−supply−voltage environments.

Two non−inverting drivers provide buffering for the HSYNC and VSYNC signals from the Video Controller IC (SYNC_IN1, SYNC_IN2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and $V_{CC}4$.

These drivers have nominal 60 Ω output impedance (R_S) to match the characteristic impedance of the HSYNC & VSYNC lines of the video cables typically used in PC applications. Two N−channel FETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. Three 75 Ω termination resistors suitable for terminating the video signals from the video DAC are also provided. These resistors have separate input pins to allow insertion of additional EMI filtering, if required, between the termination point and the ESD protection diodes. These resistors are matched to better than 2% for excellent signal level matching for the R/G/B signals.

When the PWR_UP input is driven LOW, the SYNC inputs can be floated without causing the SYNC buffers to draw any current from the $V_{CC}4$ supply. When the PWR_UP input is LOW, the SYNC outputs are driven LOW.

An internal diode (D1 in schematic on previous page) is also provided so that $V_{CC}3$ can be derived from $V_{CC}4$, if desired, by connecting $V_{CC}3$ to V_BIAS. In applications where $V_{CC}4$ may be powered down, diode D1 blocks any DC current paths from the DDC_OUT pins back to the powered down $V_{CC}4$ rail via the top ESD protection diodes.

Features

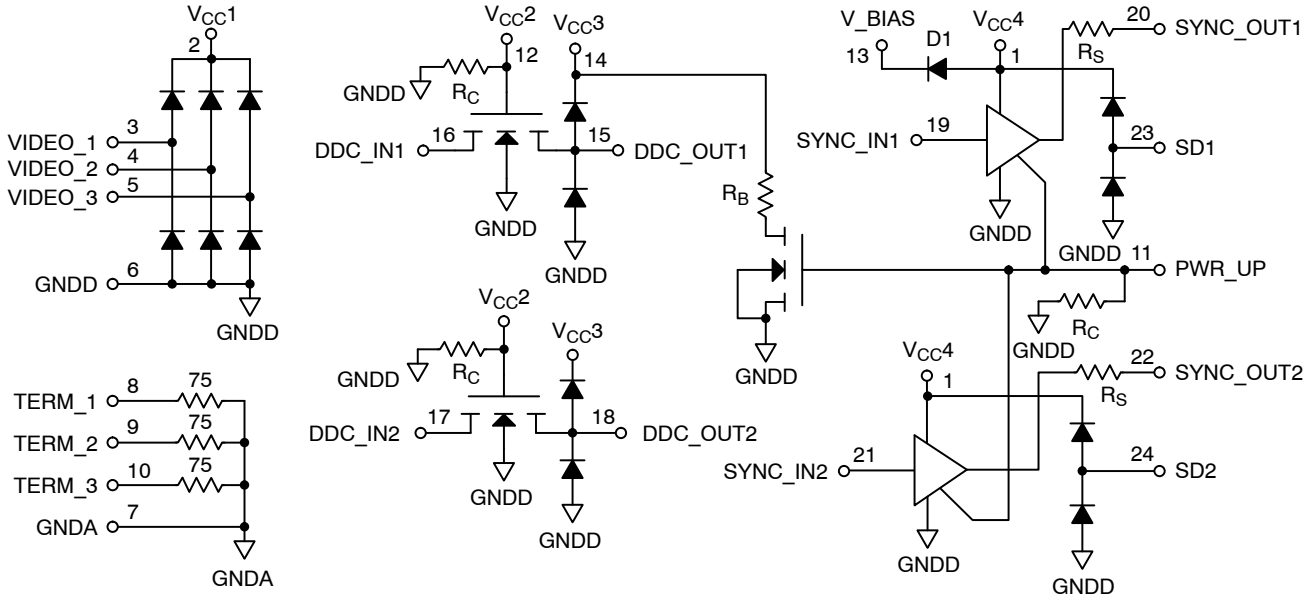
- Single Chip Solution for the VGA Port Interface
- Includes ESD Protection, Level Shifting, and RGB Termination
- Seven Channels of ESD Protection for All VGA Port Connector Pins Meeting IEC−61000−4−2 Level−4 ESD Requirements (±8 kV Contact Discharge)
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines, 4 pF Typical
- 75 Ω Termination Resistors for VIDEO Lines (Matched to 1% Typ.)
- TTL to CMOS Level−Translating Buffers with Power Down Mode for HSYNC and VSYNC Lines
- Bi−Directional Level Shifting N−Channel FETs Provided for DDC_CLK & DDC_DATA Channels
- Compact 24−Pin QSOP Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Notebook Computers with VGA Port
- Desktop PCs with VGA Port

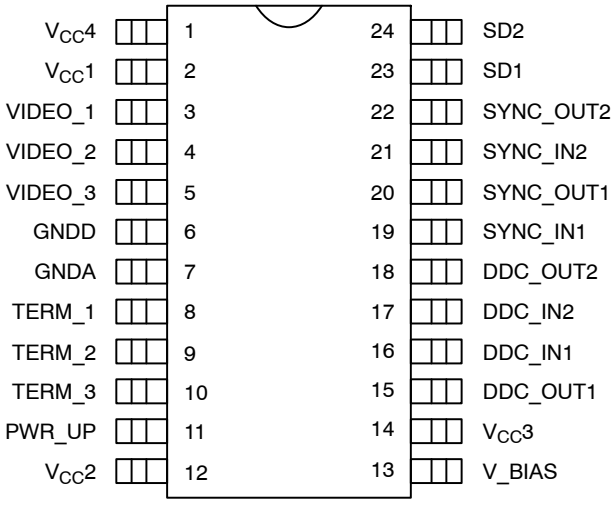
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SIMPLIFIED ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAMS

Top View



24−Pin QSOP

Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
1	$V_{CC}4$	Positive voltage supply pin. This is an isolated V_{CC} pin for the SYNC_1, SYNC_2, SD1 and SD2 circuits.
2	$V_{CC}1$	Positive voltage supply pin. This is an isolated V_{CC} pin for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD circuits.
3−5	VIDEO_1, VIDEO_2, VIDEO_3	RGB Video Protection Channels. These pins tie to the RGB video lines (for example, the Blue signal) between the VGA controller device and the video connector.
6	GNDD	Digital Ground reference supply pin.
7	GNDA	Ground reference supply pin for TERM_1, TERM_2 and TERM_3 pins.
8−10	TERM_1, TERM_2, TERM_3	RGB Video Termination Channels. These pins tie to the RGB video lines (for example, the Blue signal) providing a 75 Ω termination to GNDA for the given video channel.
11	PWR_UP	Sync Signal Output 1. Ties to the video connector side of one of the sync lines (for example the Horizontal Sync signal).
12	$V_{CC}2$	Positive voltage supply pin. This is an isolated V_{CC} pin for the DDC_IN1 and DDC_IN2 input circuits. Defines the logic one level for the DDC_OUTn outputs.
13	V_BIAS	Used to derive V_{CC3} from V_{CC4} input.
14	$V_{CC}3$	Positive voltage supply pin. This is an isolated V_{CC} pin for the DDC_OUT1 and DDC_OUT2 ESD protection circuits.
15	DDC_OUT1	DDC Signal Output 1. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).
16	DDC_IN1	DDC Signal Input 1. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).
17	DDC_IN2	DDC Signal Input 2. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Clk).
18	DDC_OUT2	DDC Signal Output 2. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Clk).
19	SYNC_IN1	Sync Signal Buffer Input 1. Connects to the VGA Controller side of one of the sync lines (for example, the Horizontal Sync signal).
20	SYNC_OUT1	Sync Signal Buffer Output 1. Connects to the video connector side of one of the sync lines (for example the Horizontal Sync signal).
21	SYNC_IN2	Sync Signal Buffer Input 2. Connects to the VGA Controller side of one of the sync lines (for example, the Vertical Sync signal).
22	SYNC_OUT2	Sync Signal Buffer Output 2. Connects to the video connector side of one of the sync lines (for example the Vertical Sync signal).
23	SD1	Sync Signal Filter 1. Connects to the video connector side of one of the sync lines (for example the Vertical Sync signal).
24	SD2	Sync Signal Filter 2. Connects to the video connector side of one of the sync lines (for example the Horizontal Sync signal).

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
$V_{CC}1$, $V_{CC}2$, $V_{CC}3$ and $V_{CC}4$ Supply Voltage	[GND − 0.5] to +6.0	V
Diode D1 Forward DC Current	100	μA
Storage Temperature Range	−65 to +150	°C
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 TERM_1, TERM_2, TERM_3 DDC_IN1, DDC_IN2 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2	 [GND − 0.5] to [$V_{CC}1$ + 0.5] −6.0, +6.0 [GND − 0.5] to [$V_{CC}2$ + 0.5] [GND − 0.5] to [$V_{CC}3$ + 0.5] [GND − 0.5] to [$V_{CC}4$ + 0.5]	V
Package Power Rating	1000	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	0 to +70	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC1}	$V_{CC}1$ Supply Current	$V_{CC}1$ = 5.0 V, VIDEO inputs at $V_{CC}1$ or GND level			10	μA
I_{CC2}, I_{CC3}	$V_{CC}2$ & $V_{CC}3$ Supply Current	$V_{CC}2$ = $V_{CC}3$ = 5.0 V			10	μA
I_{CC4}	$V_{CC}4$ Supply Current	$V_{CC}4$ = 5.0 V, SYNC Inputs at GND or $V_{CC}4$ Level, PWR−UP pin at $V_{CC}4$, SYNC Outputs Unloaded		10		μA
		$V_{CC}4$ = 5.0 V, SYNC Inputs at 3.0 V, PWR−UP Pin at $V_{CC}4$, SYNC Outputs Unloaded		200		μA
		$V_{CC}4$ = 5.0 V, PWR−UP Input at GND, SYNC Outputs Unloaded			10	μA
V_{BIAS}	V_{BIAS} Open Circuit Voltage	No External Current Drawn from V_{BIAS} Pin		$V_{CC}4$−0.8		V
R_T	Video Termination Resistance		71.25	75	78.75	Ω
	R_T Resistance Matching			1	2	%
V_{IH}	Logic High Input Voltage	$V_{CC}4$ = 5.0 V (Note 2)	2.0			V
V_{IL}	Logic Low Input Voltage	$V_{CC}4$ = 5.0 V (Note 2)			0.8	V
V_{OH}	Logic High Output Voltage	I_{OH} = −4 mA, $V_{CC}4$ = 5.0 V (Note 2)	4.5		4.8	V
V_{OL}	Logic Low Output Voltage	I_{OL} = 4 mA, $V_{CC}4$ = 5.0 V (Note 2)	0.18		0.32	V
R_{OH}	Output Resistance	(Note 2)	50		125	Ω
R_{OL}			45		80	Ω
R_B, R_P	Resistor Value	PWR_UP = $V_{CC}3$ = 5.0 V	0.5	1.0	2.0	MΩ
R_C	$V_{CC}2$ Pull−down Resistor Value	$V_{CC}2$ = 3.0 V	0.5	1.5	3.0	MΩ
I_N	Input Current VIDEO Inputs HSYNC, VSYNC Inputs	 $V_{CC}1$= 5.0 V, V_{IN} = $V_{CC}1$ or GND $V_{CC}4$ = 5.0 V, V_{IN} = $V_{CC}4$ or GND			 ±1 ±1	μA

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OFF}	Off−State Leakage Current, Level−Shifting NFET	($V_{CC}2$ − V_{DDC_IN}) ≤ 0.4 V, V_{DDC_OUT} = $V_{CC}2$ ($V_{CC}2$ − V_{DDC_OUT}) ≤ 0.4 V, V_{DDC_IN} = $V_{CC}2$			10 10	μA
V_{ON}	Voltage Drop Across Level Shifting NFET when Turned ON	$V_{CC}2$ = 2.5 V, V_S = GND, I_{DS} = 3 mA			0.15	V
C_{IN}	Input Capacitance VIDEO_1,VIDEO_2 & VIDEO_3 Inputs	 $V_{CC}1$ = 5.0 V, V_{IN} = 2.5 V, Measured at 1 MHz $V_{CC}1$ = 2.5 V, V_{IN} = 1.25 V, Measured at 1 MHz	 3.0 3.0	 4.0 4.5	 5.0 5.6	pF
t_{PLH}	SYNC Drivers L ≥ H Propagation Delay	C_L = 50 pF, V_{CC} = 5.0 V, Input t_R and t_F ≤ 5 ns		8.0	12.0	ns
t_{PHL}	SYNC Drivers H ≥ L Propagation Delay	C_L = 50 pF, V_{CC} = 5.0 V, Input t_R and t_F ≤ 5 ns		8.0	12.0	ns
t_R, t_F	SYNC Drivers Output Rise & Fall Times	C_L = 50 pF, V_{CC} = 5.0 V, Input t_R and t_F ≤ 5 ns (Measured 10% − 90%)	5.0	7.0	10.0	ns
V_{ESD}	ESD Withstand Voltage	$V_{CC}1$ = $V_{CC}3$ = $V_{CC}4$ = 5 V (Note 3)	±8			kV

1. All parameters specified over standard operating conditions unless otherwise noted.
2. This parameter applies only to the HSYNC and VSYNC channels. HSYNC and VSYNC have 8 mA drivers with R_S added in series to terminate transmission line.
3. Per the IEC−61000−4−2 International ESD Standard, Level 4 contact discharge method. $V_{CC}1$, $V_{CC}3$ and $V_{CC}4$ must be bypassed to GND via a low impedance ground plane with a 0.2 μF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SD1, SYNC_OUT2, SD2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard 2 kV per the Human Body Model (MIL−STD−883, Method 3015).

TEST CIRCUIT INFORMATION

Average Current through $V_{CC}4$ ($I_{CC}4$)

The circuit in Figure 1 was used to characterize $I_{CC}4$ current as SYNC_IN signal frequency varies. A square wave signal was connected to the input of one of the SYNC buffers (i.e. pin 19 or pin 21). The frequency of this signal was varied between 0 and 100 kHz. The risetime and falltime was kept constant at 10 ns. Three different values of C1 were used: 0 pF, 50 pF and 100 pF. The results are plotted in Figure 2.

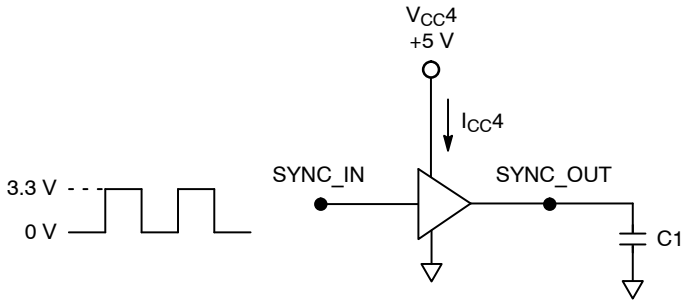


Figure 1. Sync Buffer $I_{CC}4$ Test Circuit

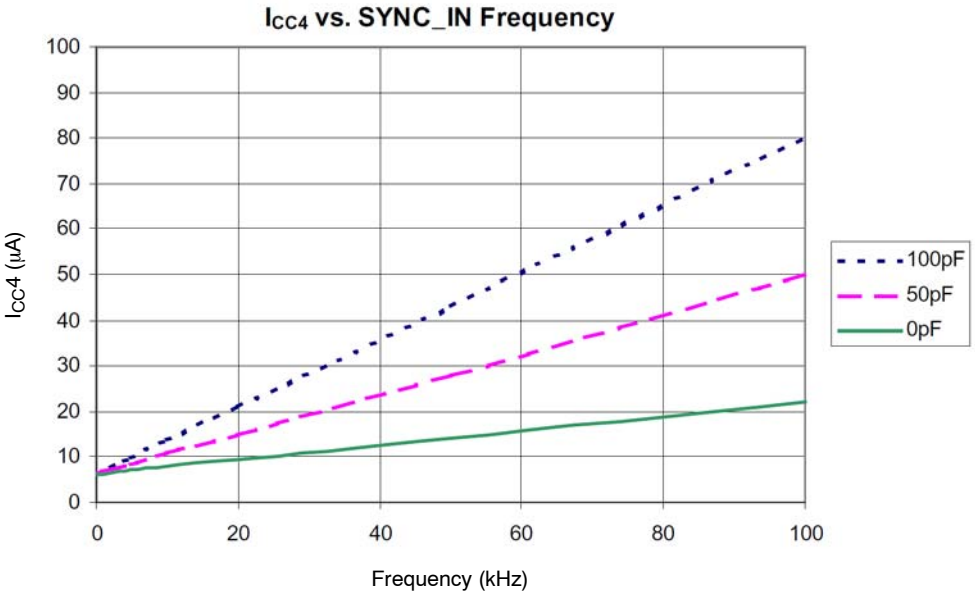


Figure 2. $I_{CC}4$ vs. SYNC_IN Frequency Performance Data

APPLICATION INFORMATION

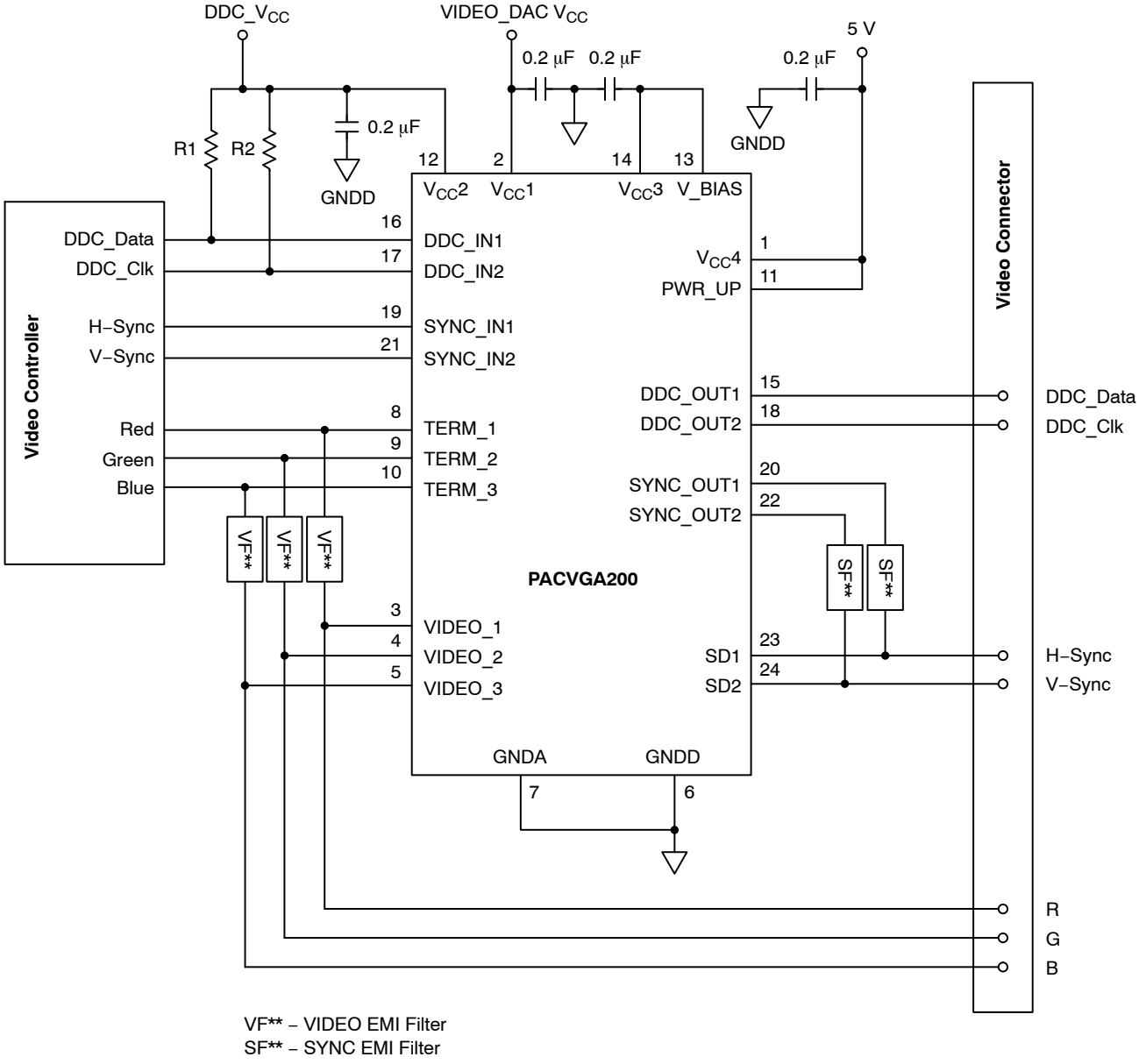


Figure 3. Typical Connection Diagram

A resistor may be necessary between the $V_{CC}3$ pin and ground if protection against a stream of ESD pulses is required while the PACVGA200 is in the power−down state. The value of this resistor should be chosen such that the extra charge deposited into the $V_{CC}3$ bypass capacitor by each ESD pulse will be discharged before the next ESD pulse occurs. The maximum ESD repetition rate specified by the IEC−61000−4−2 standard is one pulse per second. When the PACVGA200 is in the power−up state, an internal discharge resistor is connected to ground via an FET switch for this purpose.

For the same reason, $V_{CC}1$ and $V_{CC}4$ may also require bypass capacitor discharging resistors to ground if there are no other components in the system to provide a discharge path to ground.

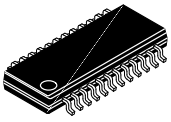
GNDA, the reference voltage for the 75 Ω resistors is not connected internally to GNDD and should ideally be connected to the ground of the video DAC IC.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

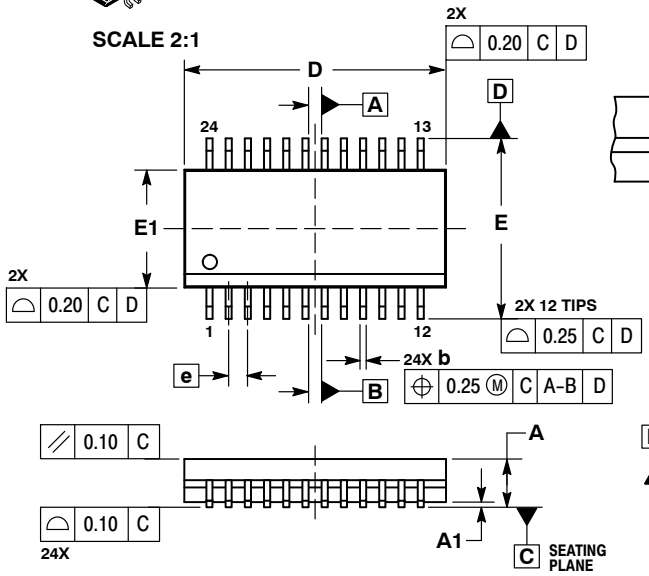
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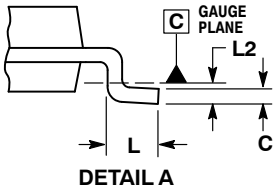
QSOP24 NB
CASE 492B–01
ISSUE A

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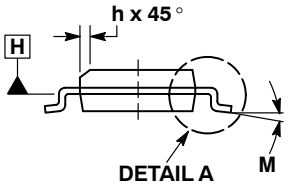


SCALE 2:1





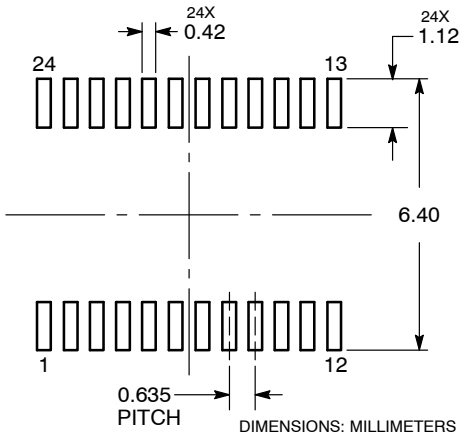
DETAIL A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

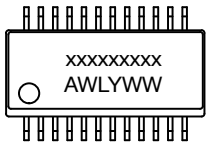
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.20	0.30
C	0.19	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
h	0.22	0.50
L	0.40	1.27
L2	0.25 BSC	
M	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G”, may or not be present.

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