Low-Power Ground Fault Interrupter

RV4145A

Description

The RV4145A is a low−power controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as equipment (connected to opposite phases of the AC line) in contact with a pool of water and open circuits the line before a harmful or lethal shock occurs.

A 26 V Zener shunt regulator, an operational amplifier, and an SCR driver are contained internally. With the addition of two sense transformers, a bridge rectifier, an SCR, a relay, and a few additional components; the RV4145A can detect and protect against both hot−wire− to−ground and neutral−wire−to−ground faults. The simple layout and conventional design ensure ease of application and long−term reliability.

Features

- No Potentiometer Required
- Direct Interface to Silicon−Controlled Rectifier (SCR)
- Supply Voltage Derived from AC Line – 26 V Shunt
- Adjustable Sensitivity
- Grounded Neutral Fault Detection
- Meets U.L. 943 Standards
- 450 μA Quiescent Current
- Ideal for 120 V or 220 V Systems
- These are Pb−Free Devices

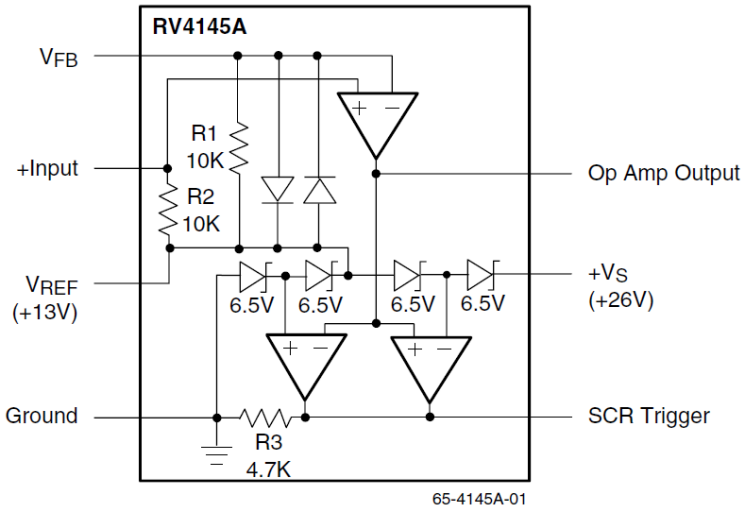
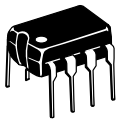


Figure 1. Block Diagram

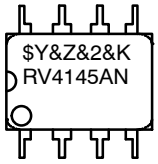
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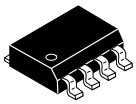
www.onsemi.com

MARKING DIAGRAM

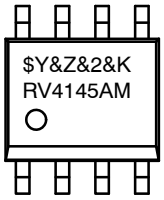


PDIP−8
CASE 626−05





SOIC8
CASE 751EB



RV4145AN, RV4145AM	= Specific Device Code
$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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PIN CONFIGURATION

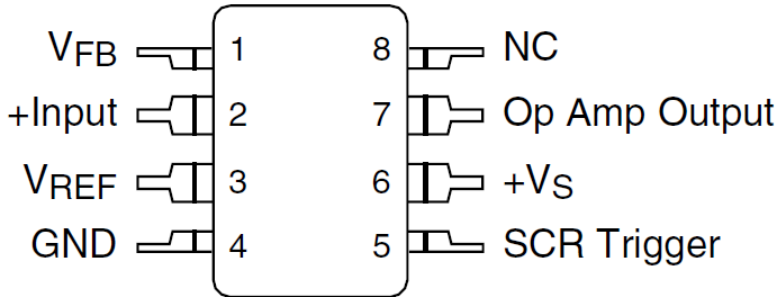


Figure 2. Pin Assignment

PIN DESCRIPTION

Pin No.	Name	Description
1	V_{FB}	Sense amplifier negative input
2	+Input	Sense amplifier positive input
3	V_{REF}	Reference Voltage
4	GND	Ground
5	SCR Trigger	Output for triggering external SCR when a fault is detected
6	$+V_S$	Supply input for RV4145A circuitry
7	Op Amp Output	Sense Amplifier Output
8	NC	No Connect

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Min	Typ	Max	Unit
V_{CC}	Supply Current			–	–	18	mA
P_D	Internal Power Dissipation			–	–	500	mW
T_{STG}	Storage Temperature Range			–65	–	+150	°C
T_A	Operating Temperature Range			–35	–	+85	°C
T_J	Junction Temperature			–	–	125	°C
T_L	Lead Soldering Temperature		60 s, DIP	–	–	300	°C
			10 s, SOIC	–	–	260	
P_D	Power Dissipation	T_A <50°C	SOIC	–	–	300	mW
			PDIP	–	–	450	
		T_A <50°C Derate	SOIC	–	4	–	mW/°C
			PDIP	–	6	–	
Θ_{JA}	Thermal Resistance		SOIC	–	240	–	°C/W
			PDIP	–	160	–	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (I_S = 1.5 mA and T_A = +25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Detector Reference Voltage	Pin 7 to Pin 3	6.8	7.2	8.1	±V
SHUNT REGULATOR						
$+V_S$	Zener Voltage	Pin 6 to Pin 4	25.0	26.0	29.2	V
V_{REF}	Reference Voltage	Pin 3 to Pin 4	12.5	13.0	14.6	V
I_s	Quiescent Current	$+V_S$ = 24 V	–	450	750	μA
OPERATION AMPLIFIER						
	Offset Voltage	Pin 2 to Pin 3	−3.0	0.5	+3.0	mV
	+Output Voltage Swing	Pin 7 to Pin 3	6.8	7.2	8.1	V
	−Output Voltage Swing	Pin 7 to Pin 3	−9.5	−11.2	−13.5	V
	+Output Source Current	Pin 7 to Pin 3	–	650	–	μA
	−Output Source Current	Pin 7 to Pin 3	–	1.0	–	mA
	Gain Bandwidth Product	f = 50 kHz	1.0	1.8	–	MHz
RESISTORS						
R1	Resistors, I_S = 0 mA	Pin 1 to Pin 3	–	10	–	kΩ
R2		Pin 2 to Pin 3	–	10	–	
R3		Pin 5 to Pin 4	3.5	4.7	5.9	
SCR TRIGGER						
	Detector On	Pin 5 to Pin 4	1.5	2.8	–	V
	Detector Off		0	1	10	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (I_S = 1.5 mA and −35°C ≤ T_A ≤ +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Detector Reference Voltage	Pin 7 to Pin 3	6.5	7.2	8.3	±V
SHUNT REGULATOR						
$+V_S$	Zener Voltage	Pin 6 to Pin 4	24	26	30	V
V_{REF}	Reference Voltage	Pin 3 to Pin 4	12	13	15	V
I_s	Quiescent Current	$+V_S$ = 24 V	–	500	–	μA
OPERATION AMPLIFIER						
	Offset Voltage	Pin 2 to Pin 3	−5.0	0.5	+5.0	mV
	+Output Voltage Swing	Pin 7 to Pin 3	6.5	7.2	8.3	V
	−Output Voltage Swing	Pin 7 to Pin 3	−9.0	−11.2	−14.0	V
	Gain Bandwidth Product	f = 50 kHz	–	1.8	–	MHz
RESISTORS						
R1	Resistors, I_S = 0 mA	Pin 1 to Pin 3	–	10	–	kΩ
R2		Pin 2 to Pin 3	–	10	–	
R3		Pin 5 to Pin 4	3.5	4.7	5.9	
SCR TRIGGER						
	Detector On	Pin 5 to Pin 4	1.3	2.8	–	V
	Detector Off		0	3	50	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PRINCIPLES OF OPERATION

The 26 V shunt regulator voltage generated by the string of Zener diodes is divided into three reference voltages: ¾ V_S, ½ V_S, and ¼ V_S. V_{REF} is at ½ V_S and is used as a reference to create an artificial ground of

+13 V at the operational amplifier non−inverting input.

Figure 3 shows a three−wire 120 V AC outlet GFI application using an RV4145A. Fault signals from the sense transformer are AC coupled into the input and are amplified according to the following equation:

$$V_7 = R_{SENSE} \times I_{SENSE}/N \quad \text{(eq. 1)}$$

where V_7 is the RMS voltage at pin 7 relative to pin 3, R_{SENSE} is the value of the feedback resistor connected from pin 7 to pin 1, I_{SENSE} is the fault current (in amps) RMS, and N is the turns ratio of the transformer.

When V_7 exceeds ±7.2 V relative to pin 3, the SCR trigger output goes high and fires the external SCR.

The formula for V_7 is approximate because it does not include the sense transformer characteristics.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between the sense transformer and the grounded neutral transformer. The resultant AC coupling closes a positive feedback path around the op amp, and the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds, the SCR output goes high.

Shunt Regulator

The R_{LINE} limits the current into the shunt regulator; 220 V applications must substitute a 47 kΩ 2 W resistor. In addition to supplying power to the IC, the shunt regulator creates internal reference voltages.

Operational Amplifier

R_{SENSE} is a feedback resistor that sets gain and, therefore sensitivity to normal faults. To adjust R_{SENSE}, apply the desired fault current (a difference in current of 5 mA is the UL 943 standard) then adjust R_{SENSE} upward until the SCR activates. A fixed resistor can be used for R_{SENSE} because the resultant ±15% variation in sensitivity meets UL's 943 4 – 6 mA specification window.

The roll−off frequency is greater than the grounded neutral fault oscillation frequency to preserve loop gain for oscillation (which is determined by the inductance of the 200:1 transformer and C4).

The sensitivity to grounded neutral faults is adjusted by changing the frequency of oscillation. Increasing the frequency reduces the sensitivity by reducing the loop gain of the positive feedback circuit. As frequency increases, the signal becomes attenuated and the loop gain decreases. With the values shown in Figure 3, the circuit detects a grounded neutral with resistance of 2 Ω or less.

The input to the operational amplifier is protected from over−voltage by back−to−back diodes.

Silicon−Controlled Rectifier (SCR) Driver

The SCR must have a high dV/dt rating to ensure that line noise (generated by noisy appliances, such as a drill motor) does not falsely trigger the SCR. The SCR must have a gate−drive requirement of less than 200 μA. C_F is a noise filter capacitor that prevents narrow pulses from firing the SCR.

The relay solenoid should have a 3 ms or less response time to meet the UL 943 timing requirement.

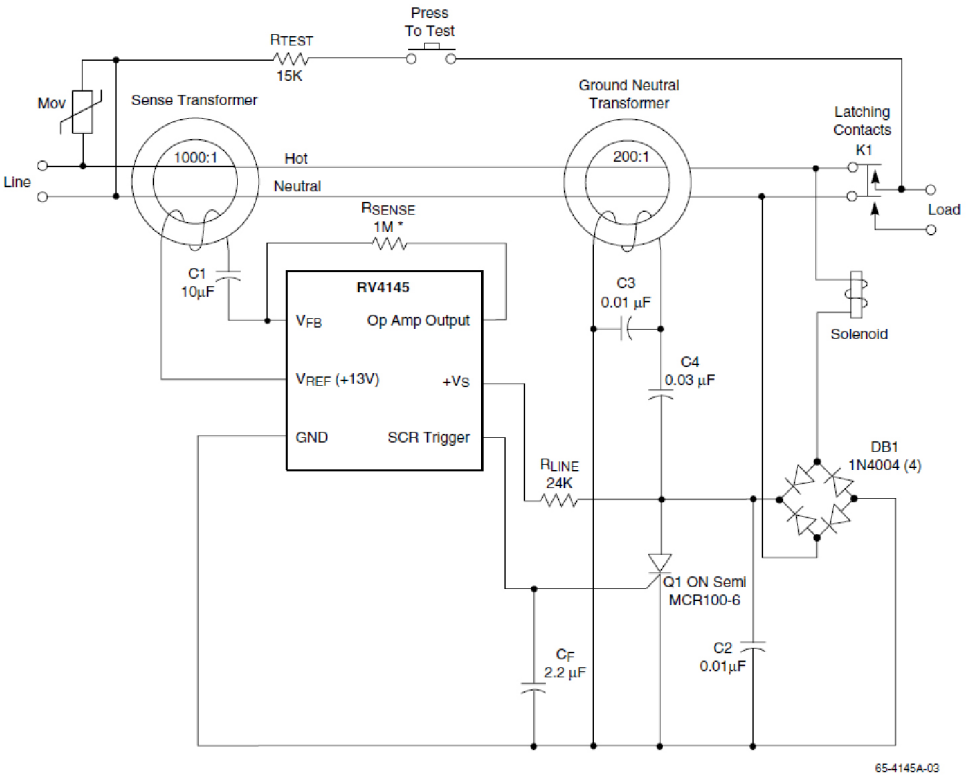
Sense Transformers and Cores

The sense and grounded neutral transformer cores are usually fabricated using high permeability laminated steel rings. Their single−turn primary is created by passing the line and neutral wires through the center of the core. The secondary is usually 200 to 1500 turns.

Magnetic Metals Corporation www.magmet.com is a full line suppliers of ring cores and transformers designed specifically for GFI applications.

Two−Wire Application Circuit

Figure 4 shows the diagram of a two−wire 120 V AC outlet GFI circuit using an RV4145A. This circuit is not designed to detect grounded neutral faults. For this reason, the grounded neutral transformer and capacitors C3 and C4 of Figure 3 are not used.



* Value depends on transformer characteristics.

Figure 3. GFI Application Circuit (Three−Wire Outlet)

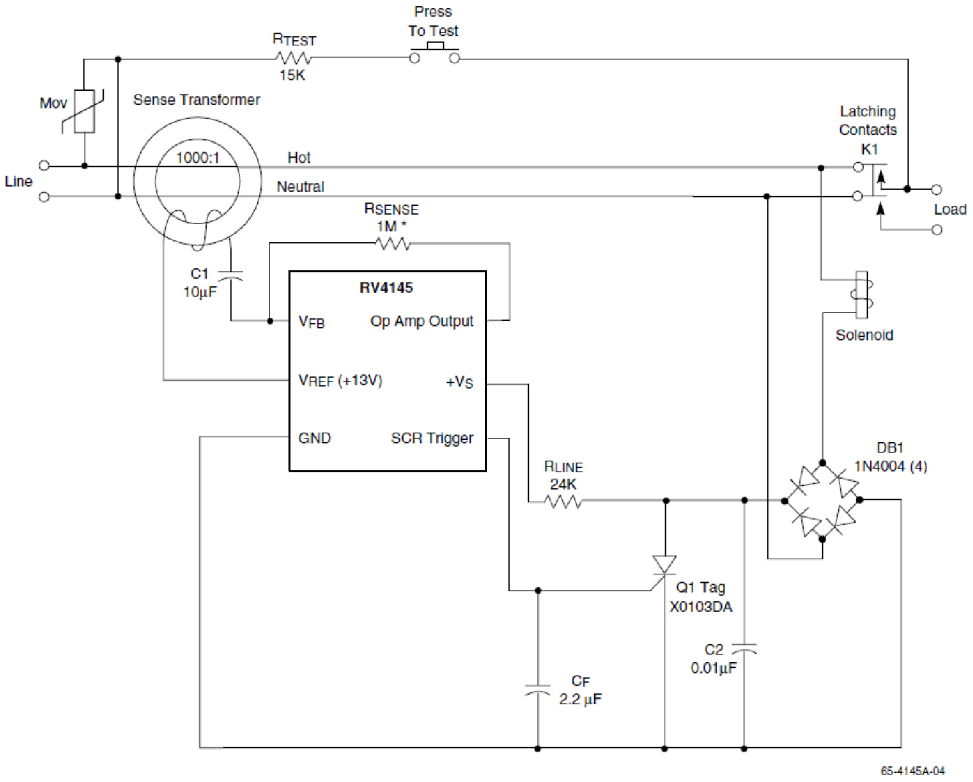


Figure 4. GFI Application Circuit (Two−Wire Outlet)

SCHEMATIC DIAGRAM

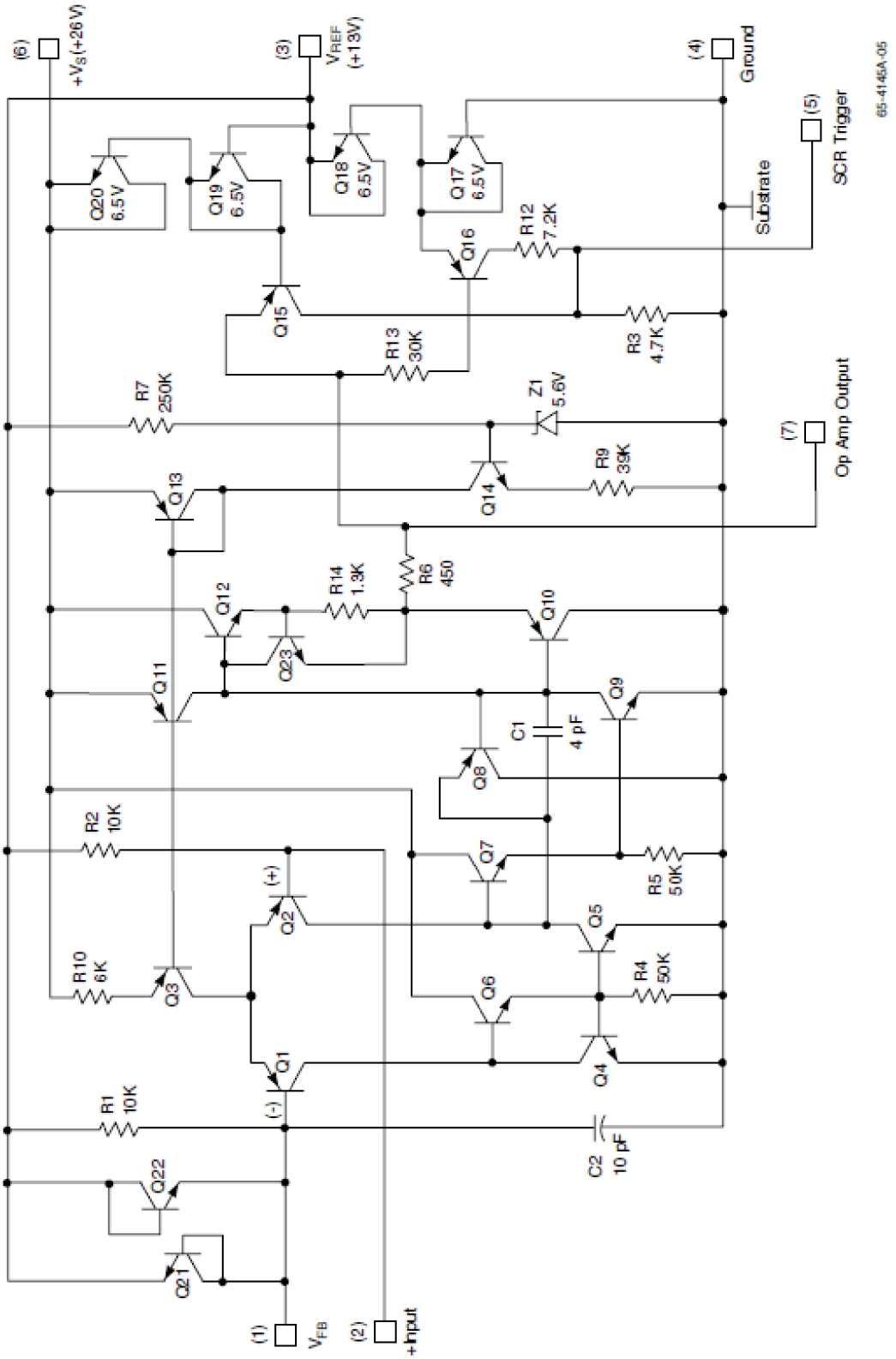


Figure 5. Schematic

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
RV4145AN	−35°C to +85°C	8−Lead, MDIP, JEDEC MS−001, .300" Wide (Pb−Free)	40 Units /Tube
RV4145AMT		8−Lead, SOIC, JEDEC MS−012, .150" Narrow Body (Pb−Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

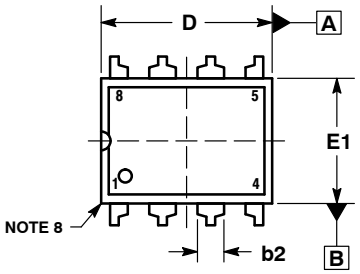
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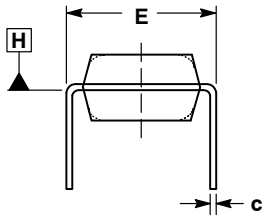
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ISSUE P

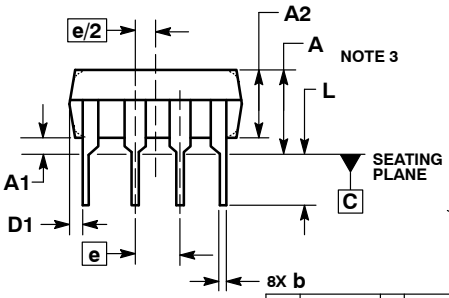
DATE 22 APR 2015



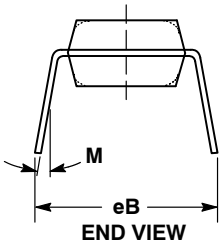
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



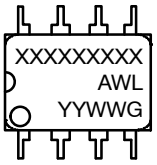
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

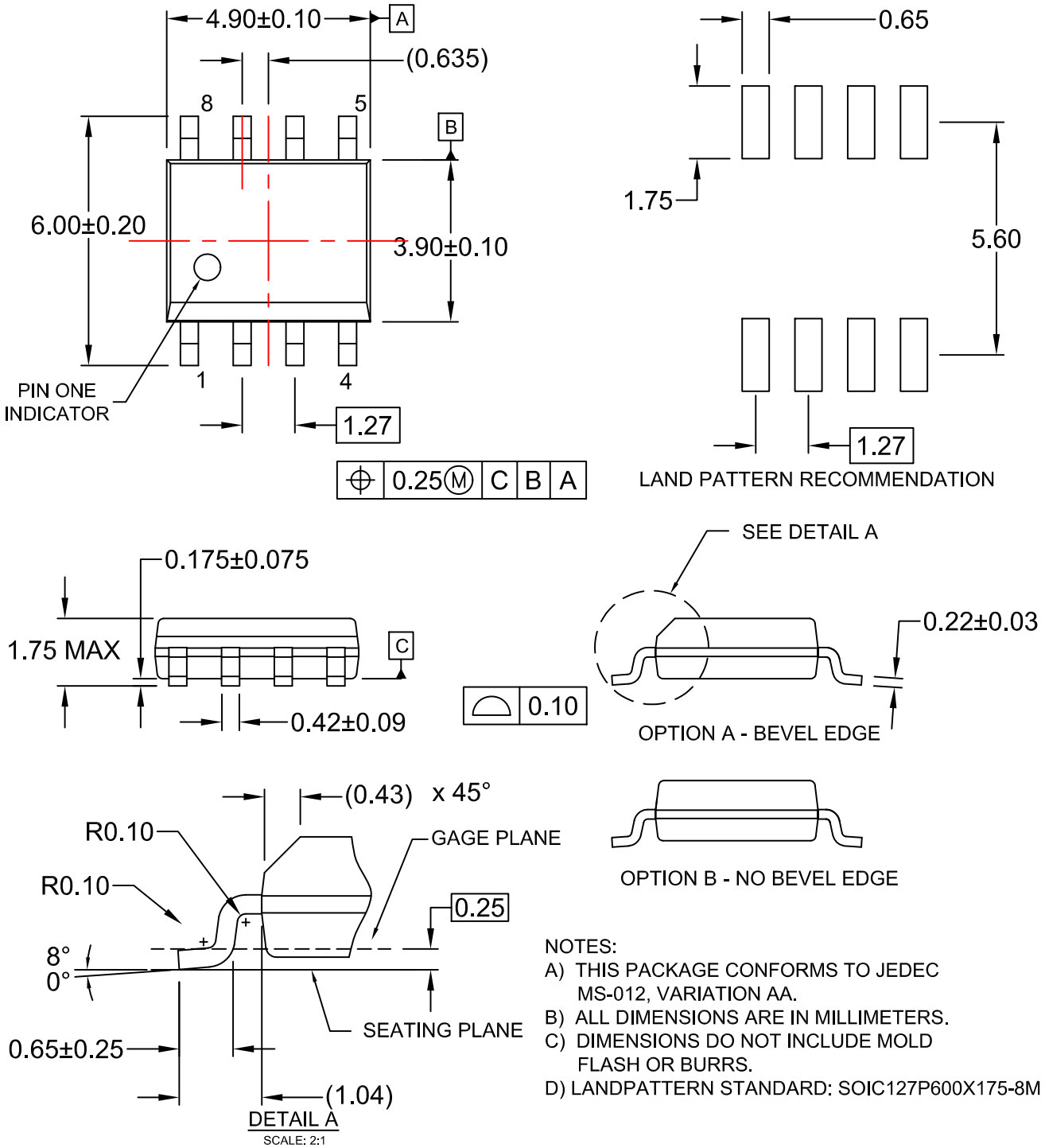
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CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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