# 50 A VRPower® Integrated Power Stage

## DESCRIPTION

The SiC639 are integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 5 mm x 5 mm MLP package, SiC639 enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art Gen IV TrenchFET® technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC639 incorporate an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, a thermal warning (THWn) that alerts the system of excessive junction temperature, and zero current detection to improve light load efficiency. The drivers are also compatible with a wide range of PWM controllers and supports tri-state PWM, 3.3 V, 5 V PWM logic.

## FEATURES

RoHS COMPLIANT HALOGEN FREE

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's Gen IV MOSFET technology and a low side MOSFET with integrated Schottky diode
- Delivers up to 50 A continuous current
- High efficiency performance
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 19 V input stage
- 3.3 V, 5 V PWM logic with tri-state and hold-off
- Zero current detect control for light load efficiency improvement
- Low PWM propagation delay (< 20 ns)
- Faster disable
- Thermal monitor flag
- Under voltage lockout for $V_{CIN}$
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

## APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-8/9 VRPower delivery
  - $V_{CORE}$, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$ Skylake, Kabylake platforms
  - $V_{CCGI}$ for Apollo Lake platforms
- Up to 24 V rail input DC/DC VR modules

## TYPICAL APPLICATION DIAGRAM

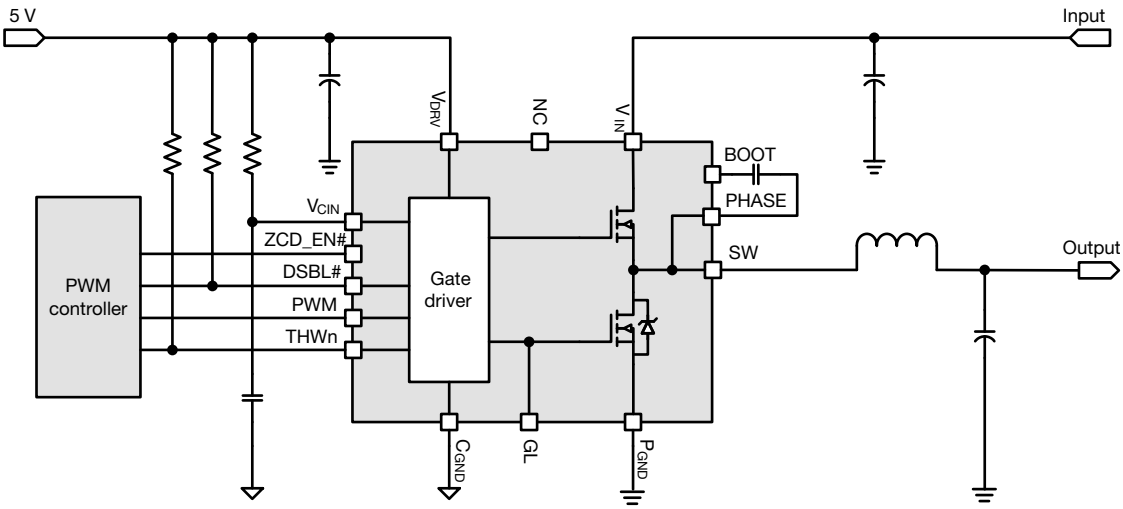


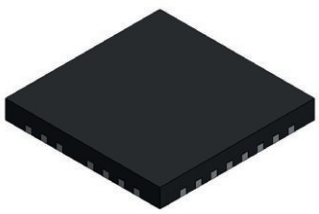

**Fig. 1 - SiC639 and SiC639A Typical Application Diagram**

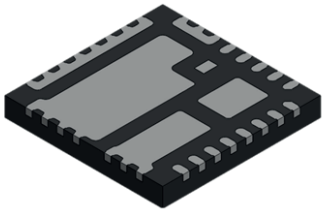


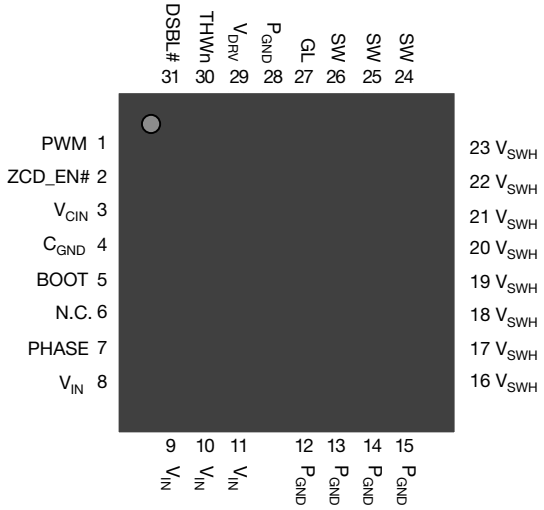
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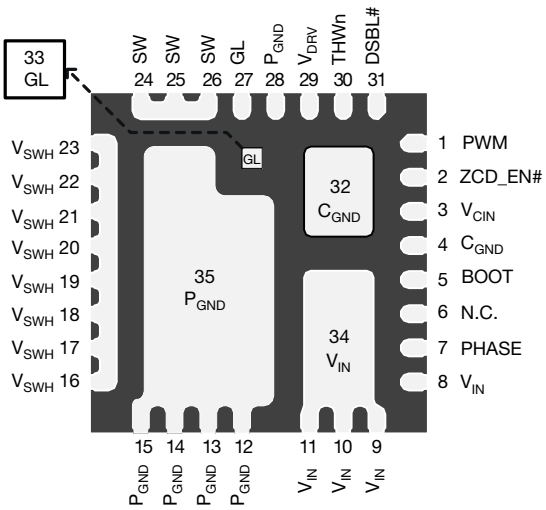
## PINOUT CONFIGURATION








Top view




Bottom view

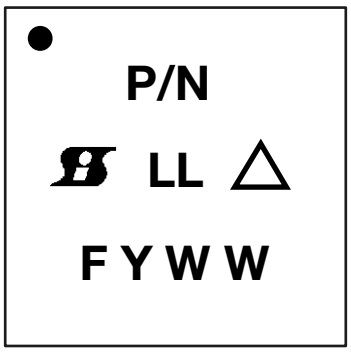
**Fig. 2 - SiC639 Pin Configuration**

| PIN CONFIGURATION | | |
|---|---|---|
| **PIN NUMBER** | **NAME** | **FUNCTION** |
| 1 | PWM | PWM input logic |
| 2 | ZCD_EN# | The ZCD_EN# pin enables or disables zero cross detection on inductor current when it detects PWM = mid.<br>When ZCD_EN# is LOW, GL stays on until ZCD detected when it detects PWM = mid.<br>When ZCD_EN# is HIGH, GL turns off when it detects PWM = mid.or PWM = 1 |
| 3 | $V_{CIN}$ | Supply voltage for internal logic circuitry |
| 4, 32 | $C_{GND}$ | Signal ground |
| 5 | BOOT | High side driver bootstrap voltage |
| 6 | N.C. | Not connected internally, can be left floating or connected to ground |
| 7 | PHASE | Return path of high side gate driver |
| 8 to 11, 34 | $V_{IN}$ | Power stage input voltage. Drain of high side MOSFET |
| 12 to 15, 28, 35 | $P_{GND}$ | Power ground |
| 16 to 26 | $V_{SWH}$ | Phase node of the power stage |
| 27, 33 | GL | Low side MOSFET gate signal |
| 29 | $V_{DRV}$ | Supply voltage for internal gate driver |
| 30 | THWn | Thermal warning open drain output |
| 31 | DSBL# | Disable pin. Active low |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **PART NUMBER** | **PACKAGE** | **MARKING CODE** | **OPTION** |
| SiC639CD-T1-GE3 | PowerPAK MLP55-31L | SiC639 | 5 V PWM optimized |
| SiC639ACD-T1-GE3 | PowerPAK MLP55-31L | SiC639A | 3.3 V PWM optimized |
| SiC639DB | Reference board | | |


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## PART MARKING INFORMATION




| | | |
|---|---|---|
| ● | = | pin 1 indicator |
| P/N | = | part number code |
| | = | Siliconix logo |
| △ | = | ESD symbol |
| F | = | assembly factory code |
| Y | = | year code |
| WW | = | week code |
| LL | = | lot code |

## ABSOLUTE MAXIMUM RATINGS

| ELECTRICAL PARAMETER | CONDITIONS | LIMIT | UNIT |
|---|---|---|---|
| Input voltage | $V_{IN}$ | -0.3 to +30 | V |
| Control logic supply voltage | $V_{CIN}$ | -0.3 to +7 | |
| Drive supply voltage | $V_{DRV}$ | -0.3 to +7 | |
| Switch node (DC voltage) | $V_{SWH}$ | -0.3 to +30 | |
| Switch node (AC voltage) (1) | | -7 to +35 | |
| BOOT voltage (DC voltage) | $V_{BOOT}$ | 35 | |
| BOOT voltage (AC voltage) (2) | | 40 | |
| BOOT to PHASE (DC voltage) | $V_{BOOT-PHASE}$ | -0.3 to +7 | |
| BOOT to PHASE (AC voltage) (3) | | -0.3 to +8 | |
| All logic inputs and outputs (PWM, DSBL#, and THWn) | | -0.3 to $V_{CIN}$ + 0.3 | |
| Max. operating junction temperature | $T_J$ | 150 | °C |
| Ambient temperature | $T_A$ | -40 to +125 | |
| Storage temperature | $T_{stg}$ | -65 to +150 | |
| Electrostatic discharge protection | Human body model, JESD22-A114 | 3000 | V |
| | Charged device model, JESD22-C101 | 1000 | |

**Notes**

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

(1) The specification values indicated “AC” is $V_{SWH}$ to $P_{GND}$ -8 V (< 20 ns, 10 µJ), min. and 35 V (< 50 ns), max.
(2) The specification value indicates “AC voltage” is $V_{BOOT}$ to $P_{GND}$, 40 V (< 50 ns) max.
(3) The specification value indicates “AC voltage” is $V_{BOOT}$ to $V_{PHASE}$, 8 V (< 20 ns) max.

## RECOMMENDED OPERATING RANGE

| ELECTRICAL PARAMETER | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|
| Input voltage ($V_{IN}$) | 2.7 | - | 24 | V |
| Drive supply voltage ($V_{DRV}$) | 4.5 | 5 | 5.5 | |
| Control logic supply voltage ($V_{CIN}$) | 4.5 | 5 | 5.5 | |
| BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage) | 4 | 4.5 | 5.5 | |
| Thermal resistance from junction to ambient | - | 10.6 | - | °C/W |
| Thermal resistance from junction to case | - | 1.6 | - | |


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## ELECTRICAL SPECIFICATIONS

(DSBL# = ZCD_EN# = 5 V, $V_{IN}$ = 12 V, $V_{DRV}$ and $V_{CIN}$ = 5 V, $T_A$ = 25 °C)

| PARAMETER | SYMBOL | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| **POWER SUPPLY** | | | | | | |
| Control logic supply current | $I_{VCIN}$ | $V_{DSBL\#}$ = 0 V, no switching, $V_{PWM}$ = FLOAT | - | 5 | - | µA |
| | | $V_{DSBL\#}$ = 5 V, no switching, $V_{PWM}$ = FLOAT | - | 300 | - | |
| | | $V_{DSBL\#}$ = 5 V, $f_S$ = 300 kHz, D = 0.1 | - | 350 | - | |
| Drive supply current | $I_{VDRV}$ | $f_S$ = 300 kHz, D = 0.1 | - | 9 | 14 | mA |
| | | $f_S$ = 1 MHz, D = 0.1 | - | 30 | - | |
| | | $V_{DSBL\#}$ = 0 V, no switching | - | 15 | - | µA |
| | | $V_{DSBL\#}$ = 5 V, no switching | - | 55 | - | |
| **BOOTSTRAP SUPPLY** | | | | | | |
| Bootstrap diode forward voltage | $V_F$ | $I_F$ = 2 mA | | | 0.4 | V |
| **PWM CONTROL INPUT (SiC639)** | | | | | | |
| Rising threshold | $V_{TH_PWM_R}$ | | - | - | 4.2 | V |
| Falling threshold | $V_{TH_PWM_F}$ | | 0.72 | - | - | |
| Tri-state voltage | $V_{TRI_FLOAT}$ | $V_{PWM}$ = FLOAT | - | 2.3 | - | |
| Tri-state window | $V_{TRI_WINDOW}$ | | 1.38 | - | 3 | |
| Tri-state rising threshold hysteresis | $V_{HYS_TRI_R}$ | | - | 225 | - | mV |
| Tri-state falling threshold hysteresis | $V_{HYS_TRI_F}$ | | - | 325 | - | |
| PWM input current | $I_{PWM}$ | $V_{PWM}$ = 5 V, DSBL# = high | - | - | 350 | µA |
| | | $V_{PWM}$ = 5 V, DSBL# = low | - | - | 1 | |
| | | $V_{PWM}$ = 0 V, DSBL# = high | - | - | -350 | |
| | | $V_{PWM}$ = 0 V, DSBL# = low | - | - | -1 | |
| **PWM CONTROL INPUT (SiC639A)** | | | | | | |
| Rising threshold | $V_{TH_PWM_R}$ | | - | - | 2.7 | V |
| Falling threshold | $V_{TH_PWM_F}$ | | 0.72 | - | - | |
| Tri-state voltage | $V_{TRI_FLOT}$ | $V_{PWM}$ = FLOAT | - | 1.8 | - | |
| Tri-state window | $V_{TRI_WINDOW}$ | | 1.38 | - | 1.95 | |
| Tri-state rising threshold hysteresis | $V_{HYS_TRI_R}$ | | - | 250 | - | mV |
| Tri-state falling threshold hysteresis | $V_{HYS_TRI_F}$ | | - | 300 | - | |
| PWM input current | $I_{PWM}$ | $V_{PWM}$ = 3.3 V, DSBL# = high | - | - | 225 | µA |
| | | $V_{PWM}$ = 3.3 V, DSBL# = low | - | - | 1 | |
| | | $V_{PWM}$ = 0 V, DSBL# = high | - | - | -225 | |
| | | $V_{PWM}$ = 0 V, DSBL# = low | - | - | -1 | |
| **TIMING SPECIFICATIONS** | | | | | | |
| Tri-state to GH/GL rising propagation delay | $t_{PD_TRI_R}$ | No load, see Fig. 4 | - | 30 | - | ns |
| Tri-state GH hold-off time | $t_{TSHO_GH}$ | | - | 35 | - | |
| Tri-state GL hold-off time | $t_{TSHO_GL}$ | | - | 130 | - | |
| GH - turn off propagation delay | $t_{PD_OFF_GH}$ | | - | 15 | - | |
| GH - turn on propagation delay (dead time rising) | $t_{PD_ON_GH}$ | | - | 10 | - | |
| GL - turn off propagation delay | $t_{PD_OFF_GL}$ | | - | 13 | - | |
| GL - turn on propagation delay (dead time falling) | $t_{PD_ON_GL}$ | | - | 10 | - | |
| DSBL# Lo to GH/GL falling propagation delay | $t_{PD_DSBL\#_F}$ | Fig. 5 | - | 15 | - | |
| PWM minimum on-time | $t_{PWM_ON_MIN}$ | | 30 | - | - | |


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## ELECTRICAL SPECIFICATIONS

(DSBL# = ZCD_EN# = 5 V, $V_{IN}$ = 12 V, $V_{DRV}$ and $V_{CIN}$ = 5 V, $T_A$ = 25 °C)

| PARAMETER | SYMBOL | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | |
| **DSBL# ZCD_EN# INPUT** | | | | | | |
| DSBL# logic input voltage | $V_{IH_DSBL\#}$ | Input logic high | 2 | - | - | V |
| | $V_{IL_DSBL\#}$ | Input logic low | - | - | 0.8 | |
| ZCD_EN# logic input voltage | $V_{IH_ZCD_EN\#}$ | Input logic high | 2 | - | - | |
| | $V_{IL_ZCD_EN\#}$ | Input logic low | - | - | 0.8 | |
| **PROTECTION** | | | | | | |
| Under voltage lockout | $V_{UVLO}$ | $V_{CIN}$ rising, on threshold | - | 3.7 | 4.1 | V |
| | | $V_{CIN}$ falling, off threshold | 2.7 | 3.1 | - | |
| Under voltage lockout hysteresis | $V_{UVLO_HYST}$ | | - | 575 | - | mV |
| THWn flag set (2) | $T_{THWn_SET}$ | | - | 160 | - | °C |
| THWn flag clear (2) | $T_{THWn_CLEAR}$ | | - | 135 | - | |
| THWn flag hysteresis (2) | $T_{THWn_HYST}$ | | - | 25 | - | |
| THWn output low | $V_{OL_THWn}$ | $I_{THWn}$ = 2 mA | - | 0.02 | - | V |

**Notes**

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design

## DETAILED OPERATIONAL DESCRIPTION

### PWM Input with Tri-State Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM_TH_R}$ the low side is turned off and the high side is turned on. When PWM input is driven below $V_{PWM_TH_F}$ the high side is turned off and the low side is turned on. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC639 and SiC639A to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, Fig. 4). If the PWM input stays in this region for the tri-state hold-off period, tTSHO, both high side and low side MOSFETs are turned off. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering.

### Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low side MOSFETs. WhenDSBL# is low, the PWM resistor divider is also disconnected. In this state, standby current is minimized. If DSBL# is left unconnected, an internal pull-down resistor will pull the pin to $C_{GND}$ and shut down the IC.

### Diode Emulation Mode (ZCD_EN#)

When ZCD_EN# pin is driven below $V_{IL_ZCD_EN\#}$ diode emulation mode is enabled. If the PWM input is wi thin the tri-state window for longer than the tri-state hold off time, then the low side MOSFET is under control of the ZCD (zero crossing detect) comparator. In this mode, the LS MOSFET is turned off if the inductor current is < or = 0. Light load efficiency is improved by avoiding discharge of output capacitors. If ZCD_EN# is high, diode emulation mode is disabled. In this mode if PWM enters tri-state, the device will go into tri-state mode after tri-state delay and both the high side and low side MOSFETs will be turned off.

### Thermal Shutdown Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect with a maximum of 20 kΩ, to $V_{CIN}$. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC639 and SiC639A do not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

### Voltage Input ($V_{IN}$)

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.


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### Switch Node ($V_{SWH}$ and PHASE)

The switch node, $V_{SWH}$, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node $V_{SWH}$. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH (the high side gate) and PHASE to provide a discharge path for the HS MOSFET in the event that $V_{CIN}$ goes to zero while $V_{IN}$ is still applied.

### Ground Connections ($C_{GND}$ and $P_{GND}$)

$P_{GND}$ (power ground) should be externally connected to $C_{GND}$ (signal ground). The layout of the printed circuit board should be such that the inductance separating $C_{GND}$ and $P_{GND}$ is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V

### Control and Drive Supply Voltage Input ($V_{DRV}$, $V_{CIN}$)

$V_{CIN}$ is the bias supply for the gate drive control IC. $V_{DRV}$ is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

### Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

### Shoot-Through Protection and Adaptive Dead Time

The SiC639 and SiC639A have an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high side and low side MOSFETs are not turned on at the same time. The adaptive dead time control operates as follows. The high side and low side gate voltages are monitored to prevent the MOSFET turning on from tuning on until the other MOSFET's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOSFET is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

### Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high side and low side MOSFET gates low until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC639, SiC639A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH (the high side gate) and PHASE to provide a discharge path for the HS MOSFET.

## FUNCTIONAL BLOCK DIAGRAM

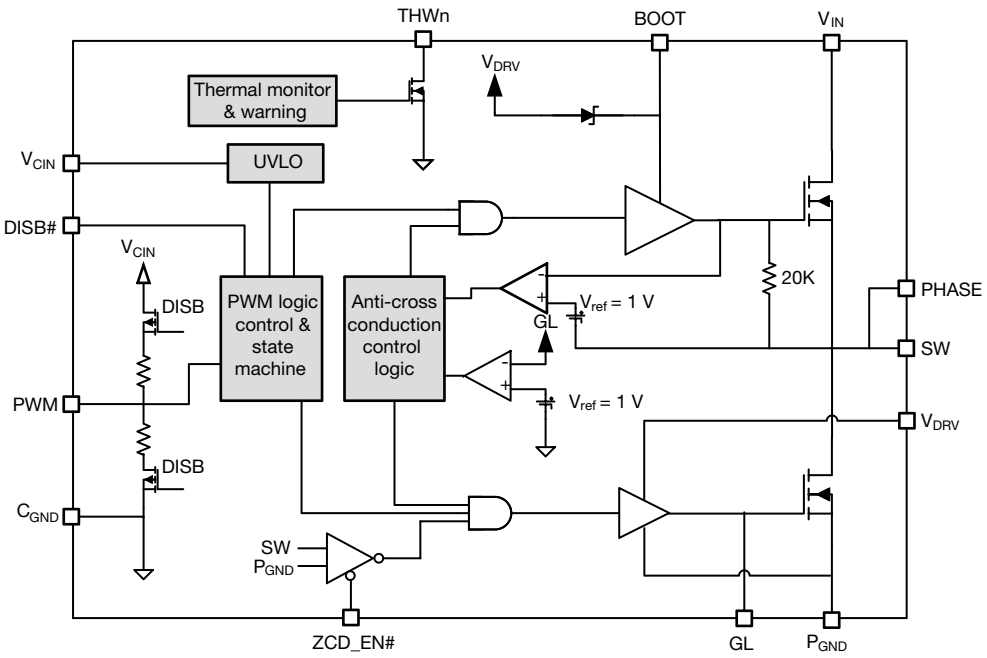



**Fig. 3 - SiC639 Functional Block Diagram**


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| DEVICE TRUTH TABLE | | | | |
|---|---|---|---|---|
| DSBL# | ZCD_EN# | PWM | GH | GL |
| H | L | H | H | L |
| H | L | H to mid | L | H, $I_L$ > 0 A<br>L, $I_L$ < 0 A |
| H | L | L to mid | L | L |
| H | L | L | L | H |
| L | X | X | L | L |
| H | H | L | L | H |
| H | H | H | H | L |
| H | H | mid | L | L |

## PWM TIMING DIAGRAM

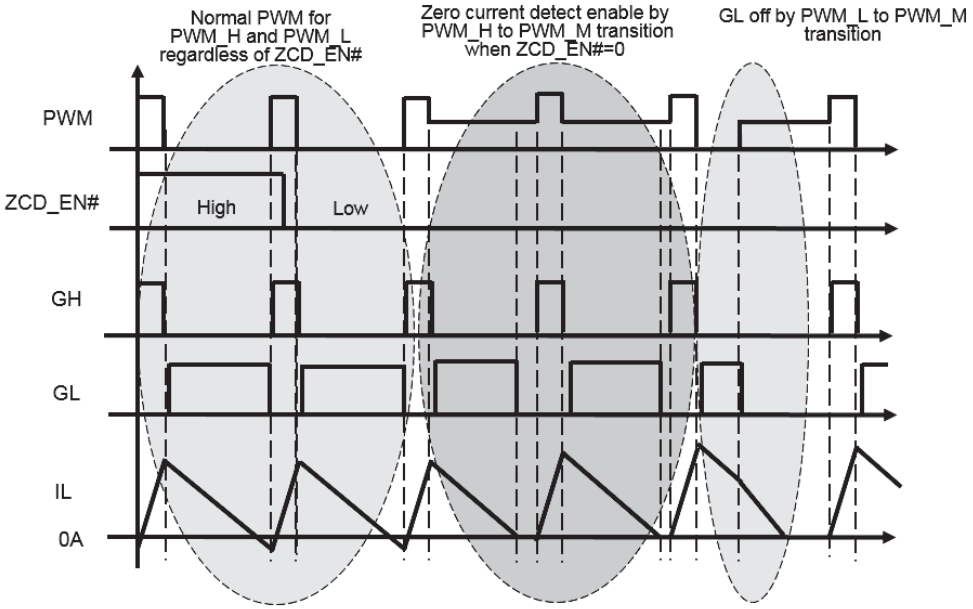



**Fig. 4 - Timing Diagram**

## DSBL# PROPAGATION DELAY

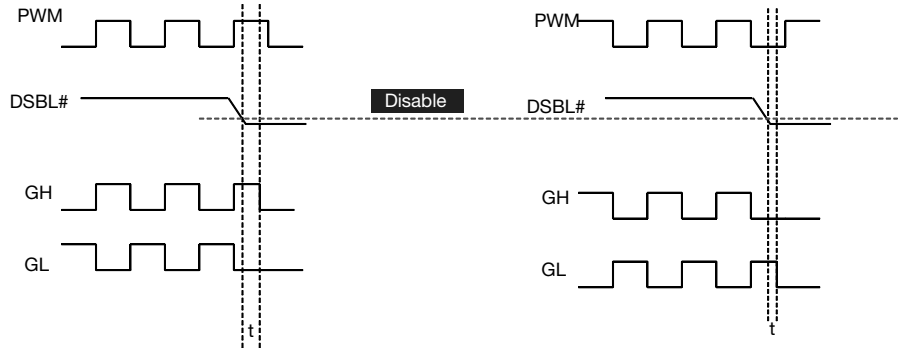



**Fig. 5 - DSBL# Falling Propagation Delay**


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## ELECTRICAL CHARACTERISTICS

Test condition: $V_{IN}$ = 13 V, DSBL# = $V_{DRV}$ = $V_{CIN}$ = 5 V, ZCD_EN# = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH (DCR = 0.32 mΩ), $T_A$ = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC639 and SiC639A losses only unless otherwise stated)

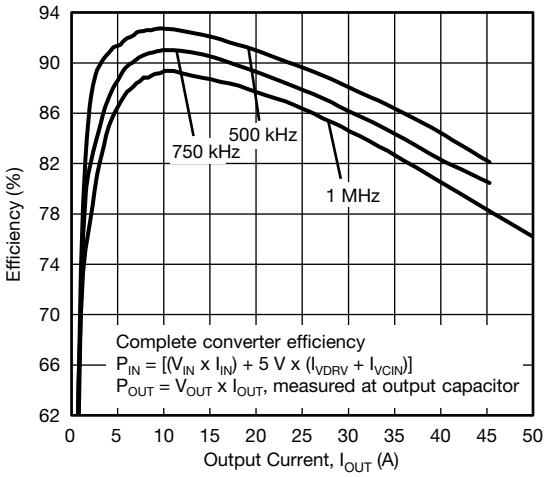



**Fig. 6 - Efficiency vs. Output Current ($V_{IN}$ = 12.6 V)**

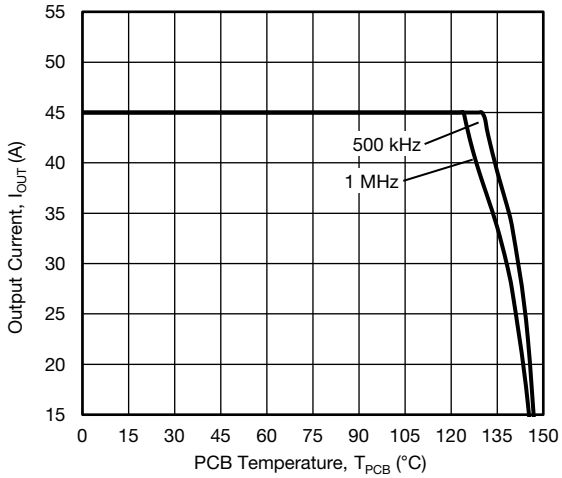



**Fig. 9 - Safe Operating Area**

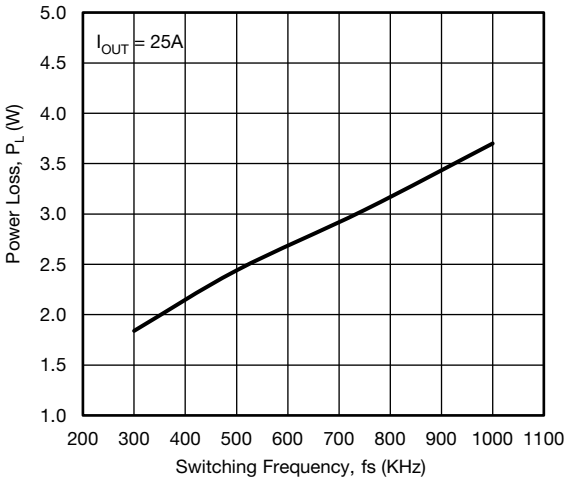



**Fig. 7 - Power Loss vs. Switching Frequency ($V_{IN}$ = 12.6 V)**

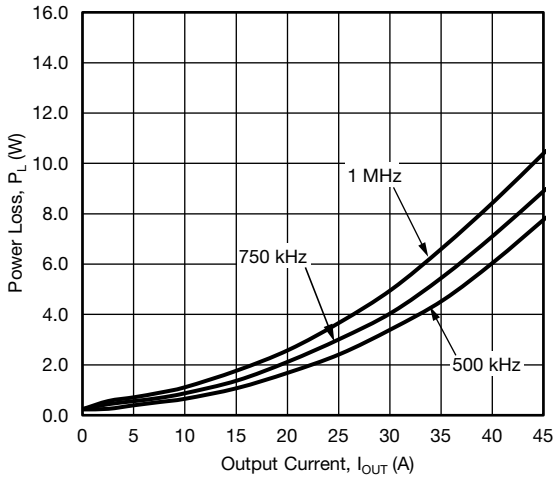



**Fig. 10 - Power Loss vs. Output Current ($V_{IN}$ = 12.6 V)**

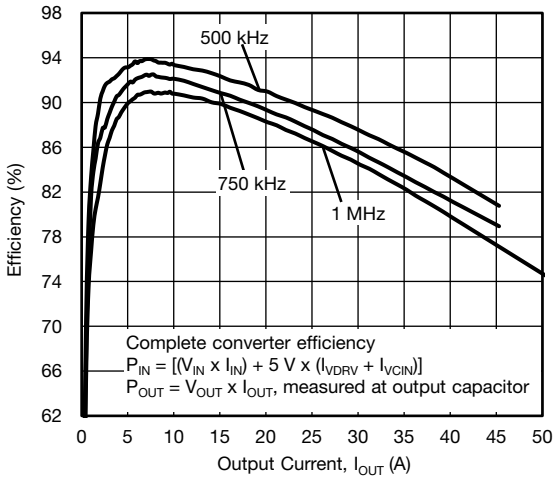



**Fig. 8 - Efficiency vs. Output Current ($V_{IN}$ = 9 V)**

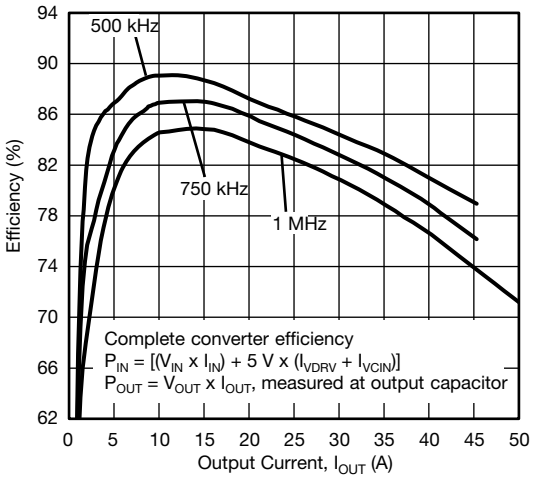



**Fig. 11 - Efficiency vs. Output Current ($V_{IN}$ = 19 V)**


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## ELECTRICAL CHARACTERISTICS

Test condition: $V_{IN}$ = 13 V, DSBL# = $V_{DRV}$ = $V_{CIN}$ = 5 V, ZCD_EN# = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH (DCR = 0.32 mΩ), $T_A$ = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC639 and SiC639A losses only unless otherwise stated)

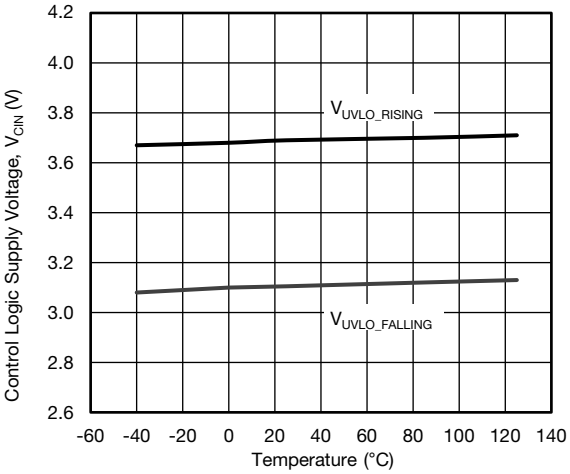



**Fig. 12 - UVLO Threshold vs. Temperature**

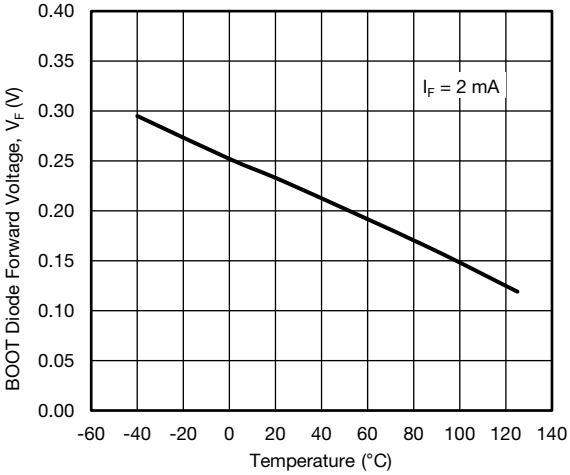



**Fig. 15 - Boot Diode Forward Voltage vs. Temperature**

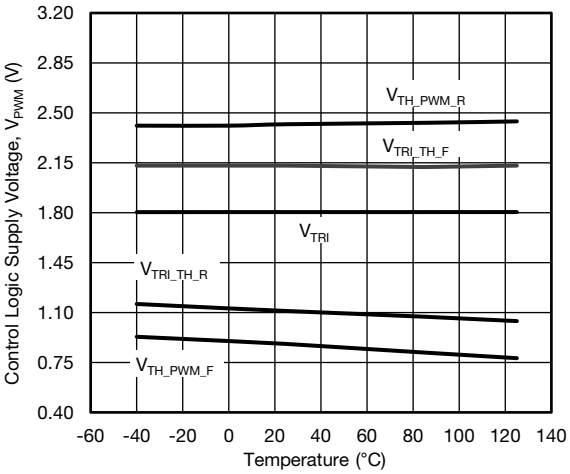



**Fig. 13 - PWM Threshold vs. Temperature (SiC639A)**

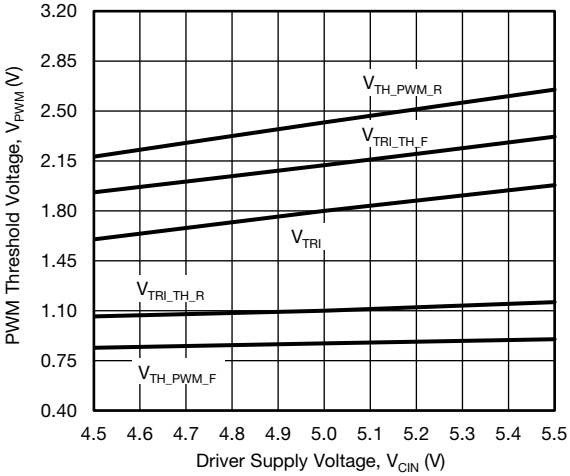



**Fig. 16 - PWM Threshold vs. Driver Supply Voltage (SiC639A)**

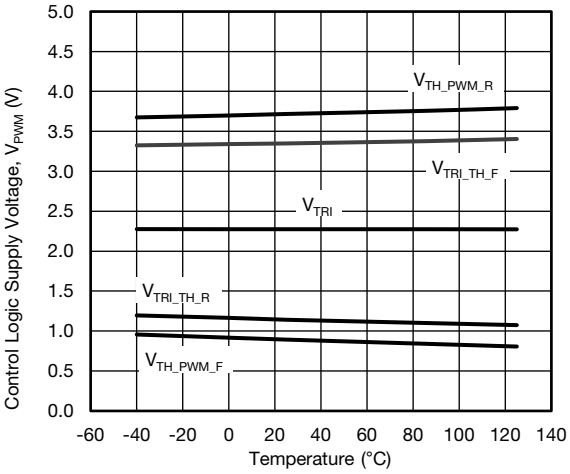



**Fig. 14 - PWM Threshold vs. Temperature (SiC639)**

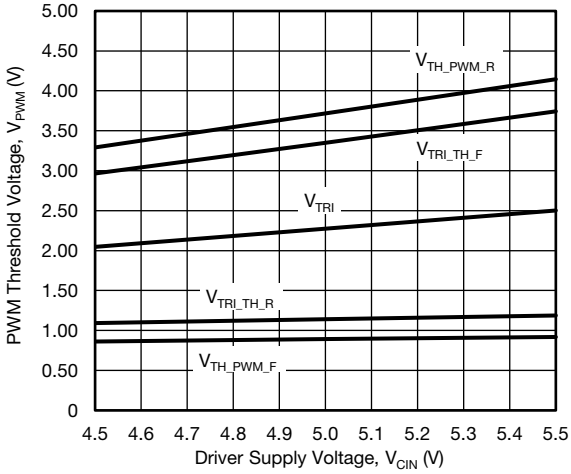



**Fig. 17 - PWM Threshold vs. Driver Supply Voltage (SiC639)**


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## ELECTRICAL CHARACTERISTICS

Test condition: $V_{IN}$ = 13 V, DSBL# = $V_{DRV}$ = $V_{CIN}$ = 5 V, ZCD_EN# = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH (DCR = 0.32 mΩ), $T_A$ = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC639 and SiC639A losses only unless otherwise stated)

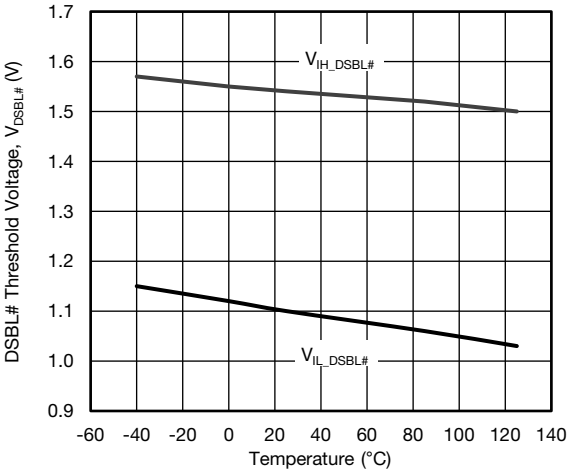



**Fig. 18 - DSBL# Threshold vs. Temperature**

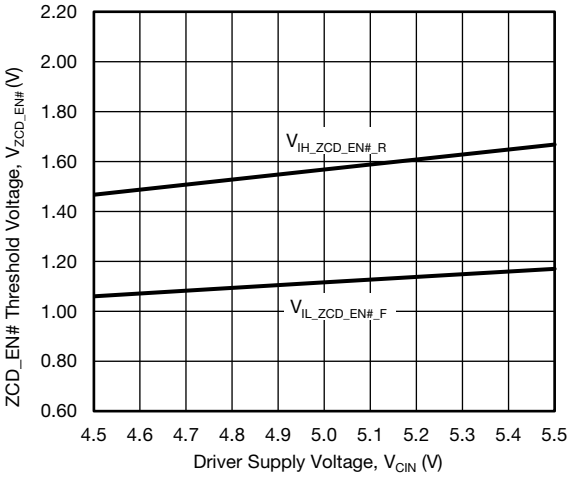



**Fig. 21 - ZCD_EN# Threshold vs. Driver Supply Voltage**

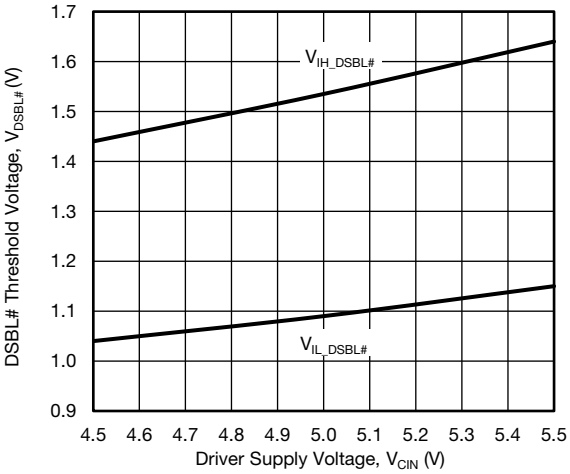



**Fig. 19 - DSBL# vs. Driver Input Voltage**

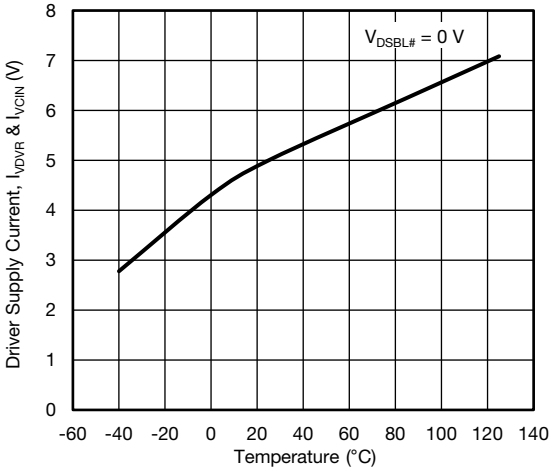



**Fig. 22 - Driver Shutdown Current vs. Temperature**

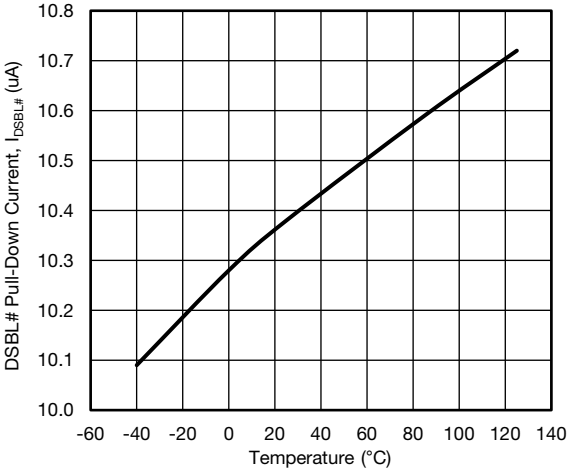



**Fig. 20 - DSBL# Pull-Down Current vs. Temperature**

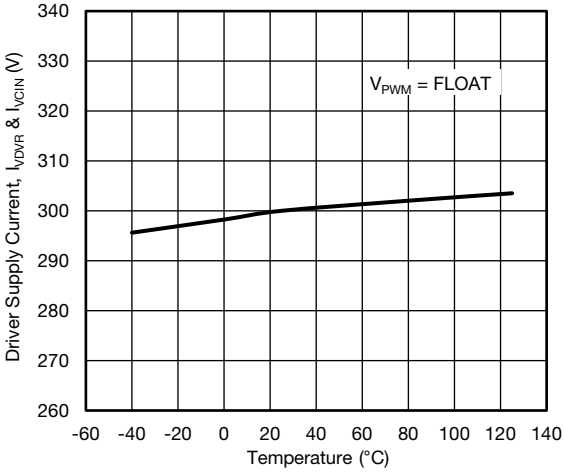
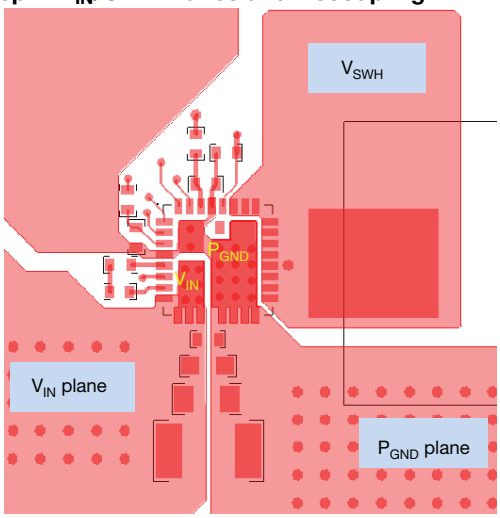



**Fig. 23 - Driver Supply Current vs. Temperature**


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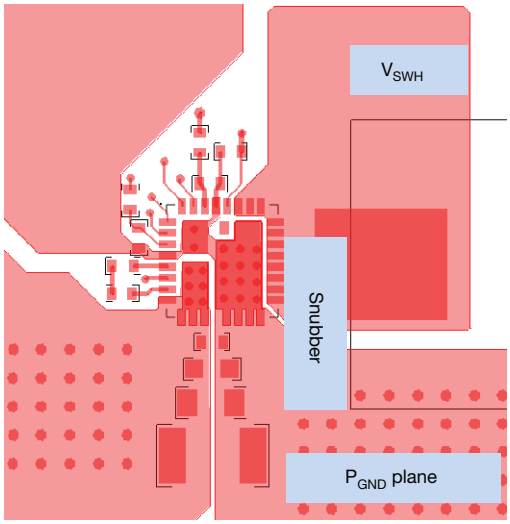
## PCB LAYOUT RECOMMENDATIONS

### Step 1: $V_{IN}$/GND Planes and Decoupling



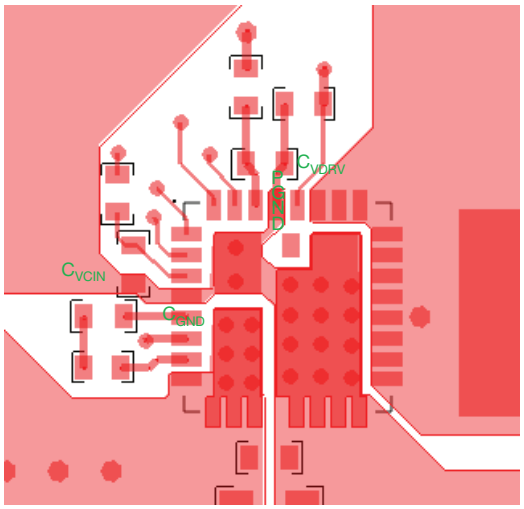

1. Layout $V_{IN}$ and $P_{GND}$ planes as shown above
2. Ceramic capacitors should be placed right between $V_{IN}$ and $P_{GND}$, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, and 0402
4. Smaller capacitance value, closer to device $V_{IN}$ pin(s) - better high frequency noise absorbing

### Step 2: $V_{SWH}$ Plane



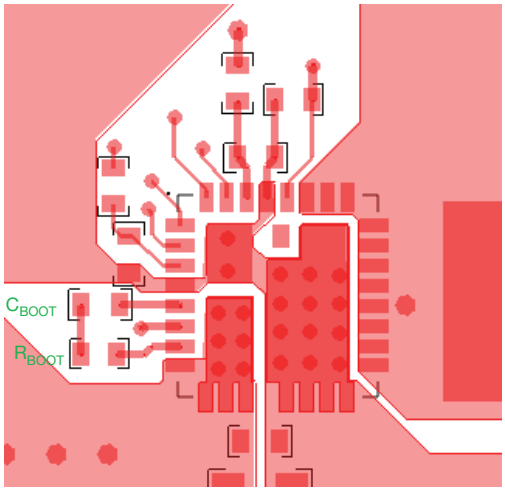

1. Connect output inductor to DrMOS with large plane to lower the resistance
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

### Step 3: $V_{CIN}$/$V_{DRV}$ Input Filter




1. The $V_{CIN}$/$V_{DRV}$ input filter ceramic cap should be placed very close to IC. It is recommended to connect two caps separately
2. $C_{VCIN}$ cap should be placed between pin 3 and pin 4 ($C_{GND}$ of driver IC) to achieve best noise filtering
3. $C_{VDRV}$ cap should be placed between pin 28 ($P_{GND}$ of driver IC) and pin 29 to provide maximum instantaneous driver current for low side MOSFET during switching cycle
4. For connecting $C_{VCIN}$ analog ground, it is recommended to use large plane to reduce parasitic inductance

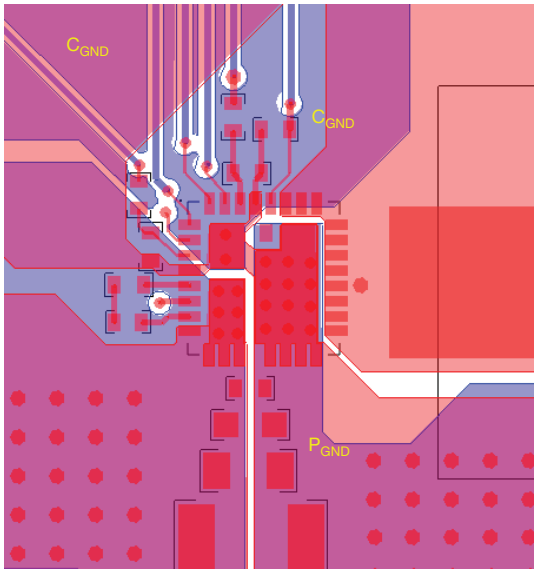
### Step 4: BOOT Resistor and Capacitor Placement




1. These components need to be placed very close to IC, right between PHASE (pin 7) and BOOT (pin 5)
2. To reduce parasitic inductance, chip size 0402 can be used

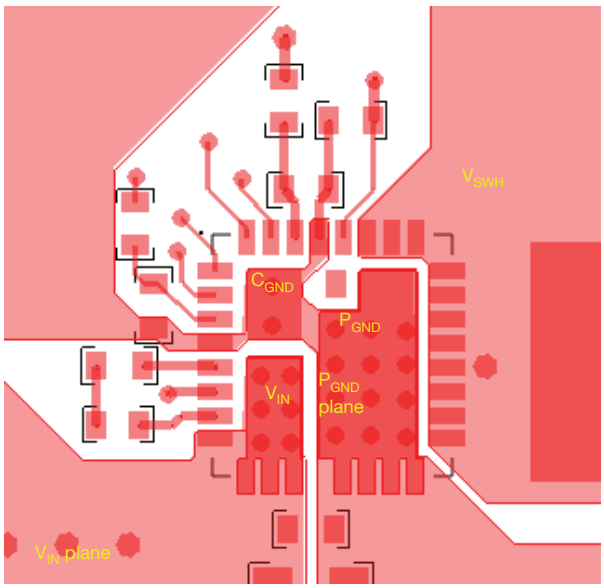

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### Step 5: Signal Routing



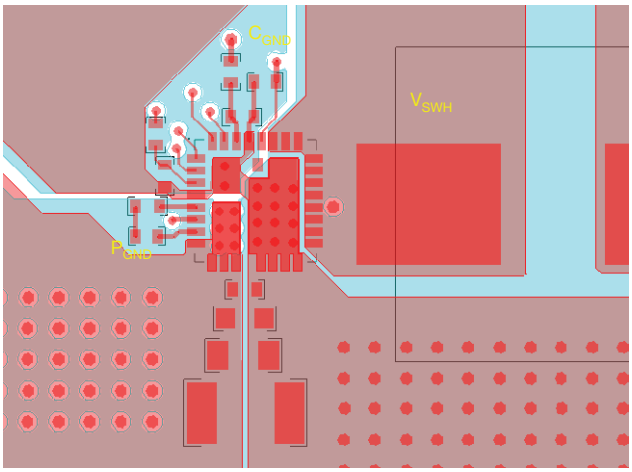

1. Route the PWM / ZCD_EN# / DSBL# / THWn signal traces out of the top left corner next DrMOS pin 1
2. PWM signal is very important signal, both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer
3. It is best to “shield” traces form power switching nodes, e.g. $V_{SWH}$, to improve signal integrity
4. GL (pin 27) has been connected with GL pad internally and does not need to connect externally

### Step 6: Adding Thermal Relief Vias




1. Thermal relief vias can be added on the $V_{IN}$ and $P_{GND}$ pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional vias can be put on $V_{IN}$ plane and $P_{GND}$ plane.
3. $V_{SWH}$ pad is a noise source and not recommended to put vias on this plane
4. 8 mil drill for pads and 10 mils drill for plane can be the optional via size. Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

### Step 7: Ground Connection




1. It is recommended to make single connection between $C_{GND}$ and $P_{GND}$ and this connection can be done on top layer
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into $C_{GND}$ and $P_{GND}$ plane
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer


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### Multi-Phases VRPower PCB Layout

Following is an example for 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling caps next to them. The inductors are placed as close as possible to the SiC639 and SiC639A to minimize the PCB copper loss. Vias are applied on all PADs ($V_{IN}$, $P_{GND}$, $C_{GND}$) of the SiC639 and SiC639A to ensure that both electrical and thermal performance are excellent. Large copper planes are used for all the high current loops, such as $V_{IN}$, $V_{SWH}$, $V_{OUT}$ and $P_{GND}$. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC639 and SiC639A to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

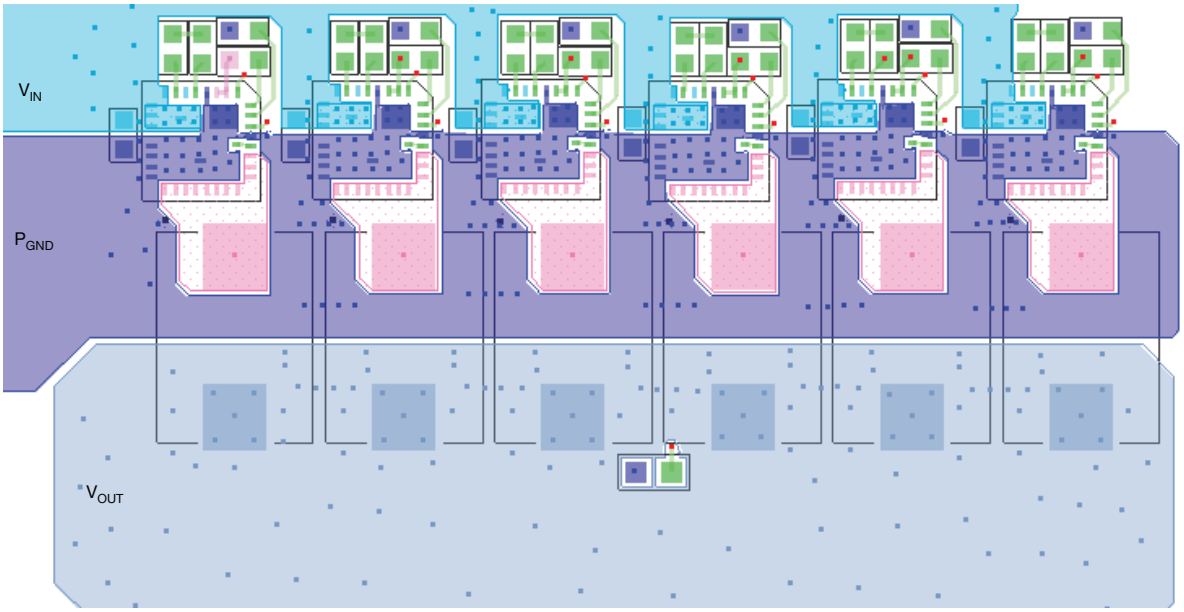



**Fig. 24 - Multi-Phase VRPower Layout Top View**

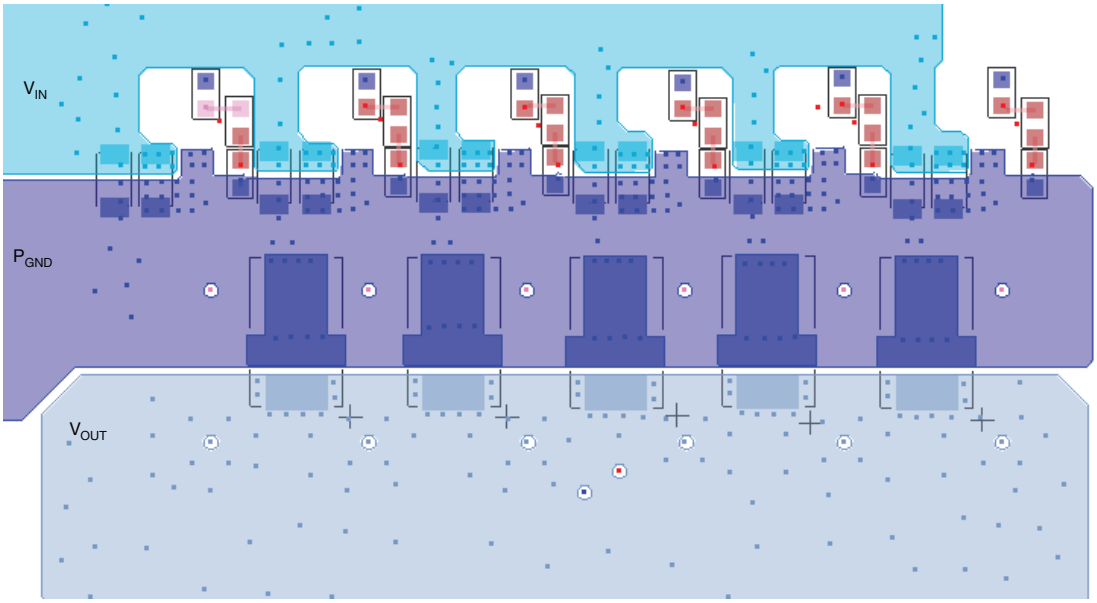



**Fig. 25 - Multi-Phase VRPower Layout Bottom View**


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| PRODUCT SUMMARY | | |
|---|---|---|
| Part number | SiC639 | SiC639A |
| Description | 50 A power stage, 2.7 $V_{IN}$ to 24 $V_{IN}$, 5 V PWM with ZCD mode | 50 A power stage, 2.7 $V_{IN}$ to 24 $V_{IN}$, 3.3 V PWM with ZCD mode |
| Input voltage min. (V) | 2.7 | 2.7 |
| Input voltage max. (V) | 24 | 24 |
| Continuous current rating max. (A) | 50 | 50 |
| Switch frequency max. (kHz) | 1500 | 1500 |
| Enable (yes / no) | Yes | Yes |
| Monitoring features | - | - |
| Protection | UVLO, THDN | UVLO, THDN |
| Light load mode | ZCD | ZCD |
| Pulse-width modulation (V) | 5 | 3.3 |
| Package type | PowerPAK MLP55-31L | PowerPAK MLP55-31L |
| Package size (W, L, H) (mm) | 5.0 x 5.0 x 0.75 | 5.0 x 5.0 x 0.75 |
| Status code | 2 | 2 |
| Product type | VRPower (DrMOS) | VRPower (DrMOS) |
| Applications | Computer, industrial, networking | Computer, industrial, networking |

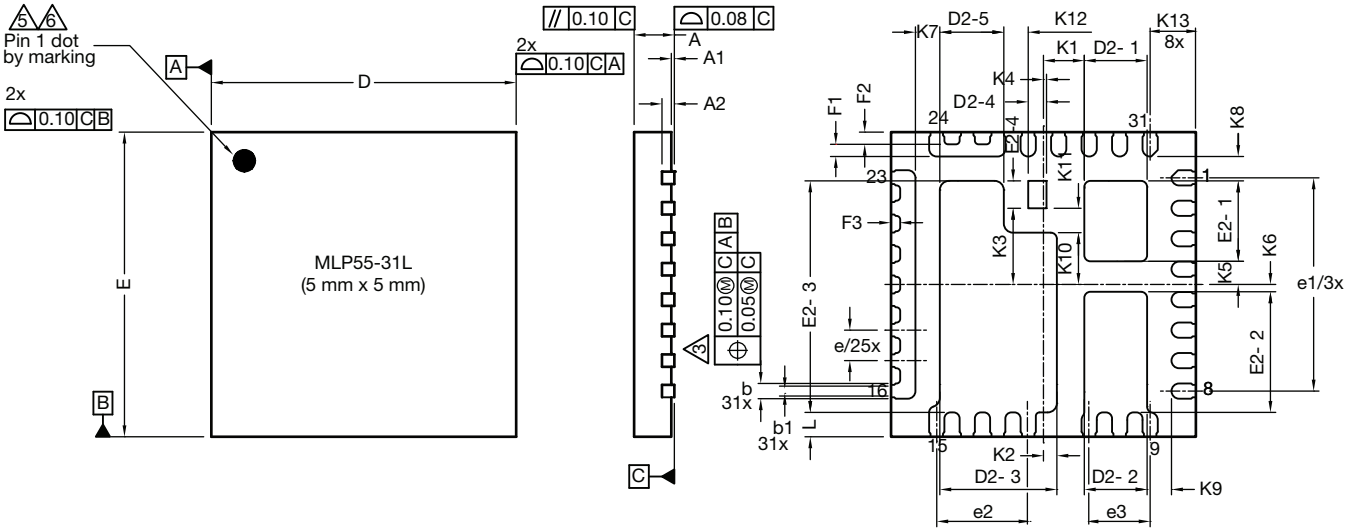
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# PowerPAK® MLP55-31L Case Outline




| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.027 | 0.029 | 0.031 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| A2 | | 0.20 ref. | | | 0.008 ref. | |
| b | 0.20 | 0.25 | 0.30 | 0.078 | 0.098 | 0.011 |
| b1 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.196 | 0.200 |
| e | | 0.50 BSC | | | 0.019 BSC | |
| e1 | | 3.50 BSC | | | 0.138 BSC | |
| e2 | | 1.50 BSC | | | 0.060 BSC | |
| e3 | | 1.00 BSC | | | 0.040 BSC | |
| E | 4.90 | 5.00 | 5.10 | 0.193 | 0.196 | 0.200 |
| L | 0.35 | 0.40 | 0.45 | 0.013 | 0.015 | 0.017 |
| D2-1 | 0.98 | 1.03 | 1.08 | 0.039 | 0.041 | 0.043 |
| D2-2 | 0.98 | 1.03 | 1.08 | 0.039 | 0.041 | 0.043 |
| D2-3 | 1.87 | 1.92 | 1.97 | 0.074 | 0.076 | 0.078 |
| D2-4 | | 0.30 BSC | | | 0.012 BSC | |
| D2-5 | 1.05 | 1.10 | 1.15 | 0.041 | 0.043 | 0.045 |
| E2-1 | 1.27 | 1.32 | 1.37 | 0.050 | 0.052 | 0.054 |
| E2-2 | 1.93 | 1.98 | 2.03 | 0.076 | 0.078 | 0.080 |
| E2-3 | 3.75 | 3.80 | 3.85 | 0.148 | 0.150 | 0.152 |
| E2-4 | | 0.45 BSC | | | 0.018 BSC | |
| F1 | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| F2 | | 0.20 ref. | | | 0.008 ref. | |
| F3 | | 0.15 ref. | | | 0.006 ref. | |



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| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| K1 | | 0.67 BSC | | | 0.026 BSC | |
| K2 | | 0.22 BSC | | | 0.008 BSC | |
| K3 | | 1.25 BSC | | | 0.049 BSC | |
| K4 | | 0.10 BSC | | | 0.004 BSC | |
| K5 | | 0.38 BSC | | | 0.015 BSC | |
| K6 | | 0.12 BSC | | | 0.005 BSC | |
| K7 | | 0.40 BSC | | | 0.016 BSC | |
| K8 | | 0.40 BSC | | | 0.016 BSC | |
| K9 | | 0.40 BSC | | | 0.016 BSC | |
| K10 | | 0.85 BSC | | | 0.033 BSC | |
| K11 | | 0.40 BSC | | | 0.016 BSC | |
| K12 | | 0.40 BSC | | | 0.016 BSC | |
| K13 | | 0.75 BSC | | | 0.030 BSC | |
| ECN: T17-0423-Rev. F, 21-Aug-17<br>DWG: 6025 | | | | | | |

**Notes**

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
4. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
5. Exact shape and size of this feature is optional
6. Package warpage max. 0.08 mm
7. Applied only for terminals

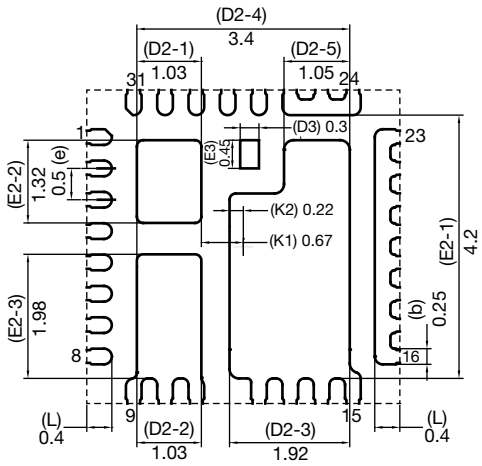


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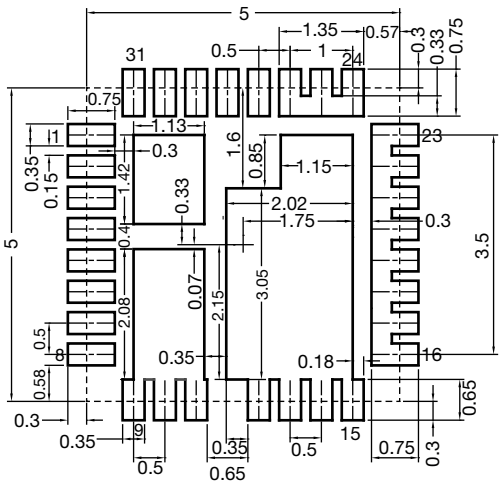
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# Recommended Land Pattern
# PowerPAK® MLP55-31L

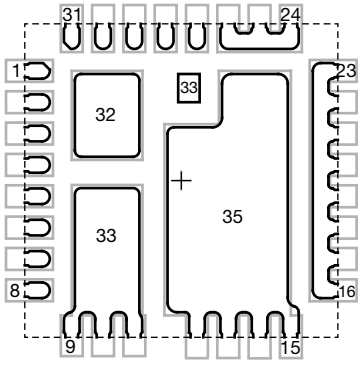
Top side transparent view
(not bottom view)




Land pattern for MLP55-31L




All dimensions in millimeters




Component for MLP55-31L

Land pattern for MLP55-31L



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