# 50 A VRPower® Integrated Power Stage

## DESCRIPTION

The SiC788 and SiC788A are integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 6 mm x 6 mm MLP package, SiC788 and SiC788A enable voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilize Vishay's state-of-the-art Gen IV TrenchFET® technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC788 and SiC788A incorporate an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, a thermal warning (THWn) that alerts the system of excessive junction temperature, and skip mode (SMOD#) to improve light load efficiency. The drivers are also compatible with a wide range of PWM controllers and supports tri-state PWM, 3.3 V (SiC788A) and5 V (SiC788) PWM logic.

## FEATURES

- Thermally enhanced PowerPAK® MLP66-40L package
- Vishay's Gen IV MOSFET technology and a low-side MOSFET with integrated Schottky diode
- Delivers up to 50 A continuous current
- 95 % peak efficiency
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 12 V input stage
- 3.3 V (SiC788A) and 5 V (SiC788) PWM logic with tri-state and hold-off
- SMOD# logic for light load efficiency improvement
- Low PWM propagation delay (< 20 ns)
- Thermal monitor flag
- Faster enable / disable
- Under voltage lockout for $V_{CIN}$
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT HALOGEN FREE

## APPLICATIONS

- Multi-phase VRDs for CPU, GPU, and memory

## TYPICAL APPLICATION DIAGRAM

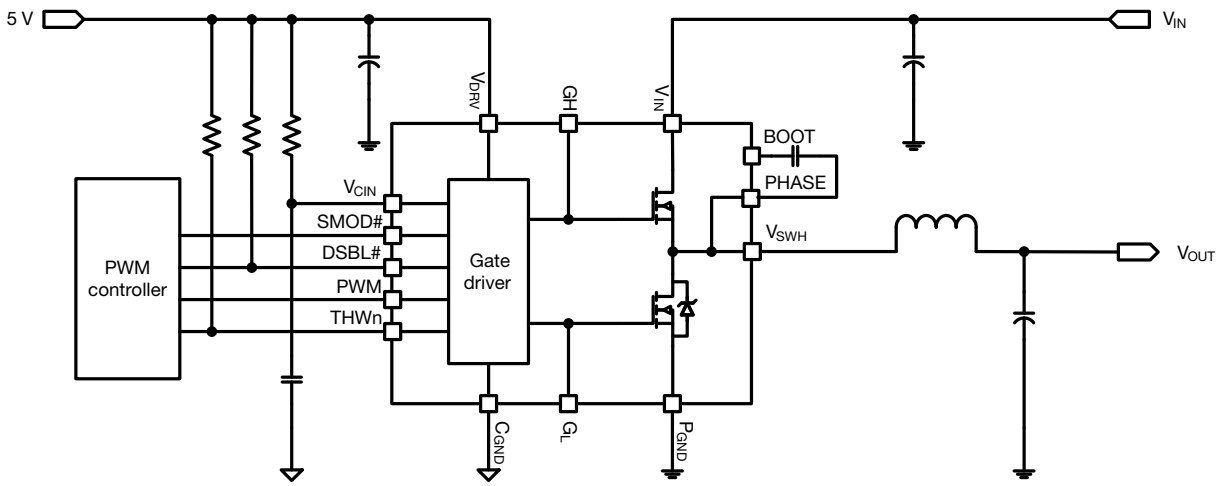



**Fig. 1 - SiC788 and SiC788A Typical Application Diagram**



For technical questions, contact: powerictechsupport@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

## PINOUT CONFIGURATION

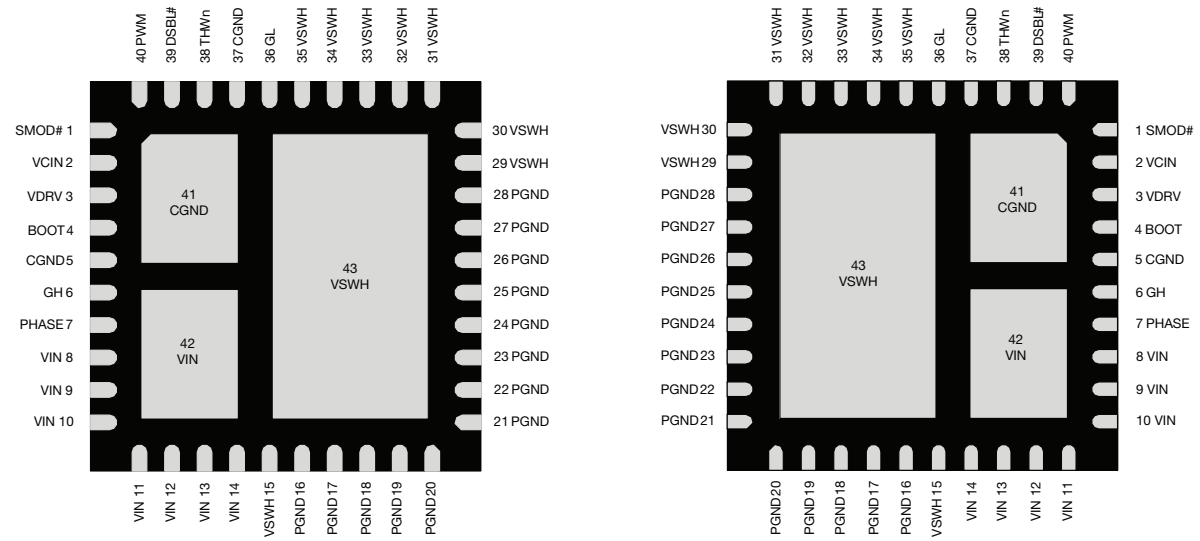



**Fig. 2 - SiC788 and SiC788A Pin Configuration**

| PIN DESCRIPTION | | |
|---|---|---|
| **PIN NUMBER** | **NAME** | **FUNCTION** |
| 1 | SMOD# | Low-side gate turn-off logic. Active low |
| 2 | $V_{CIN}$ | Supply voltage for internal logic circuitry |
| 3 | $V_{DRV}$ | Supply voltage for internal gate driver |
| 4 | BOOT | High-side driver bootstrap voltage |
| 5, 37, 41 | $C_{GND}$ | Analog ground for the driver IC |
| 6 | GH | High-side gate signal |
| 7 | PHASE | Return path of high-side gate driver |
| 8 to 14, 42 | $V_{IN}$ | Power stage input voltage. Drain of high side MOSFET |
| 15, 29 to 35, 43 | $V_{SWH}$ | Switch node of the power stage |
| 16 to 28 | $P_{GND}$ | Power ground |
| 36 | GL | Low-side gate signal |
| 38 | THWn | Thermal warning open drain output |
| 39 | DSBL# | Disable pin. Active low |
| 40 | PWM | PWM control input |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **PART NUMBER** | **PACKAGE** | **MARKING CODE** | **OPTION** |
| SiC788ACD-T1-GE3 | PowerPAK® MLP66-40L | SiC788A | 3.3 V PWM optimized |
| SiC788CD-T1-GE3 | | SiC788 | 5 V PWM optimized |
| SiC788ADB and SiC788DB | Reference board | | |



For technical questions, contact: powerictechsupport@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|---|---|
| **ELECTRICAL PARAMETER** | **CONDITIONS** | **LIMIT** | **UNIT** |
| Input voltage | $V_{IN}$ | -0.3 to +25 | V |
| Control logic supply voltage | $V_{CIN}$ | -0.3 to +7 | |
| Drive supply voltage | $V_{DRV}$ | -0.3 to +7 | |
| Switch node (DC voltage) | $V_{SWH}$ | -0.3 to +25 | |
| Switch node (AC voltage) (1) | | -8 to +30 | |
| BOOT voltage (DC voltage) | $V_{BOOT}$ | 32 | |
| BOOT voltage (AC voltage) (2) | | 38 | |
| BOOT to PHASE (DC voltage) | $V_{BOOT- PHASE}$ | -0.3 to +7 | |
| BOOT to PHASE (AC voltage) (3) | | -0.3 to +8 | |
| All logic inputs and outputs (PWM, DSBL#, and THWn) | | -0.3 to $V_{CIN}$ + 0.3 | |
| Output current, $I_{OUT(AV)}$ (4) | $f_S$ = 300 kHz, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.8 V | 50 | A |
| | $f_S$ = 1 MHz, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.8 V | 40 | |
| Max. operating junction temperature | $T_J$ | 150 | °C |
| Ambient temperature | $T_A$ | -40 to +125 | |
| Storage temperature | $T_{stg}$ | -65 to +150 | |
| Electrostatic discharge protection | Human body model, JESD22-A114 | 5000 | V |
| | Charged device model, JESD22-C101 | 1000 | |

**Notes**

(1) The specification values indicated "AC" is $V_{SWH}$ to $P_{GND}$, -8 V (< 20 ns, 10 µJ), min. and 30 V (< 50 ns), max.

(2) The specification value indicates "AC voltage" is $V_{BOOT}$ to $P_{GND}$, 36 V (< 50 ns) max.

(3) The specification value indicates "AC voltage" is $V_{BOOT}$ to $V_{PHASE}$, 8 V (< 20 ns) max.

(4) Output current rated with testing evaluation board at $T_A$ = 25 °C with natural convection cooling. The rating is limited by the peak evaluation board temperature, $T_J$ = 150 °C, and varies depending on the operating conditions and PCB layout. This rating may be changed with different application settings

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

| RECOMMENDED OPERATING RANGE | | | | |
|---|---|---|---|---|
| **ELECTRICAL PARAMETER** | **MINIMUM** | **TYPICAL** | **MAXIMUM** | **UNIT** |
| Input voltage ($V_{IN}$) | 4.5 | - | 18 | V |
| Drive supply voltage ($V_{DRV}$) | 4.5 | 5 | 5.5 | |
| Control logic supply voltage ($V_{CIN}$) | 4.5 | 5 | 5.5 | |
| BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage) | 4 | 4.5 | 5.5 | |
| Thermal resistance from junction to PAD | - | 1 | - | °C/W |
| Thermal resistance from junction to case | - | 2.5 | - | |


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

## ELECTRICAL SPECIFICATIONS

(DSBL# = SMOD# = 5 V, $V_{IN}$ = 12 V, $V_{DRV}$ and $V_{CIN}$ = 5 V, $T_A$ = 25 °C)

| PARAMETER | SYMBOL | TEST CONDITION | LIMITS MIN. | LIMITS TYP. | LIMITS MAX. | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Control logic supply current | $I_{VCIN}$ | $V_{DSBL\#}$ = 0 V, no switching, $V_{PWM}$ = FLOAT | - | 85 | - | µA |
| | | $V_{DSBL\#}$ = 5 V, no switching, $V_{PWM}$ = FLOAT | - | 290 | - | |
| | | $V_{DSBL\#}$ = 5 V, $f_S$ = 300 kHz, D = 0.1 | - | 295 | - | |
| Drive supply current | $I_{VDRV}$ | $f_S$ = 300 kHz, D = 0.1 | - | 9 | 15 | mA |
| | | $f_S$ = 1 MHz, D = 0.1 | - | 30 | - | |
| | | $V_{DSBL\#}$ = 0 V, no switching | - | 30 | - | µA |
| | | $V_{DSBL\#}$ = 5 V, no switching | - | 55 | - | |
| **BOOTSTRAP SUPPLY** | | | | | | |
| Bootstrap diode forward voltage | $V_F$ | $I_F$ = 2 mA | | | 0.4 | V |
| **PWM CONTROL INPUT (SiC788)** | | | | | | |
| Rising threshold | $V_{TH_PWM_R}$ | | 3.4 | 3.7 | 4.0 | V |
| Falling threshold | $V_{TH_PWM_F}$ | | 0.72 | 0.9 | 1.1 | |
| Tri-state voltage | $V_{TRI}$ | $V_{PWM}$ = FLOAT | - | 2.3 | - | |
| Tri-state rising threshold | $V_{TRI_TH_R}$ | | 0.9 | 1.15 | 1.38 | |
| Tri-state falling threshold | $V_{TRI_TH_F}$ | | 3.1 | 3.35 | 3.6 | |
| Tri-state rising threshold hysteresis | $V_{HYS_TRI_R}$ | | - | 225 | - | mV |
| Tri-state falling threshold hysteresis | $V_{HYS_TRI_F}$ | | - | 325 | - | |
| PWM input current | $I_{PWM}$ | $V_{PWM}$ = 5 V | - | - | 350 | µA |
| | | $V_{PWM}$ = 0 V | - | - | -350 | |
| **PWM CONTROL INPUT (SiC788A)** | | | | | | |
| Rising threshold | $V_{TH_PWM_R}$ | | 2.2 | 2.45 | 2.7 | V |
| Falling threshold | $V_{TH_PWM_F}$ | | 0.72 | 0.9 | 1.1 | |
| Tri-state voltage | $V_{TRI}$ | $V_{PWM}$ = FLOAT | - | 1.8 | - | |
| Tri-state rising threshold | $V_{TRI_TH_R}$ | | 0.9 | 1.15 | 1.38 | |
| Tri-state falling threshold | $V_{TRI_TH_F}$ | | 1.95 | 2.2 | 2.45 | |
| Tri-state rising threshold hysteresis | $V_{HYS_TRI_R}$ | | - | 225 | - | mV |
| Tri-state falling threshold hysteresis | $V_{HYS_TRI_F}$ | | - | 275 | - | |
| PWM input current | $I_{PWM}$ | $V_{PWM}$ = 3.3 V | - | - | 225 | µA |
| | | $V_{PWM}$ = 0 V | - | - | -225 | |
| **TIMING SPECIFICATIONS** | | | | | | |
| Tri-State to GH/GL rising propagation delay | $t_{PD_TRI_R}$ | No load, see fig. 4 | - | 30 | - | ns |
| Tri-state hold-off time | $t_{TSHO}$ | | - | 130 | - | |
| GH - turn off propagation delay | $t_{PD_OFF_GH}$ | | - | 18 | - | |
| GH - turn on propagation delay (dead time rising) | $t_{PD_ON_GH}$ | | - | 15 | - | |
| GL - turn off propagation delay | $t_{PD_OFF_GL}$ | | - | 12 | - | |
| GL - turn on propagation delay (dead time falling) | $t_{PD_ON_GL}$ | | - | 8 | - | |
| DSBL# low to GH/GL falling propagation delay | $t_{PD_DSBL\#_F}$ | Fig. 5 | - | 15 | - | |
| DSBL# high to GH/GL rising propagation delay | $t_{PD_DSBL\#_R}$ | Fig. 5 | - | 20 | - | |
| PWM minimum on-time | $t_{PWM_ON_MIN}$ | | 30 | - | - | |
| **DSBL# SMOD# INPUT** | | | | | | |
| DSBL# logic input voltage | $V_{IH_DSBL\#}$ | Input logic high | 2 | - | - | V |
| | $V_{IL_DSBL\#}$ | Input logic low | - | - | 0.8 | |
| SMOD# logic input voltage | $V_{IH_SMOD\#}$ | Input logic high | 2 | - | - | |
| | $V_{IL_SMOD\#}$ | Input logic low | - | - | 0.8 | |
| **PROTECTION** | | | | | | |
| Under voltage lockout | $V_{UVLO}$ | $V_{CIN}$ rising, on threshold | - | 3.7 | 4.1 | V |
| | | $V_{CIN}$ falling, off threshold | 2.7 | 3.1 | - | |
| Under voltage lockout hysteresis | $V_{UVLO_HYST}$ | | - | 575 | - | mV |
| THWn flag set (2) | $T_{THWn_SET}$ | | - | 160 | - | °C |
| THWn flag clear (2) | $T_{THWn_CLEAR}$ | | - | 135 | - | |
| THWn flag hysteresis (2) | $T_{THWn_HYST}$ | | - | 25 | - | |
| THWn output low | $V_{OL_THWn}$ | $I_{THWn}$ = 2 mA | - | 0.02 | - | V |

**Notes**

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design



For technical questions, contact: powerictechsupport@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

## DETAILED OPERATIONAL DESCRIPTION

### PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM_TH_R}$ the low-side is turned off and the high-side is turned on. When PWM input is driven below $V_{PWM_TH_F}$ the high-side is turned off and the low-side is turned on. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shutdown. The high impedance state of the controller's PWM output allows the SiC788 and SiC788A to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, Fig. 4). If the PWM input stays in this region for the tri-state hold-off period, $t_{TSHO}$, both high-side and low-side MOSFETs are turned off. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC788A incorporates PWM voltage thresholds that are compatible with 3.3 V logic and the SiC788 thresholds are compatible with 5 V logic.

### Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFETs. In this state, standby current is minimized. If DSBL# is left unconnected, an internal pull-down resistor will pull the pin to $C_{GND}$ and shut down the IC.

### Pre-Charger Function

When DSBL# is driven from below $V_{IL_DSBL\#}$ to above $V_{IH_DSBL\#}$ the low-side is turned on for a short duration (60 ns typical) to refresh the BOOT capacitor in case it has been discharged due to the driver being in standby for a long period of time.

### Diode Emulation Mode (SMOD#)

When SMOD# is logic low diode emulation mode is enabled and the low-side is turned off. This is a non-synchronous conversion mode that improves light load efficiency by reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative can also be reduced. Circuitry in the external controller IC detects when inductor current crosses zero and drives SMOD# below $V_{IL_SMOD\#}$ turning the low-side MOSFET off. The function can be also be used for a pre-biased output voltage. If SMOD# is left unconnected, an internal pull up resistor will pull the pin to $V_{CIN}$ (logic high) to disable the SMOD# function.

### Thermal Shutdown Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect, with a maximum of 20 kΩ, to $V_{CIN}$. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC788 and SiC788A do not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

### Voltage Input ($V_{IN}$)

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

### Switch Node ($V_{SWH}$ and PHASE)

The switch node, $V_{SWH}$, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node, $V_{SWH}$. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that $V_{CIN}$ goes to zero while $V_{IN}$ is still applied.

### Ground Connections ($C_{GND}$ and $P_{GND}$)

$P_{GND}$ (power ground) should be externally connected to $C_{GND}$ (control signal ground). The layout of the printed circuit board should be such that the inductance separating $C_{GND}$ and $P_{GND}$ is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V

### Control and Drive Supply Voltage Input ($V_{DRV}$, $V_{CIN}$)

$V_{CIN}$ is the bias supply for the gate drive control IC. $V_{DRV}$ is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

### Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

### Shoot-Through Protection and Adaptive Dead Time

The SiC788 and SiC788A have an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned on at the same time. The adaptive dead time control operates as follows. The high-side and low-side gate voltages are monitored to prevent the MOSFET turning on from tuning on until the other MOSFET's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOSFET is completely off, before the other can be turned ON. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

### Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive, holding high-side and low-side MOSFET gates low, until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC788 and SiC788A also incorporate logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

## FUNCTIONAL BLOCK DIAGRAM

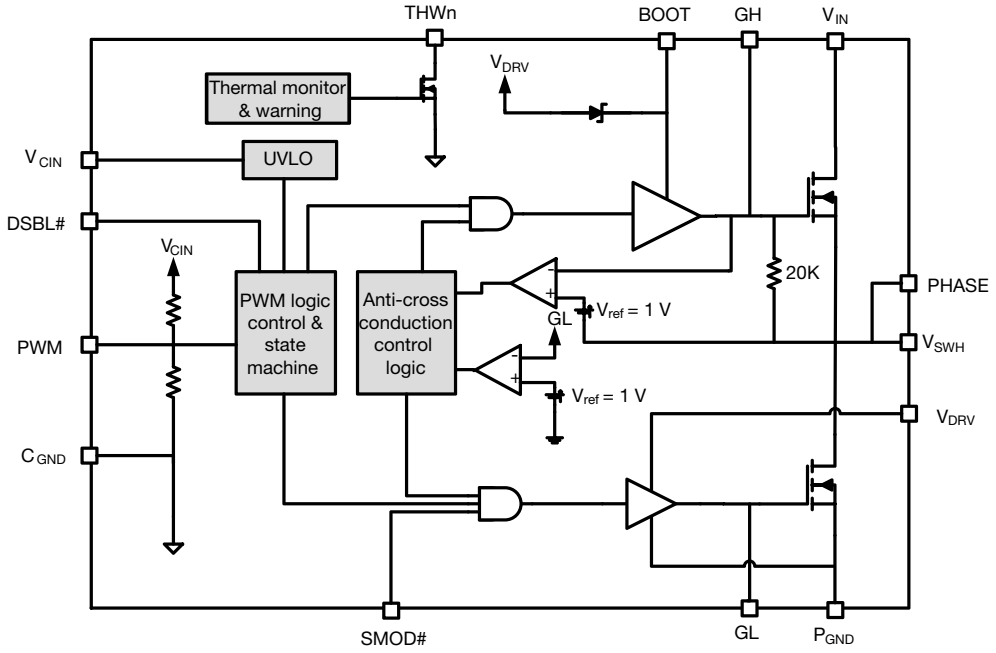



**Fig. 3 - SiC788 and SiC788A Functional Block Diagram**

| DEVICE TRUTH TABLE | | | | |
|---|---|---|---|---|
| **DSBL#** | **SMOD#** | **PWM** | **GH** | **GL** |
| Open | X | X | L | L |
| L | X | X | L | L |
| H | L | L | L | L |
| H | L | H | H | L |
| H | L | Tri-state | L | L |
| H | H | L | L | H |
| H | H | H | H | L |
| H | H | Tri-state | L | L |


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

## PWM TIMING DIAGRAM

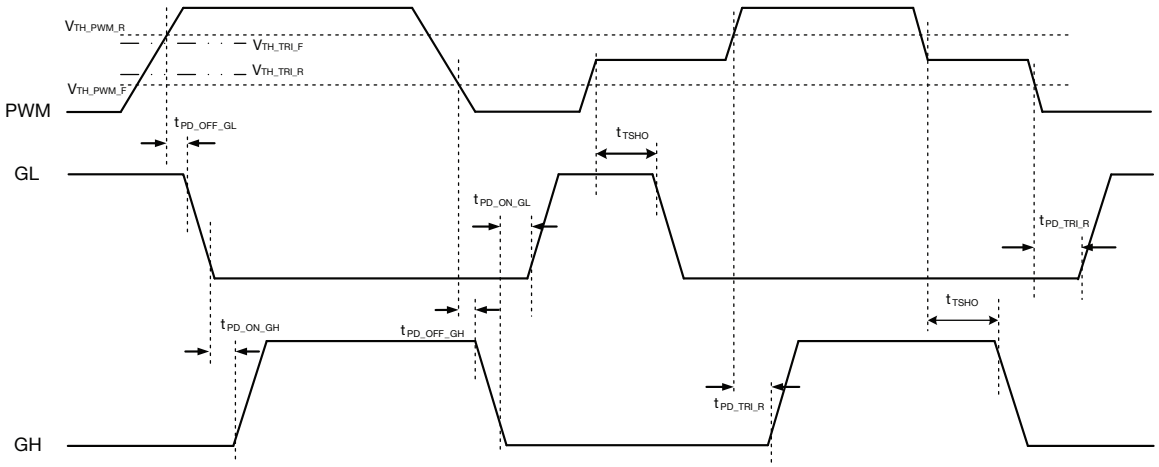
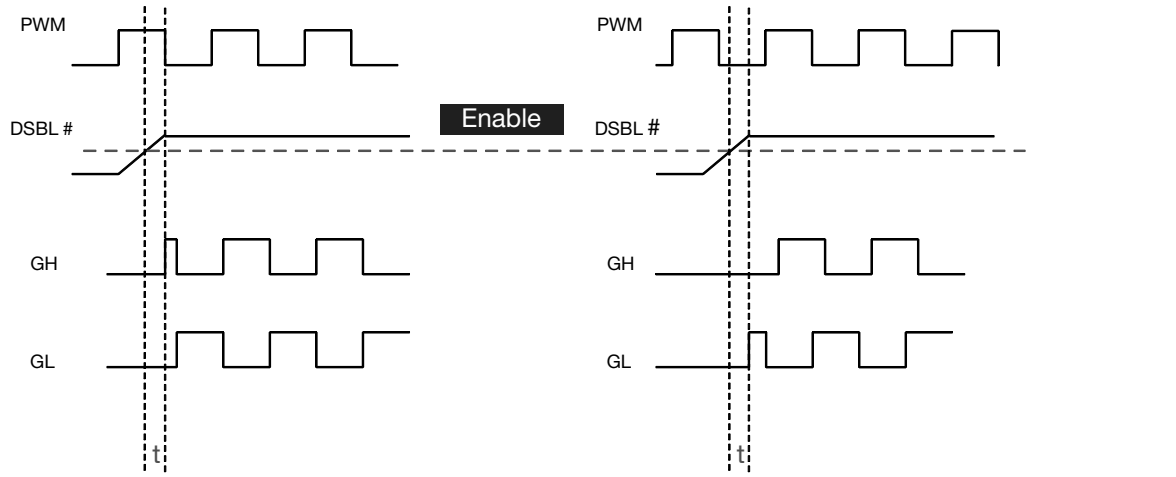


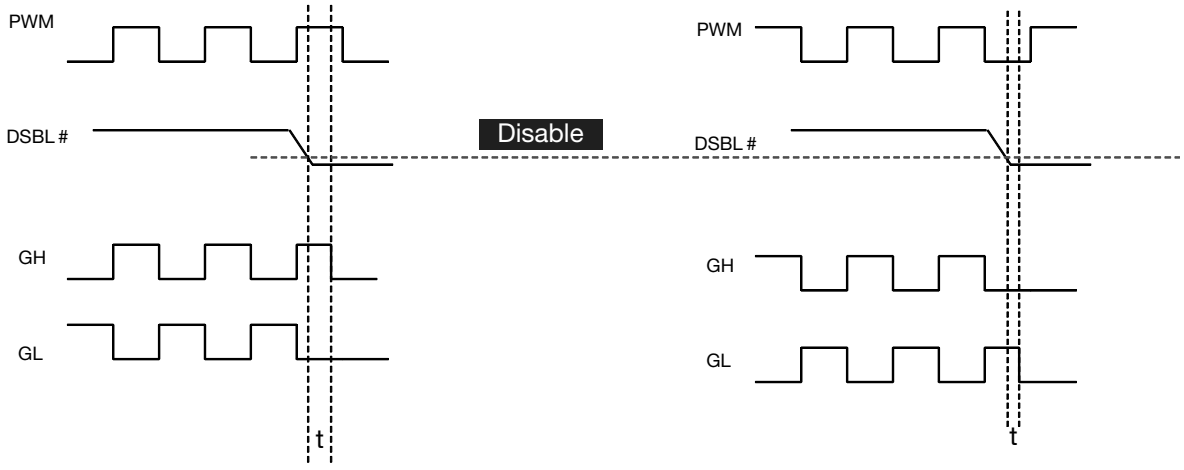

**Fig. 4 - Definition of PWM Logic and Tri-State**

## OPERATION TIMING DIAGRAM: DSBL#




DSBL# High to GH Rising Propagation Delay

DSBL# High to GL Rising Propagation Delay




DSBL# Low to GH Falling Propagation Delay

DSBL# Low to GL Falling Propagation Delay

**Fig. 5 - DSBL# Propagation Delay**


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

## ELECTRICAL CHARACTERISTICS

Test condition: $V_{IN}$ = 12 V, $V_{DRV}$ = $V_{CIN}$ = 5 V, DSBL# = SMOD# = 5 V, $V_{OUT}$ = 1.8 V, $L_{OUT}$ = 250 nH (DCR = 0.32 mΩ), $T_A$ = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC788 and SiC788A losses only unless otherwise stated)

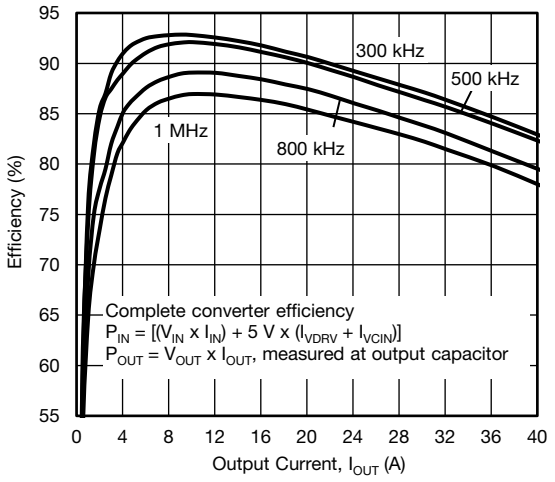



**Fig. 6 - Efficiency vs. Output Current**

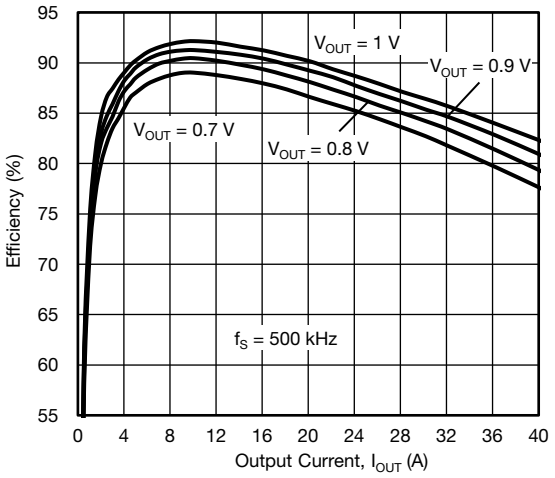



**Fig. 7 - Efficiency vs. Output Current**

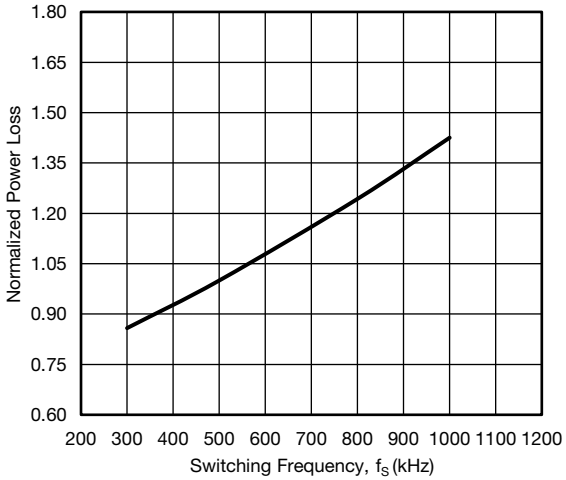



**Fig. 8 - Power Loss vs. Switching Frequency**

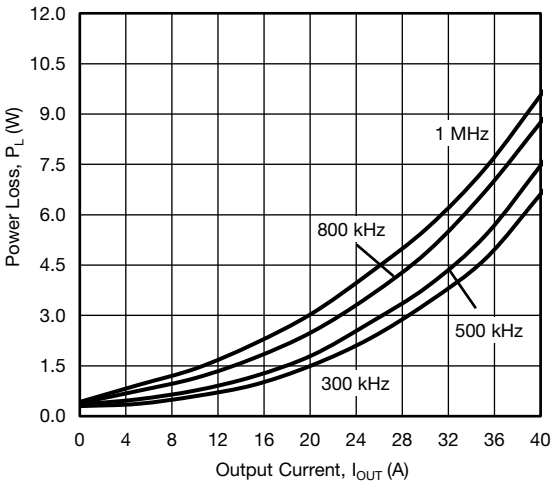



**Fig. 9 - Power Loss vs. Output Current**

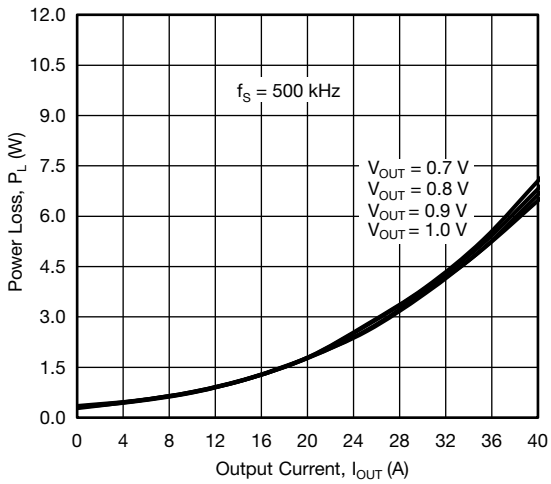



**Fig. 10 - Power Loss vs. Output Current**


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

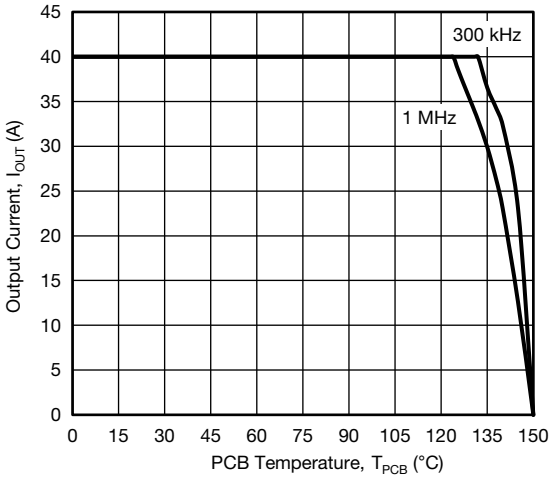



**Fig. 11 - Safe Operating Area**

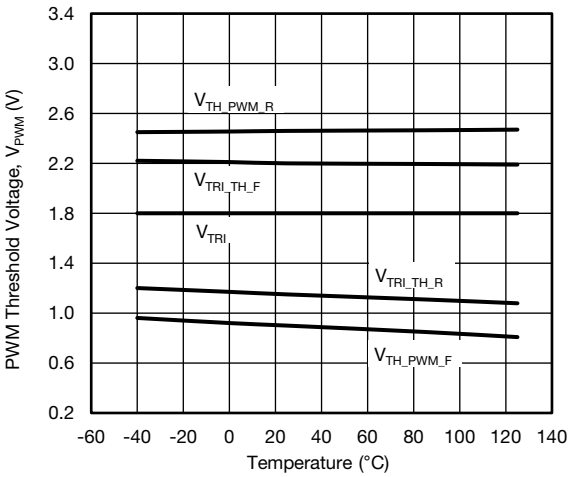



**Fig. 14 - PWM Threshold vs. Temperature (SiC788A)**

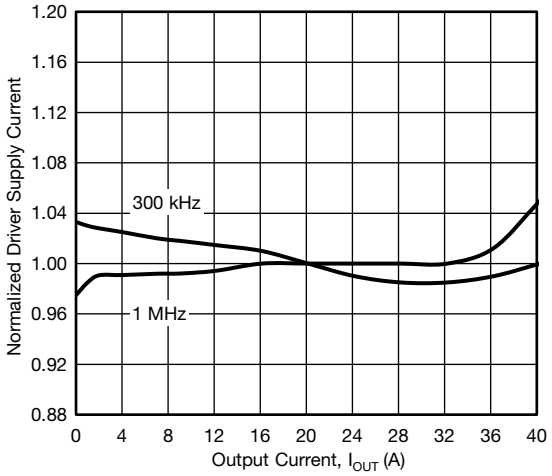



**Fig. 12 - Driver Supply Current vs. Output Current**

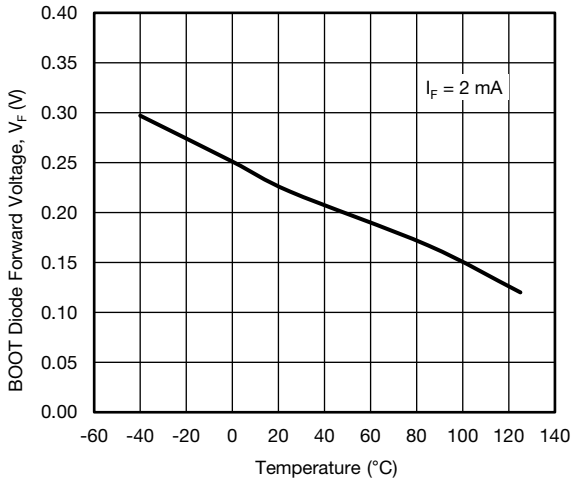



**Fig. 15 - BOOT Diode Forward Voltage vs. Temperature**

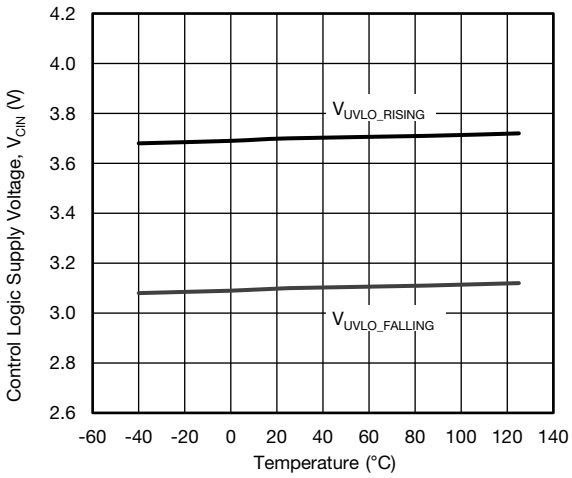



**Fig. 13 - UVLO Threshold vs. Temperature**

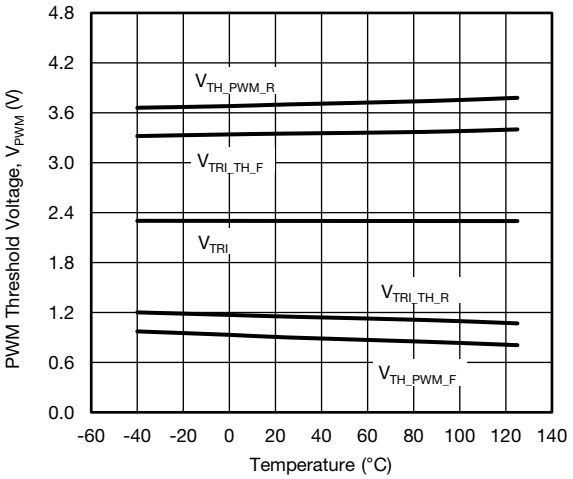



**Fig. 16 - PWM Threshold vs. Temperature (SiC788)**


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

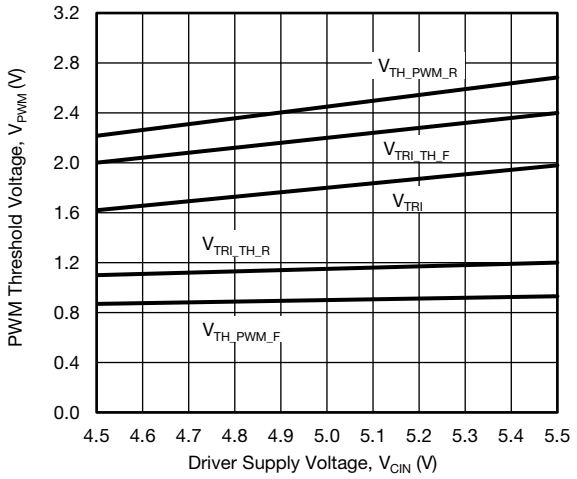



**Fig. 17 - PWM Threshold vs. Driver Supply Voltage (SiC788A)**

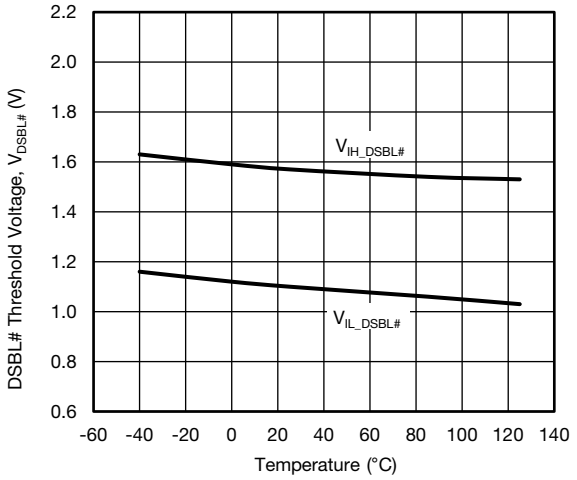



**Fig. 18 - DSBL# Threshold vs. Temperature**

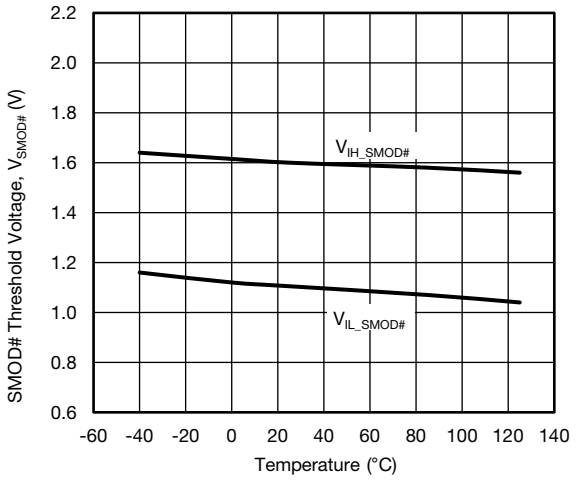



**Fig. 19 - SMOD# Threshold vs. Temperature**

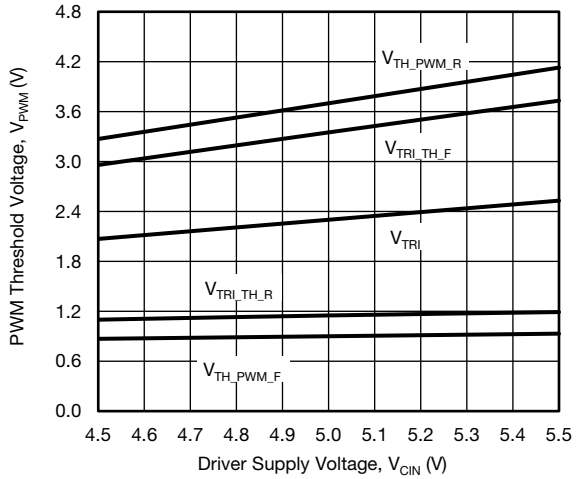



**Fig. 20 - PWM Threshold vs. Driver Supply Voltage (SiC788)**

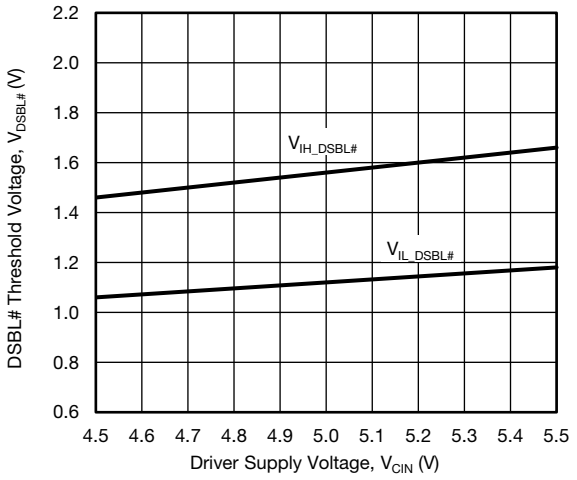



**Fig. 21 - DSBL# Threshold vs. Driver Supply Voltage**

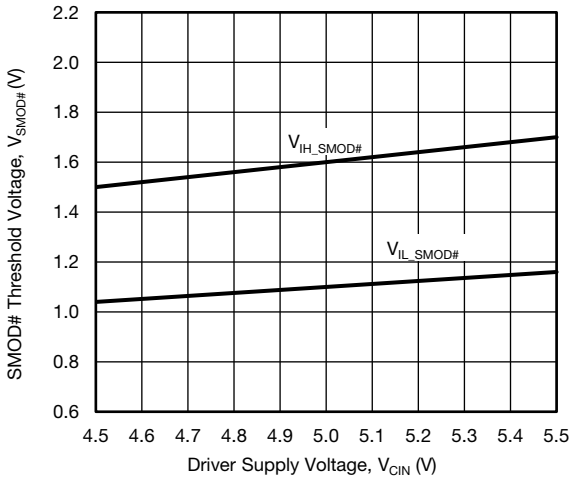



**Fig. 22 - SMOD# Threshold vs. Driver Supply Voltage**


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

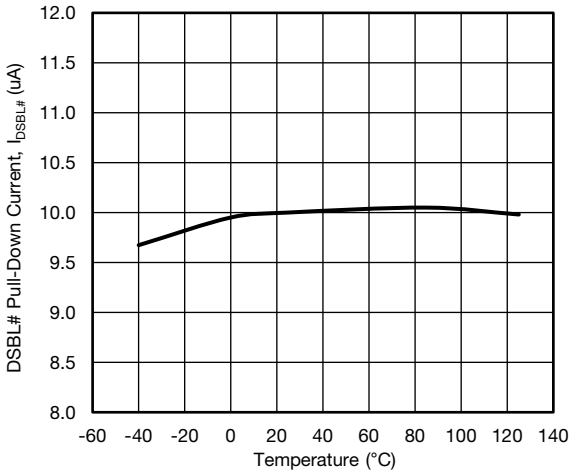



**Fig. 23 - DSBL# Pull-down Current vs. Temperature**

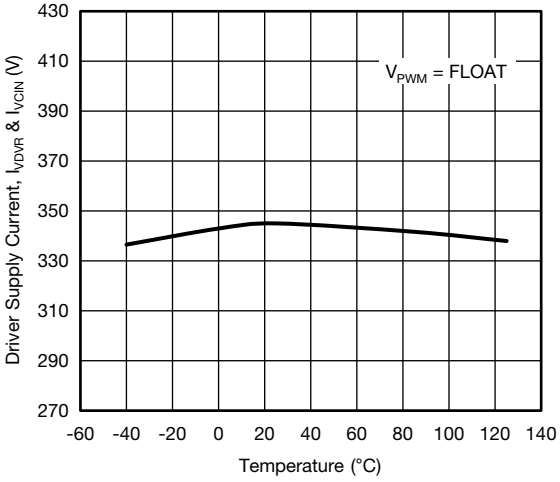



**Fig. 26 - Driver Quiescent Current vs. Temperature**

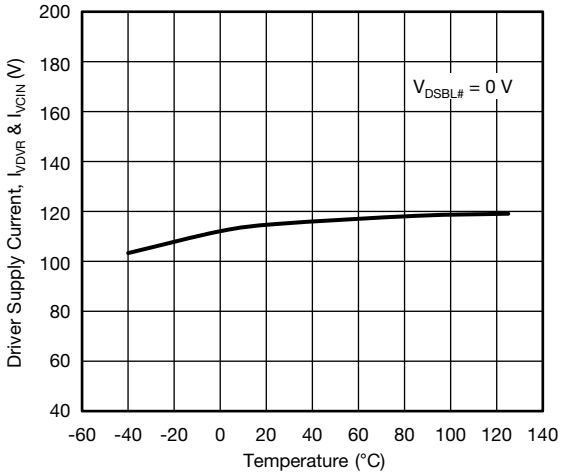



**Fig. 24 - Driver Quiescent Current vs. Temperature**

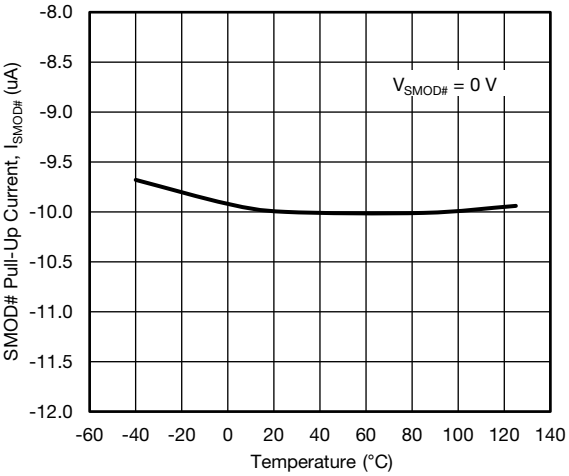
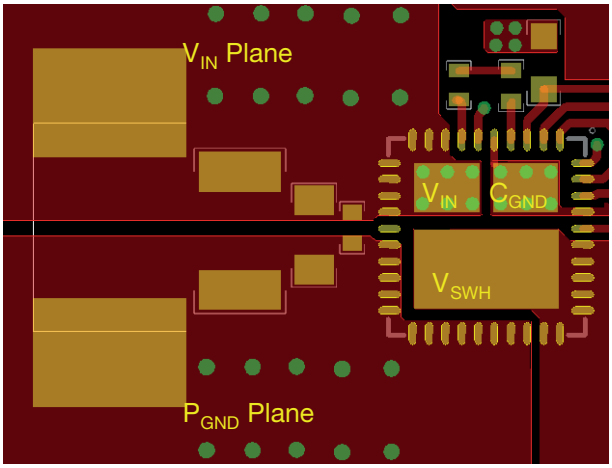



**Fig. 25 - SMOD# Pull-up Current vs. Temperature**


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

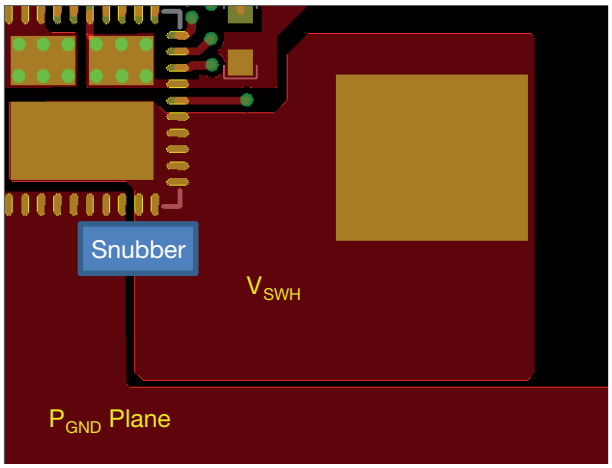
## PCB LAYOUT RECOMMENDATIONS

### Step 1: $V_{IN}$ / $P_{GND}$ Planes and Decoupling



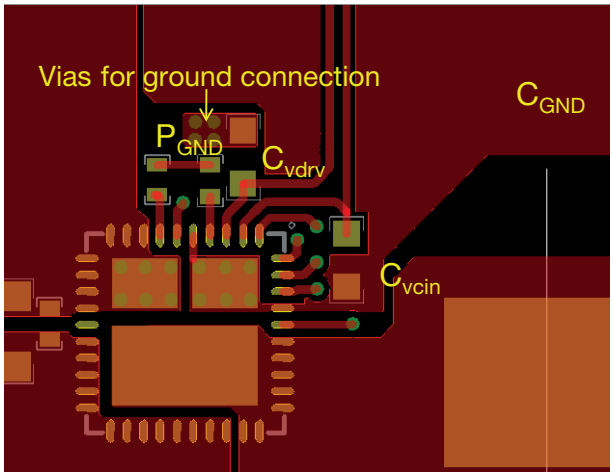

1. Layout $V_{IN}$ and $P_{GND}$ planes as shown above
2. Ceramic capacitors should be placed directly between $V_{IN}$ and $P_{GND}$, and as close as possible to IC for best decoupling effect
3. Different ceramic capacitor values and packages should be used to cover entire decoupling spectrum, e.g. 1210, 0805, 0603, and 0402
4. Smaller capacitance values, placed closer to the IC's $V_{IN}$ pin(s), result in better high frequency noise absorbing

### Step 2: $V_{SWH}$ Plane



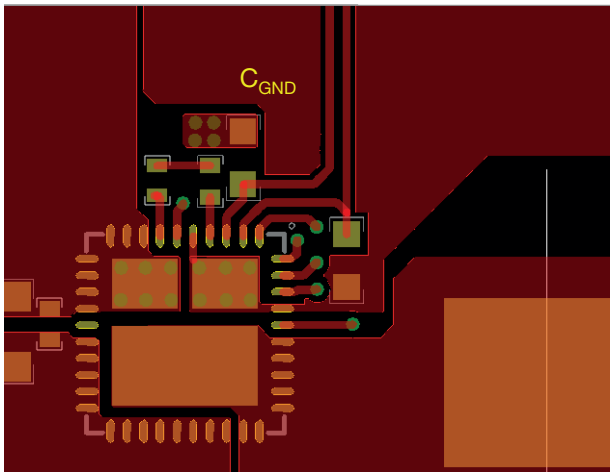

1. Connect output inductor to IC with large plane to lower resistance
2. $V_{SWH}$ plane also serves as a heat-sink for low-side MOSFET. Please make the plane wide and short to achieve best thermal path
3. If a snubber network is required, place components as shown above

### Step 3: $V_{CIN}$ / $V_{DRV}$ Input Filter




1. $V_{CIN}$ / $V_{DRV}$ input filter ceramic capacitors should be placed as close as possible to IC. It is recommended to connect two capacitors separately
2. $V_{CIN}$ capacitor should be placed between pin 2 and pin 37 ($C_{GND}$ of driver IC) to achieve best noise filtering
3. $V_{DRV}$ capacitor should be placed between pin 3 and $P_{GND}$ to provide maximum instantaneous driver current for low-side MOSFET during switching cycle. $P_{GND}$ can be connected to inner ground plane through vias, as shown above
4. Pin 5 and pin 37 should be connected with $C_{GND}$ pad, as shown above
5. For connecting $V_{CIN}$ to $C_{GND}$, it is recommended to use a large plane to reduce parasitic inductance

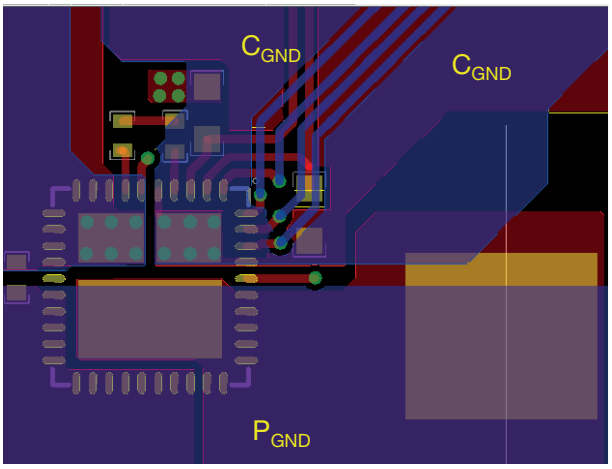
### Step 4: BOOT Resistor and Capacitor Placement




1. The components need to be placed as close as possible to IC, directly between PHASE (pin 7) and BOOT (pin 4)
2. To reduce parasitic inductance, 0402 package size can be used

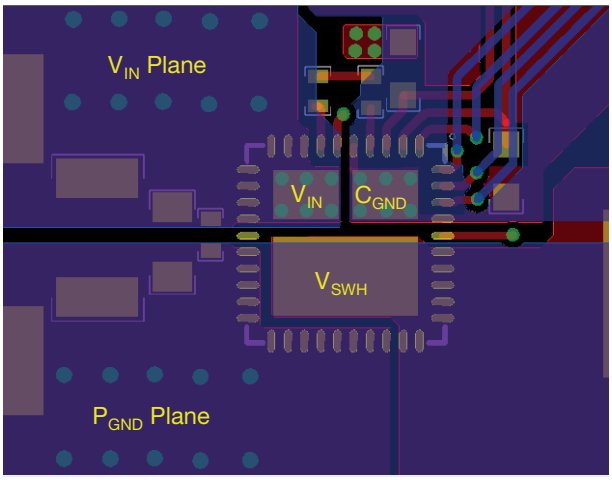

For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

**Step 5: Signal Routing**



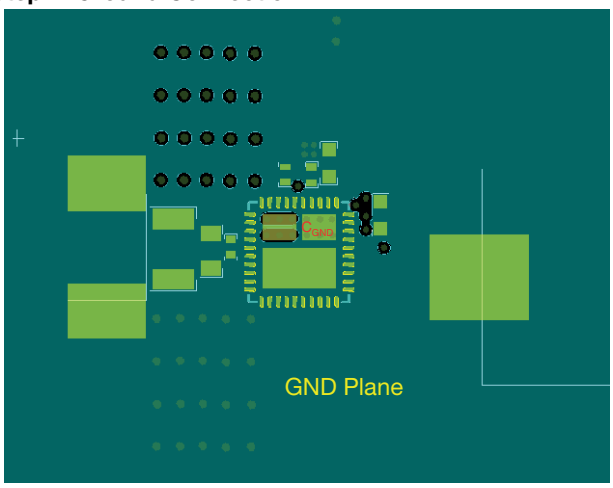

1. Route the PWM, SMOD#, DSBL#, and THWn signal traces out of the top right corner, next to pin 1
2. The PWM signal is a very important signal, both signal and return traces should not cross any power nodes on any layer
3. It is best to “shield” these traces from power switching nodes, e.g. $V_{SWH}$, with a GND island to improve signal integrity

**Step 6: Adding Thermal Relief Vias**




1. Thermal relief vias can be added to the $V_{IN}$ and $C_{GND}$ pads to utilize inner layers for high-current and thermal dissipation
2. To achieve better thermal performance, additional vias can be added to $V_{IN}$ and $P_{GND}$ planes
3. The $V_{SWH}$ pad is a noise source and it is not recommended to place vias on this pad
4. 8 mil vias for pads and 10 mils vias for planes are the optimal sizes. Vias on pad may drain solder during assembly and cause assembly issues. Please consult with the assembly house for guidelines

**Step 7: Ground Connection**




1. It is recommended to make the entire first inner layer (below top layer) the ground plane
2. The ground plane provides analog ground and power ground connections
3. The ground plane provides shielding between noise source on top layer and signal traces on bottom layer


For technical questions, contact: powerictechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

| PRODUCT SUMMARY | | |
|---|---|---|
| Part number | SiC788 | SiC788A |
| Description | 50 A power stage, 4.5 $V_{IN}$ to 18 $V_{IN}$, 5 V PWM with diode emulation mode | 50 A power stage, 4.5 $V_{IN}$ to 18 $V_{IN}$, 3.3 V PWM with diode emulation mode |
| Input voltage min. (V) | 4.5 | 4.5 |
| Input voltage max. (V) | 18 | 18 |
| Continuous current rating max. (A) | 50 | 50 |
| Switch frequency max. (kHz) | 1000 | 1000 |
| Enable (yes / no) | Yes | Yes |
| Monitoring features | - | - |
| Protection | UVLO, THDN | UVLO, THDN |
| Light load mode | Diode emulation | Diode emulation |
| Pulse-width modulation (V) | 5 | 3.3 |
| Package type | PowerPAK MLP66-40L | PowerPAK MLP66-40L |
| Package size (W, L, H) (mm) | 6.0 x 6.0 x 0.75 | 6.0 x 6.0 x 0.75 |
| Status code | 2 | 2 |
| Product type | VRPower (DrMOS) | VRPower (DrMOS) |
| Applications | Computer, industrial, networking | Computer, industrial, networking |

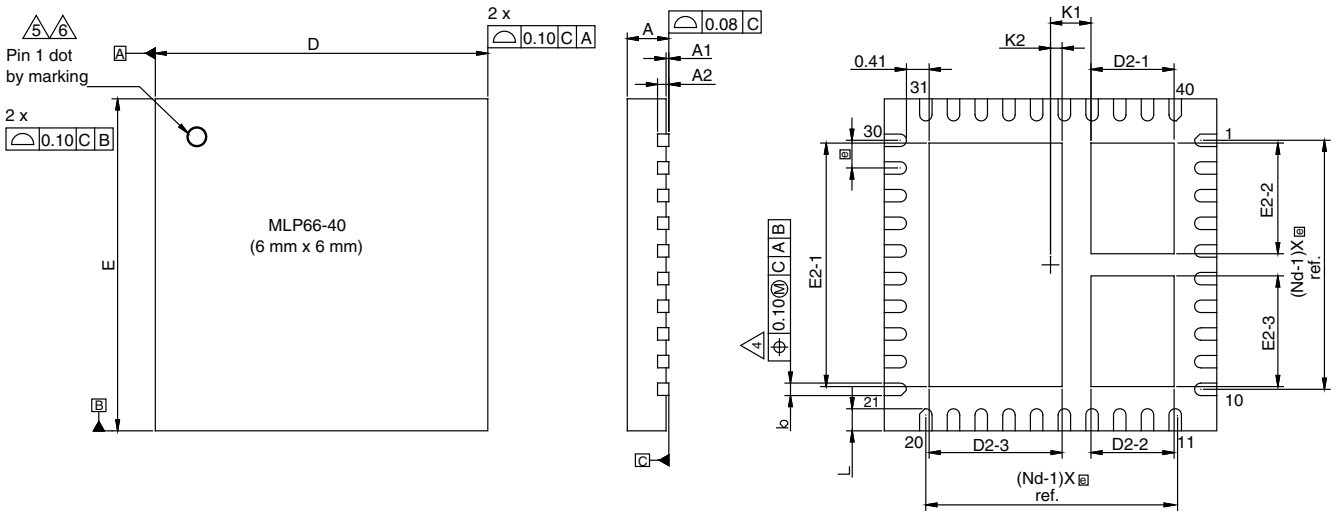
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62985.*



For technical questions, contact: powerictechsupport@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

# PowerPAK® MLP66-40 Case Outline




Top View

Side View

Bottom View

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A (8) | 0.70 | 0.75 | 0.80 | 0.027 | 0.029 | 0.031 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| A2 | | 0.20 ref. | | | 0.008 ref. | |
| b (4) | 0.20 | 0.25 | 0.30 | 0.078 | 0.098 | 0.011 |
| D | | 6.00 BSC | | | 0.236 BSC | |
| e | | 0.50 BSC | | | 0.019 BSC | |
| E | | 6.00 BSC | | | 0.236 BSC | |
| L | 0.35 | 0.40 | 0.45 | 0.013 | 0.015 | 0.017 |
| N (3) | | 40 | | | 40 | |
| Nd (3) | | 10 | | | 10 | |
| Ne (3) | | 10 | | | 10 | |
| D2-1 | 1.45 | 1.50 | 1.55 | 0.057 | 0.059 | 0.061 |
| D2-2 | 1.45 | 1.50 | 1.55 | 0.057 | 0.059 | 0.061 |
| D2-3 | 2.35 | 2.40 | 2.45 | 0.095 | 0.094 | 0.096 |
| E2-1 | 4.35 | 4.40 | 4.45 | 0.171 | 0.173 | 0.175 |
| E2-2 | 1.95 | 2.00 | 2.05 | 0.076 | 0.078 | 0.080 |
| E2-3 | 1.95 | 2.00 | 2.05 | 0.076 | 0.078 | 0.080 |
| K1 | | 0.73 BSC | | | 0.028 BSC | |
| K2 | | 0.21 BSC | | | 0.008 BSC | |
| ECN: T14-0826-Rev. B, 12-Jan-15<br>DWG: 5986 | | | | | | |

**Notes**

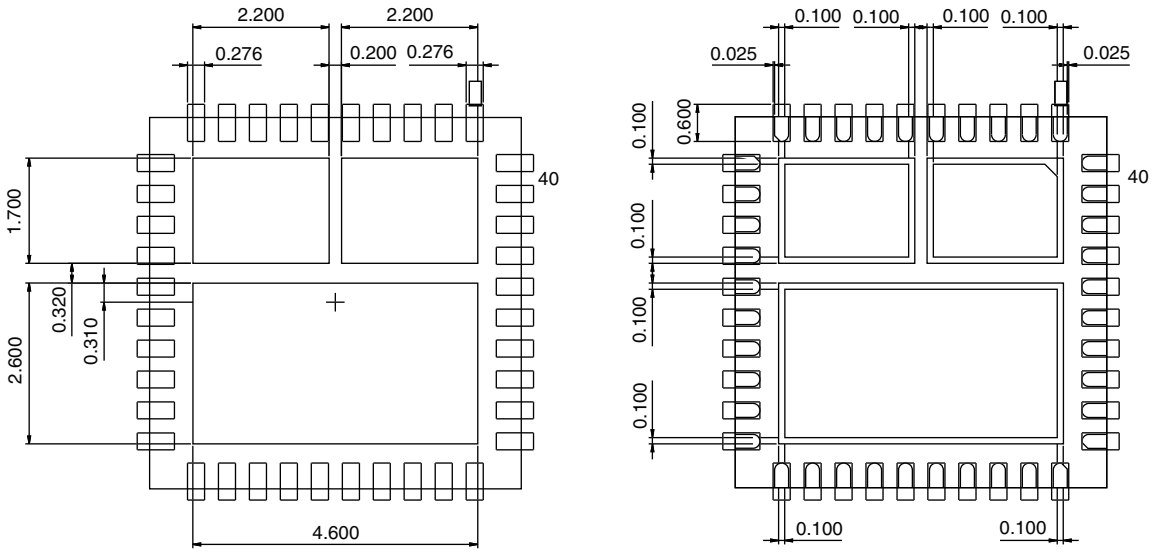
1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals



For technical questions, contact: powerictechsupport@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

# Recommended Land Pattern PowerPAK® MLP66-40L




All Dimensions are in milimeters



For technical questions, contact: analogswitchtechsupport@vishay.com

THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

# Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

*© 2022 VISHAY INTERTECHNOLOGY, INC. ALL RIGHTS RESERVED*