ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 250-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **250-mA Low-Dropout Regulator With Enable**
- **Available in Fixed and Adjustable (1.2 V to 5.5 V) Versions**
- **High PSRR (60 dB at 10 kHz)**
- **Ultralow Noise (32 μVrms, TPS79428)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 2.2-μF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage (155 mV at Full Load)**
- **Available in MSOP-8 and SOT223-6 Packages**

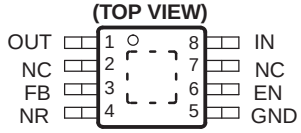
APPLICATIONS

- **RF: VCOs, Receivers, ADCs**
- **Audio**
- **Bluetooth™, Wireless LAN**
- **Cellular and Cordless Telephones**
- **Handheld Organizers, PDAs**

DESCRIPTION

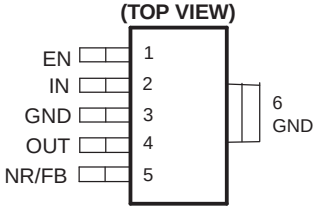
The TPS794xx family of low-dropout (LDO) linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in small outline, MSOP-8 PowerPAD™ and SOT223-6 packages. Each device in the family is stable with a small 2.2-μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 155 mV at 250 mA). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79428 exhibits approximately 32 μV_{RMS} of output voltage noise at 2.8 V output with a 0.1-μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

DGN PACKAGE
MSOP-8 PowerPAD™
(TOP VIEW)

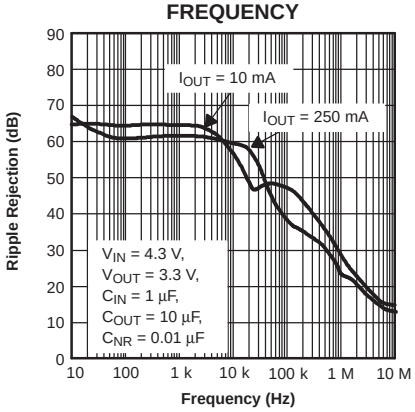


NC − No internal connection

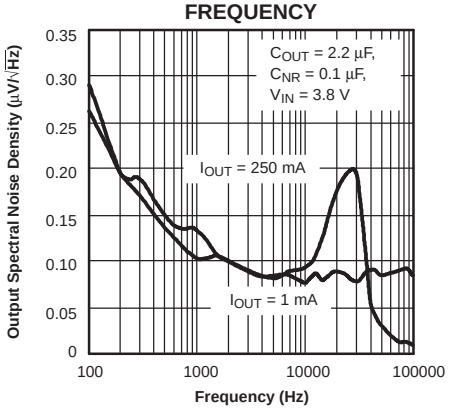
DCQ PACKAGE
SOT223-6
(TOP VIEW)



TPS79433
RIPPLE REJECTION vs FREQUENCY



TPS79428
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY



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Bluetooth is a trademark of Bluetooth SIG, Inc.
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS794**xxyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 1.3 V to 5.0 V in 100 mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

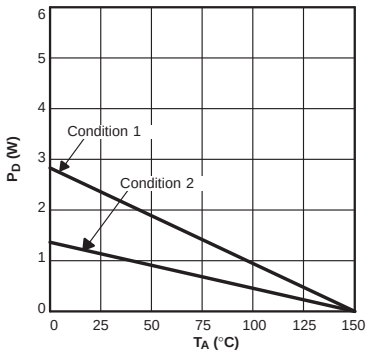
over operating temperature range unless otherwise noted(1)

	VALUE
V_{IN} range	–0.3 V to 6 V
V_{EN} range	–0.3 V to V_{IN} + 0.3 V
V_{OUT} range	–0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, T_J	–40°C to +150°C
Storage temperature range, T_{stg}	–65°C to +150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)	$T_A \leq 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	0	8.47	55.09	2.27 W	1.45 W	1.18 W
	150	8.21	49.97	2.50 W	1.60 W	1.30 W
	250	8.20	48.10	2.60 W	1.66 W	1.35 W



CONDITIONS	PACKAGE	PCB AREA	θJA
1	SOT223	4in² Top Side Only	53°C/W
2	SOT223	0.5in² Top Side Only	110°C/W

Figure 1. SOT223 Power Dissipation

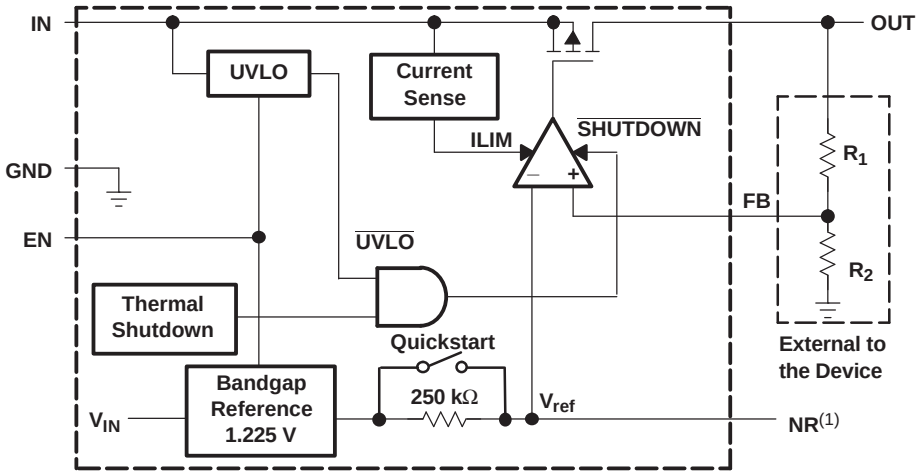
ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_J = –40°C to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01 µF, unless otherwise noted. Typical values are at 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage, V_{IN}(1)					2.7		5.5	V
Continuous output current, I_{OUT}					0		250	mA
Output voltage	Output voltage range	TPS79401			1.225		5.5 – V_{DO}	V
	Accuracy	TPS79401(2)	0 µA ≤ I_{OUT} ≤ 250 mA, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		0.97(V_{OUT})	V_{OUT}	1.03(V_{OUT})	V
		Fixed V_{OUT}	0 µA ≤ I_{OUT} ≤ 250 mA, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–3.0		+3.0	%
Output voltage line regulation ($\Delta V_{OUT}\%/\Delta V_{IN}$)(1)			V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			0.05	0.12	%/V
Load regulation ($\Delta V_{OUT}\%/\Delta I_{OUT}$)			0 µA ≤ I_{OUT} ≤ 250 mA			10		mV
Dropout voltage(3) V_{IN} = $V_{OUT(nom)}$ – 0.1 V		TPS79428	I_{OUT} = 250 mA			155	210	mV
		TPS79430	I_{OUT} = 250 mA			155	210	
		TPS79433	I_{OUT} = 250 mA			145	200	
Output current limit			V_{OUT} = 0 V			925		mA
Ground pin current			0 µA ≤ I_{OUT} ≤ 250 mA			170	220	µA
Shutdown current(4)			V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	µA
FB pin current			V_{FB} = 1.225 V				1	µA
Power-supply ripple rejection		TPS79428	f = 100 Hz, I_{OUT} = 250 mA			65		dB
			f = 10 kHz, I_{OUT} = 250 mA			60		
			f = 100 kHz, I_{OUT} = 250 mA			40		
Output noise voltage		TPS79428	BW = 100 Hz to 100 kHz, I_{OUT} = 250 mA	C_{NR} = 0.001 µF		55		μV_{RMS}
				C_{NR} = 0.0047 µF		36		
				C_{NR} = 0.01 µF		33		
				C_{NR} = 0.1 µF		32		
Time, start-up		TPS79428	R_L = 14 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		70		
				C_{NR} = 0.01 µF		100		
High-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		1.7		V_{IN}	V
Low-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.7	V
EN pin current			V_{EN} = 0		1		1	µA
UVLO threshold			V_{CC} rising		2.25		2.65	V
UVLO hysteresis						100		mV

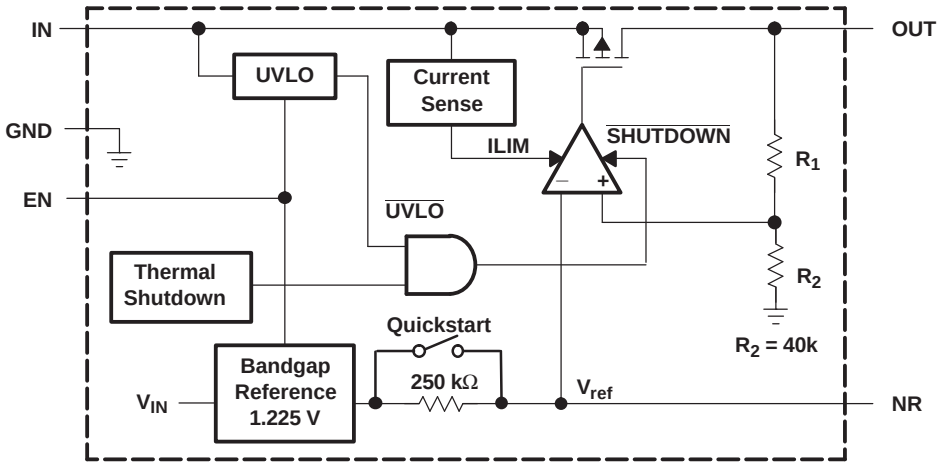
(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured for the TPS79418 and TPS79425 since minimum V_{IN} = 2.7 V.
(4) For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



(1) Not Available on DCQ (SOT223) options.

FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			DESCRIPTION
NAME	DGN (MSOP)	DCQ (SOT223)	
NR	4	5	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise.
EN	6	1	The EN terminal is an input that enables or shuts down the device. When EN is a logic high, the device is enabled. When the device is a logic low, the device is in shutdown mode.
FB	3	5	Feedback input voltage for the adjustable device.
GND	5, PAD	3, 6	Regulator ground
IN	8	2	Unregulated input to the device.
NC	2, 7		No internal connection.
OUT	1	4	Regulator output

TYPICAL CHARACTERISTICS

TPS79433
OUTPUT VOLTAGE
vs OUTPUT CURRENT

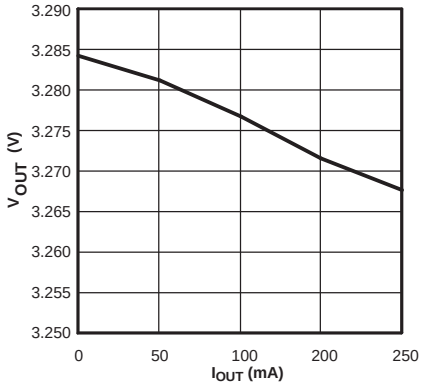


Figure 2.

TPS79428
OUTPUT VOLTAGE
vs JUNCTION TEMPERATURE

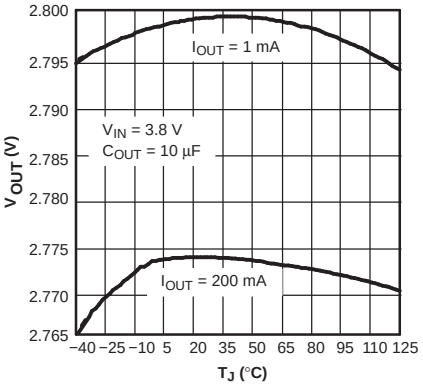


Figure 3.

TPS79428
GROUND CURRENT
vs JUNCTION TEMPERATURE

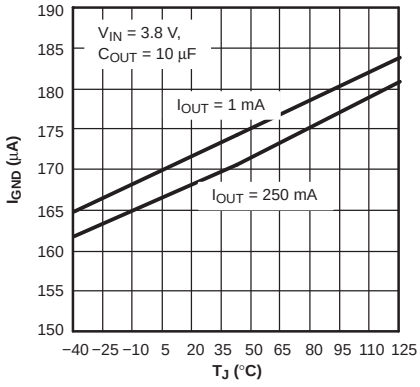


Figure 4.

TPS79428
OUTPUT SPECTRAL
NOISE DENSITY
vs FREQUENCY

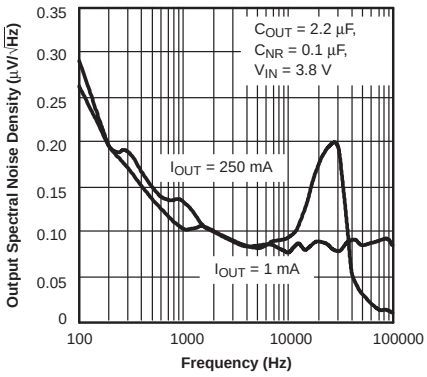


Figure 5.

TPS79428
OUTPUT SPECTRAL
NOISE DENSITY
vs FREQUENCY

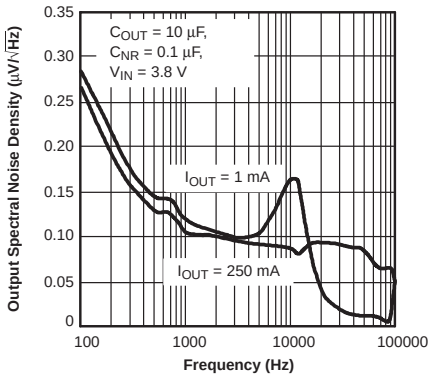


Figure 6.

TPS79428
OUTPUT SPECTRAL
NOISE DENSITY
vs FREQUENCY

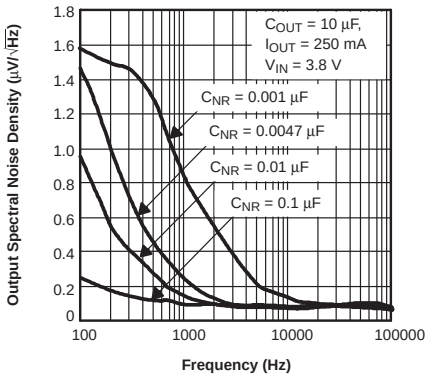


Figure 7.

TPS79428
ROOT MEAN SQUARED
OUTPUT NOISE vs C_{NR}

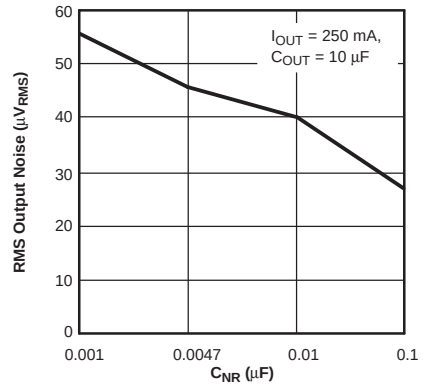


Figure 8.

TPS79433
OUTPUT IMPEDANCE
vs FREQUENCY

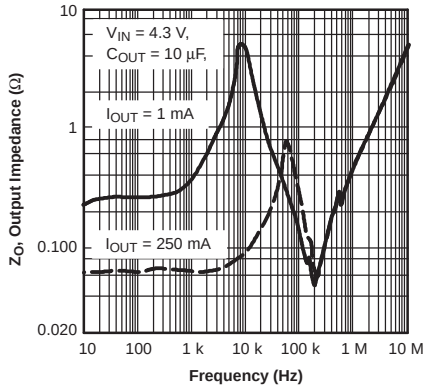


Figure 9.

TPS79428
DROPOUT VOLTAGE
vs JUNCTION TEMPERATURE

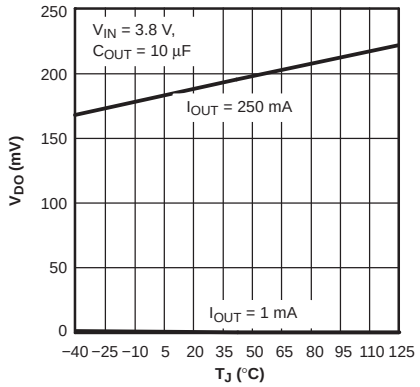


Figure 10.

TYPICAL CHARACTERISTICS (continued)

TPS79433
RIPPLE REJECTION
vs FREQUENCY

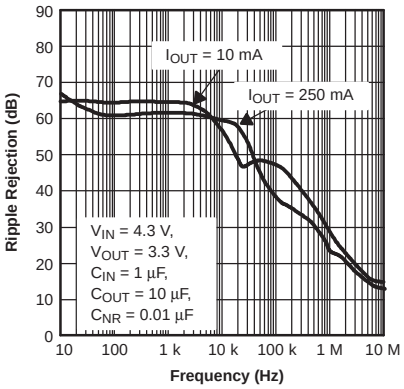


Figure 11.

TPS79433
RIPPLE REJECTION
vs FREQUENCY

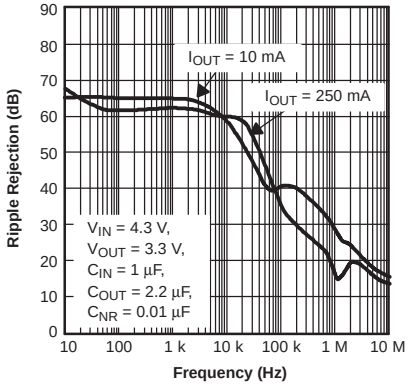


Figure 12.

TPS79433
RIPPLE REJECTION
vs FREQUENCY

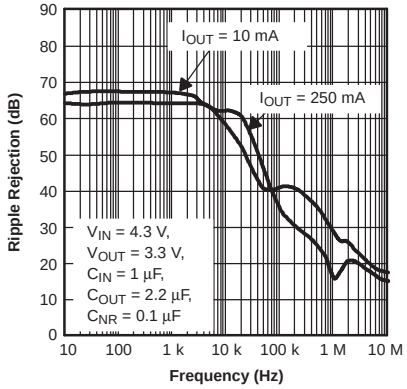


Figure 13.

TPS79433
OUTPUT VOLTAGE,
ENABLE VOLTAGE
vs TIME (START-UP)

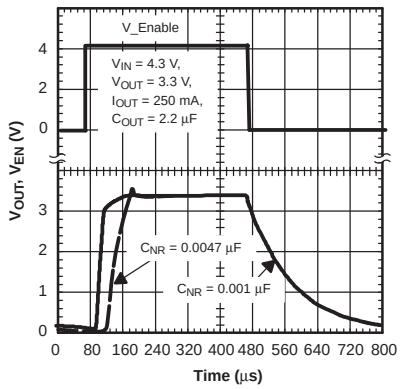


Figure 14.

TPS79433
LINE TRANSIENT
RESPONSE

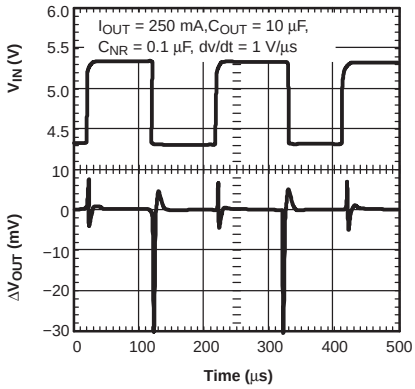


Figure 15.

TPS79433
LOAD TRANSIENT
RESPONSE

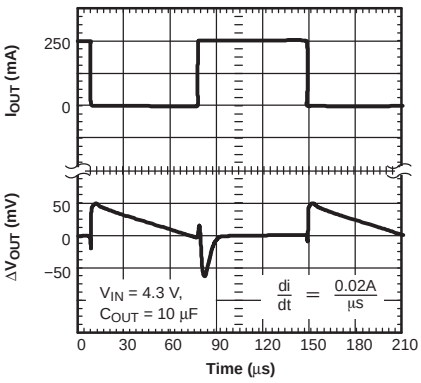


Figure 16.

TPS79425
POWER-UP/
POWER-DOWN

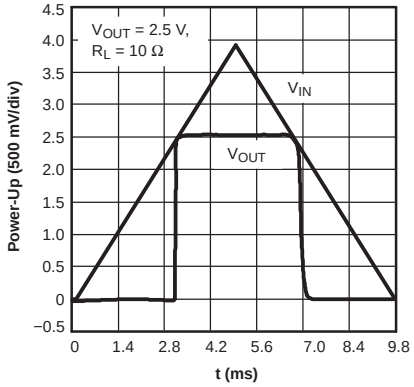


Figure 17.

TPS79433
DROPOUT VOLTAGE
vs OUTPUT CURRENT

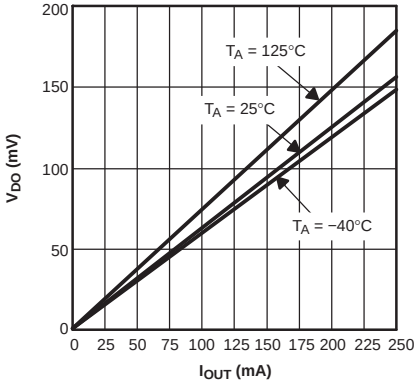


Figure 18.

TPS79401
DROPOUT VOLTAGE
vs INPUT VOLTAGE

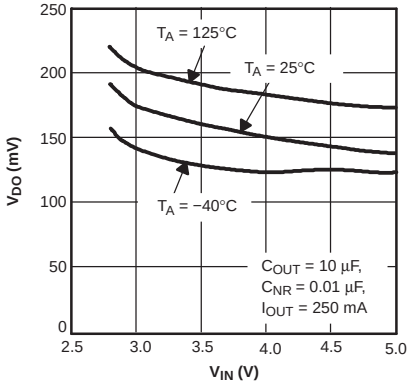


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TPS79428
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs OUTPUT CURRENT

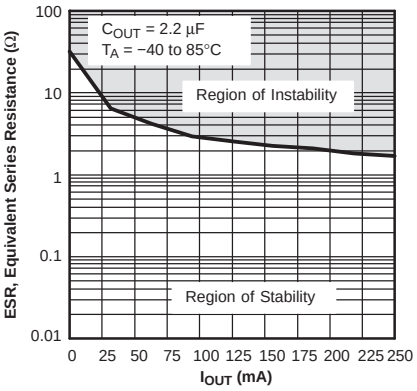


Figure 20.

TPS79428
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs OUTPUT CURRENT

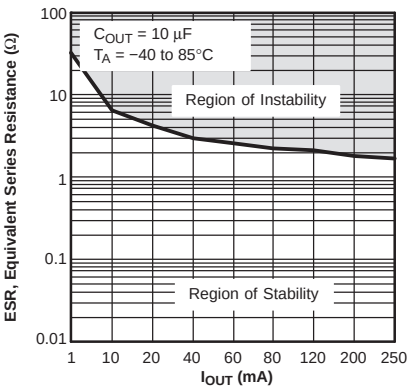


Figure 21.

APPLICATION INFORMATION

The TPS794xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 µA typically), and an enable input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

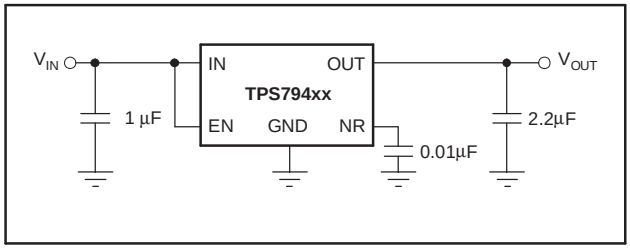


Figure 22. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS794xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS794xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 µF. Any 1 µF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS794xx has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1-µF in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the Functional Block Diagram.

For example, the TPS79430 exhibits only 33 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 10-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Report SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI web site (www.ti.com).

PROGRAMMING THE TPS79401 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79401 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

- V_{REF} = 1.2246 V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 40-µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 40 µA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated as Equation 3:

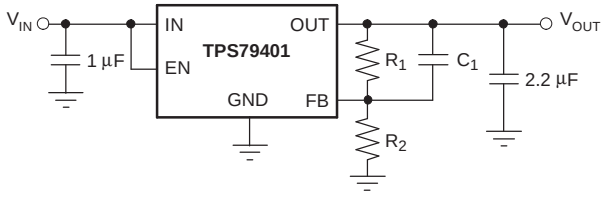
$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within Figure 23. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 µF instead of 1 µF.

REGULATOR PROTECTION

The TPS794xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS794xx features internal current limiting and thermal protection. During normal operation, the TPS794xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.8 V	14.0 kΩ	30.1 kΩ	22 pF
3.6 V	61.9 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79401 Adjustable LDO Regulator Programming

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_D$max) consumed by a linear regulator is computed as shown in Equation 4:

$$P_D\text{max} = \left(V_{IN(avg)} - V_{OUT(avg)}\right) \times I_{OUT(avg)} + V_{I(avg)} \times I_Q \quad (4)$$

where:

- $V_{IN(avg)}$ is the average input voltage
- $V_{OUT(avg)}$ is the average output voltage
- $I_{OUT(avg)}$ is the average output current
- I_Q is the quiescent current

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)}$ x I_Q can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\Theta JC}$), the case to heatsink ($R_{\Theta CS}$), and the heatsink to ambient ($R_{\Theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 24 illustrates these thermal resistances for a SOT223 package mounted in a JEDEC low-K board.

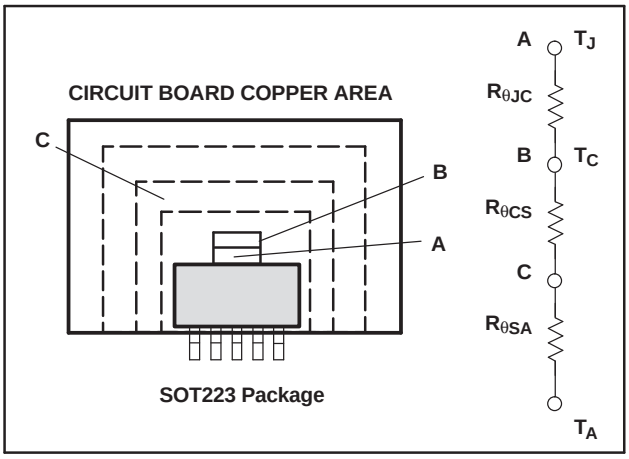


Figure 24. Thermal Resistances

Equation 5 summarizes the computation:

$$T_J = T_A + P_D\text{max} \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (5)$$

The $R_{\Theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\Theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\Theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\Theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\Theta CS}$ of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\Theta JA}$). This $R_{\Theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 5 simplifies into Equation 6:

$$T_J = T_A + P_D max \times R_{\theta JA} \quad (6)$$

Rearranging Equation 6 gives Equation 7:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \quad (7)$$

Using Equation 6 and the computer model generated curves shown in Figure 25, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

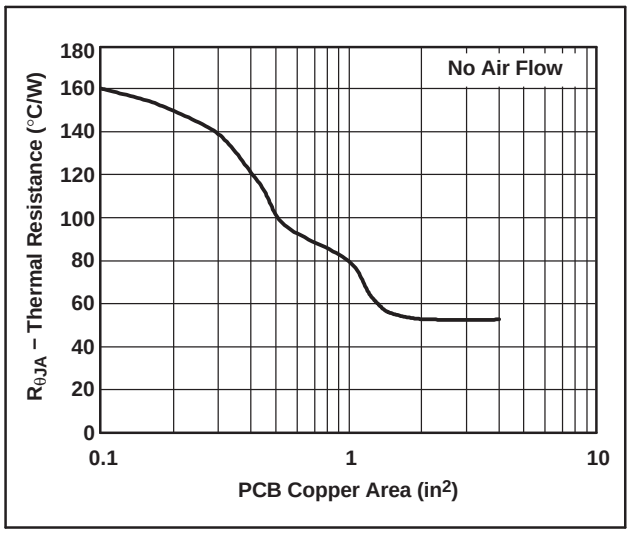


Figure 25. SOT223 Thermal Resistance vs PCB Copper Area

SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface-mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS79425 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is Equation 8:

$$P_D max = (3.3 - 2.5)V \times 1A = 800mW \quad (8)$$

Substituting $T_J max$ for T_J into Equation 4 gives Equation 9:

$$R_{\theta JA} max = (125 - 55)°C/800mW = 87.5°C/W \quad (9)$$

From Figure 25, $R_{\theta JA}$ vs PCB Copper Area, the ground plane needs to be 0.55 in^2 for the part to dissipate 800 mW. The operating environment used to construct Figure 25 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

From the data in Figure 25 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed, as shown in Figure 26.

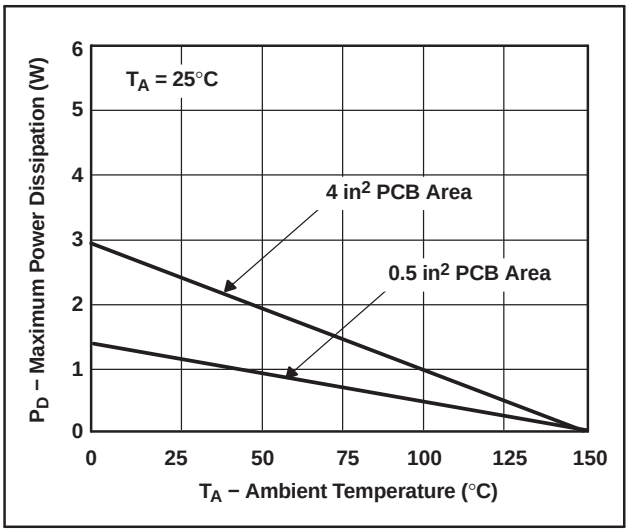


Figure 26. SOT223 Maximum Power Dissipation vs Ambient Temperature

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79401DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79401	Samples
TPS79401DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79401	Samples
TPS79401DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AXL	Samples
TPS79401DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AXL	Samples
TPS79418DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79418	Samples
TPS79418DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79418	Samples
TPS79418DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXM	Samples
TPS79418DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXM	Samples
TPS79425DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79425	Samples
TPS79425DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79425	Samples
TPS79425DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYB	Samples
TPS79425DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYB	Samples
TPS79428DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79428	Samples
TPS79428DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79428	Samples
TPS79428DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYC	Samples
TPS79430DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79430	Samples
TPS79430DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79430	Samples
TPS79430DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYD	Samples
TPS79430DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYD	Samples
TPS79433DCQ	ACTIVE	SOT-223	DCQ	6	78	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79433	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79433DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS79433	Samples
TPS79433DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYE	Samples
TPS79433DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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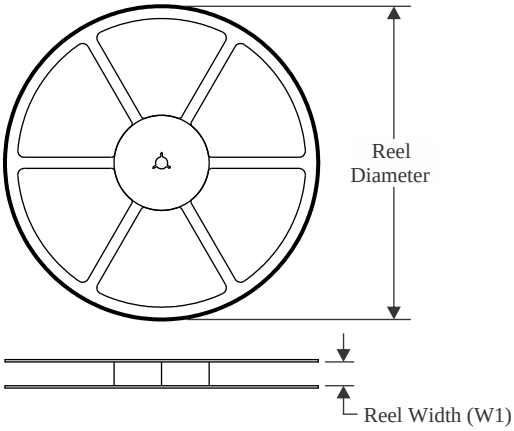
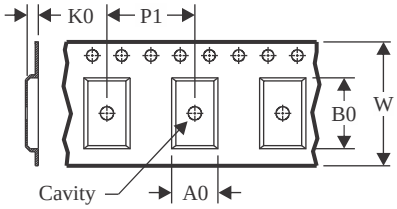
TAPE AND REEL INFORMATION

REEL DIMENSIONS

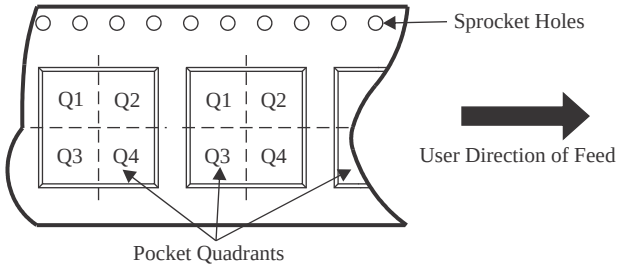


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

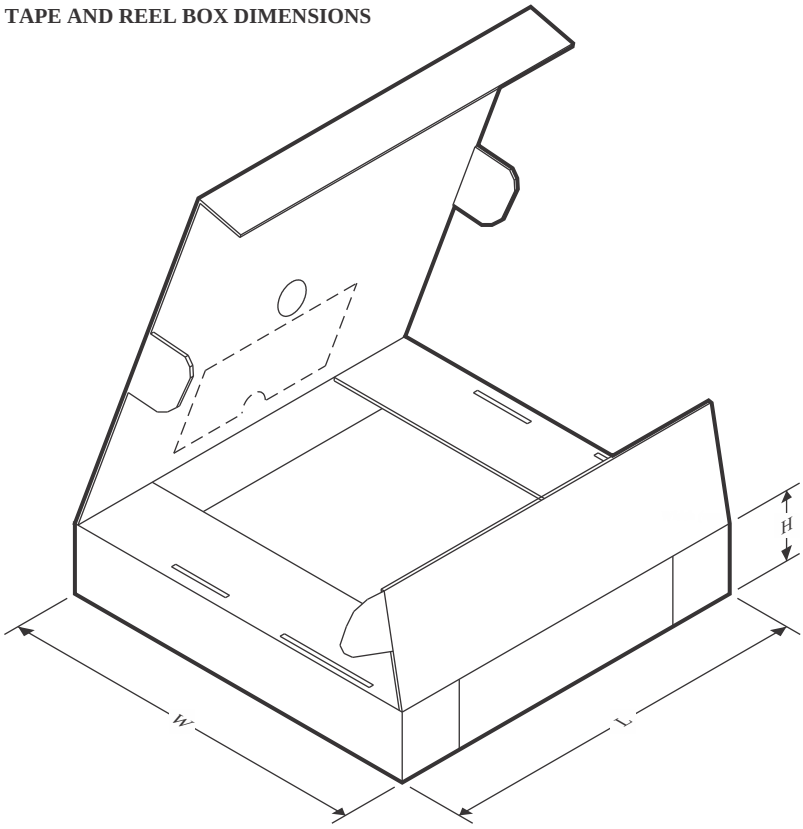
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79401DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79418DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79418DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79418DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79425DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79425DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79425DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79428DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79428DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79430DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79430DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79430DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79433DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS79433DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS79433DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

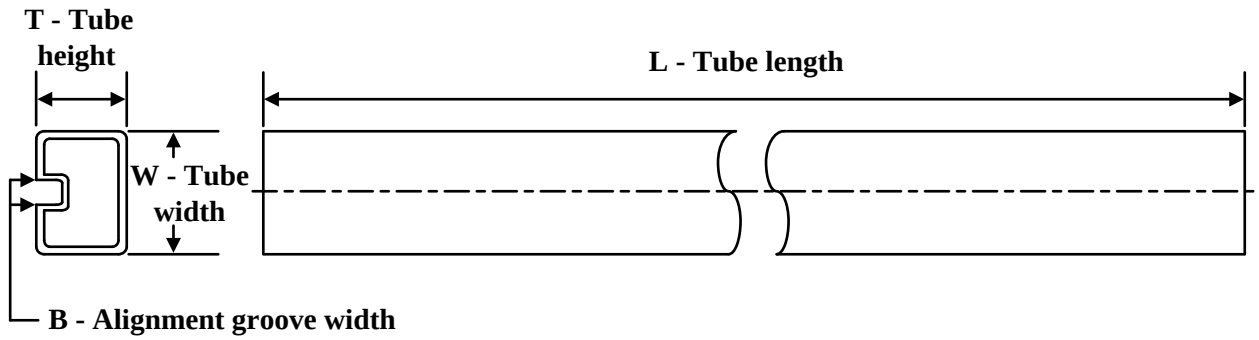
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79401DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79418DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS79418DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS79418DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0
TPS79425DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS79425DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS79425DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0
TPS79428DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS79428DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0
TPS79430DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79430DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS79430DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0
TPS79433DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS79433DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS79433DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

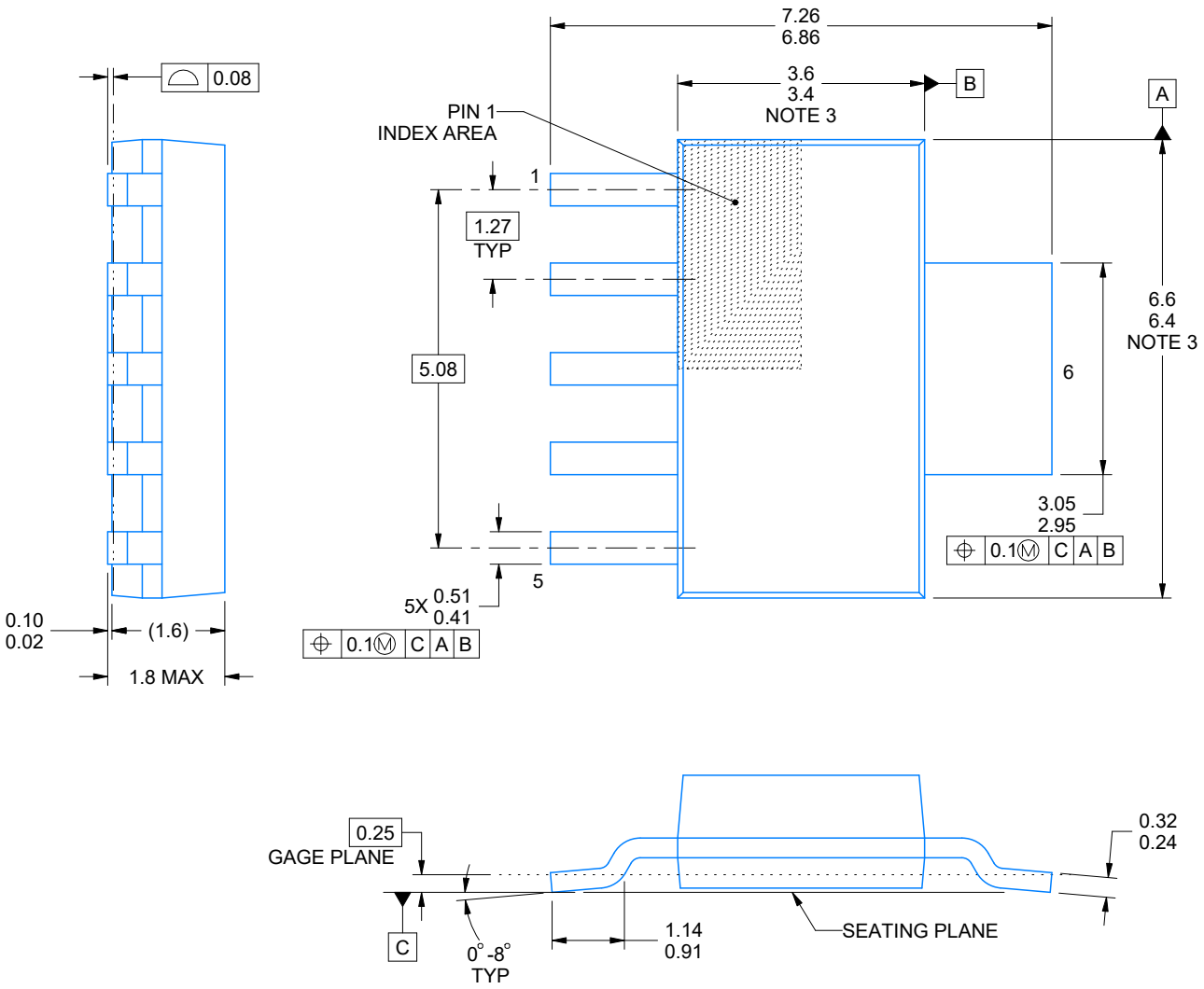
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS79401DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79418DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79425DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79428DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79430DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68
TPS79433DCQ	DCQ	SOT-223	6	78	532.13	8.63	3.6	3.68

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

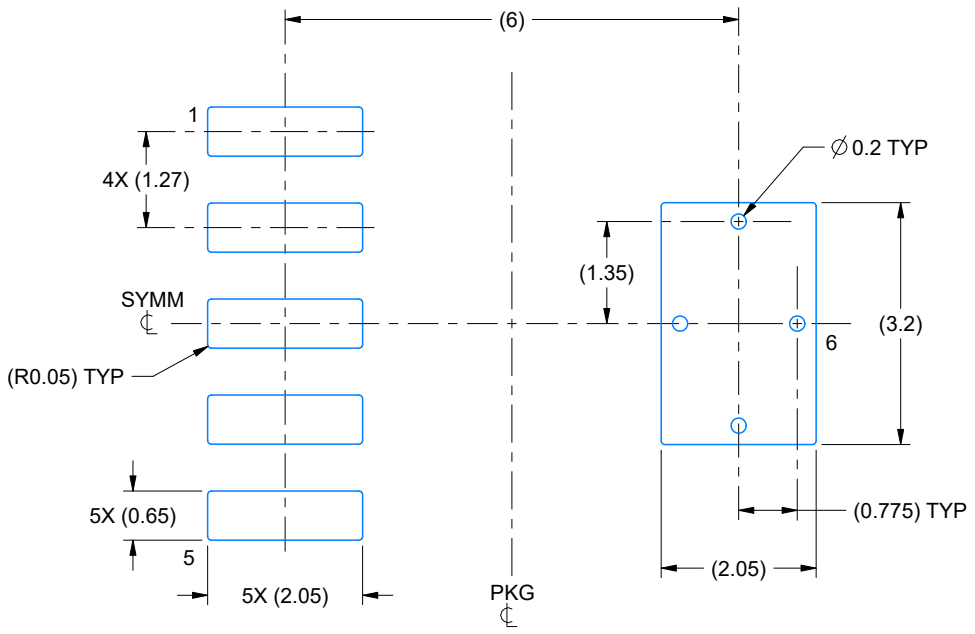
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

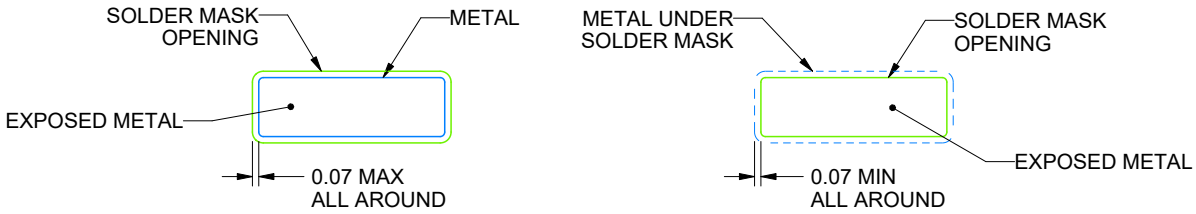
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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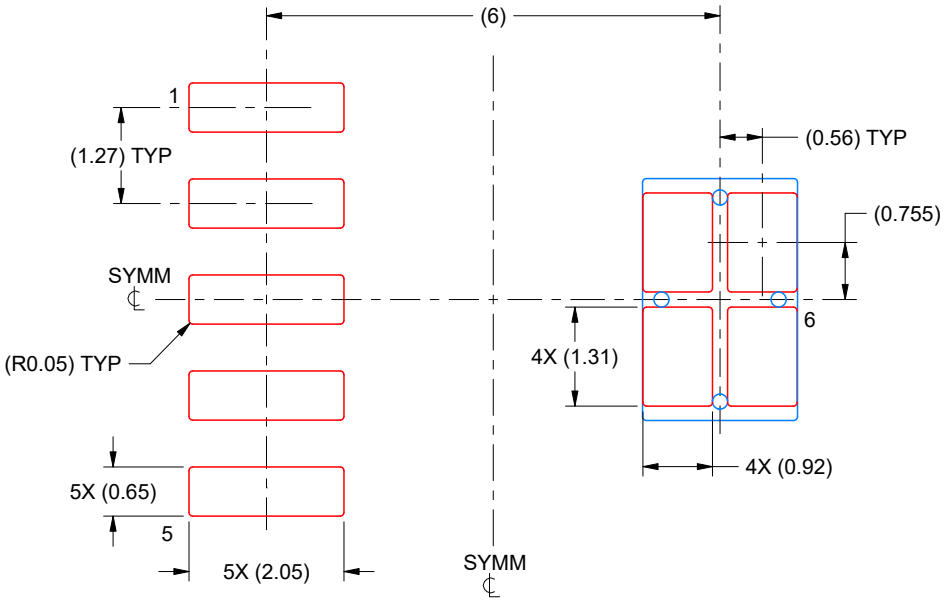
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

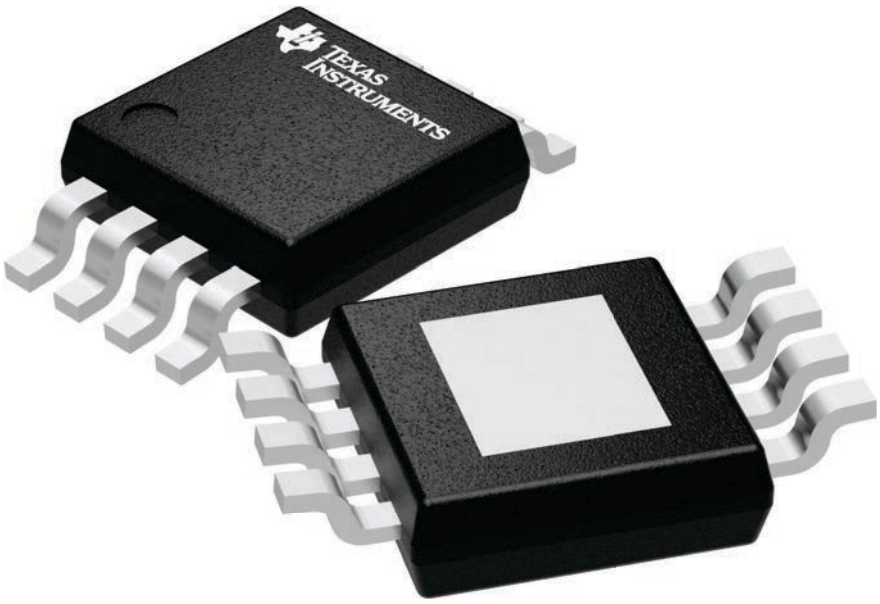
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

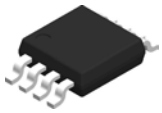
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

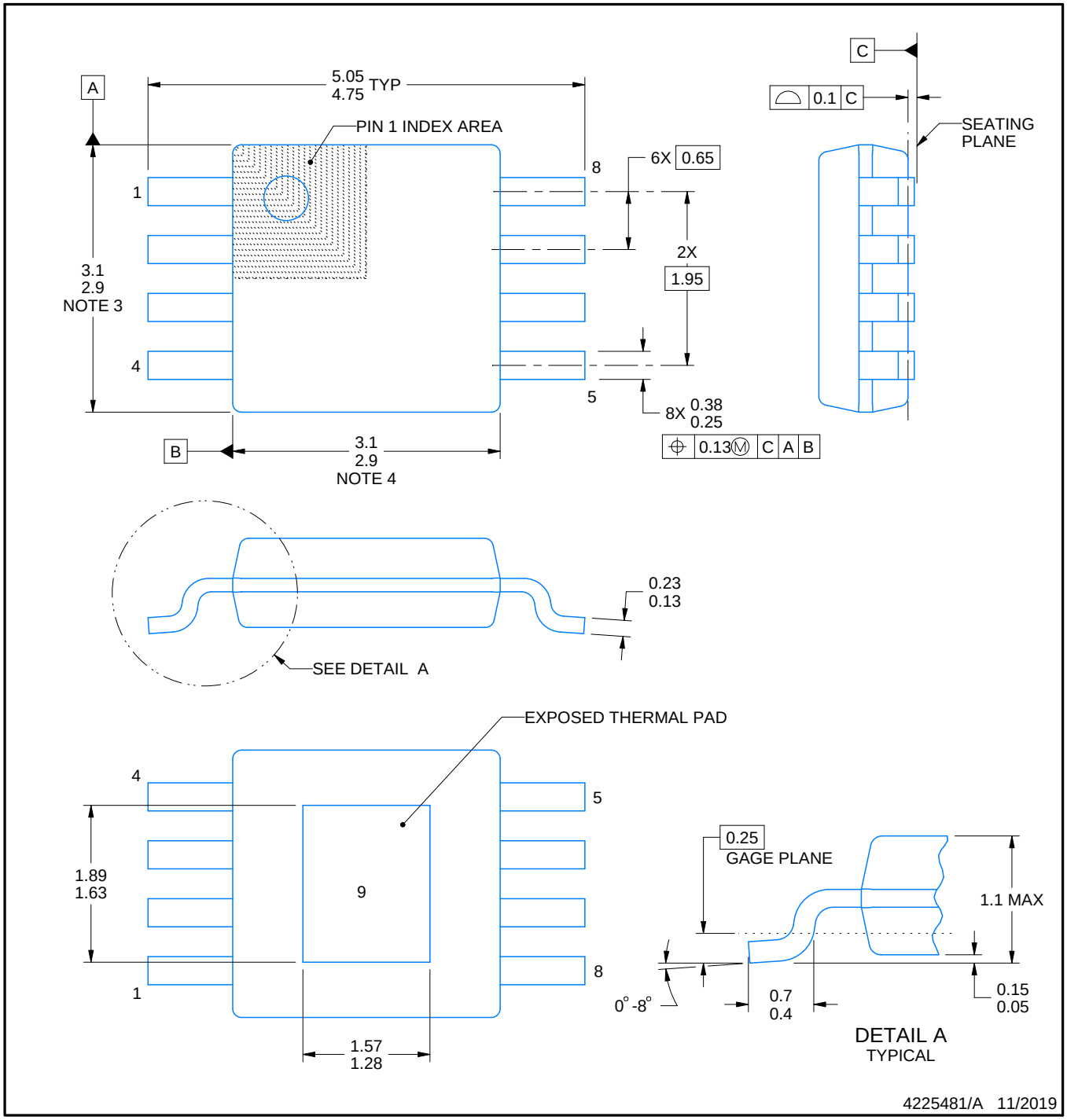
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

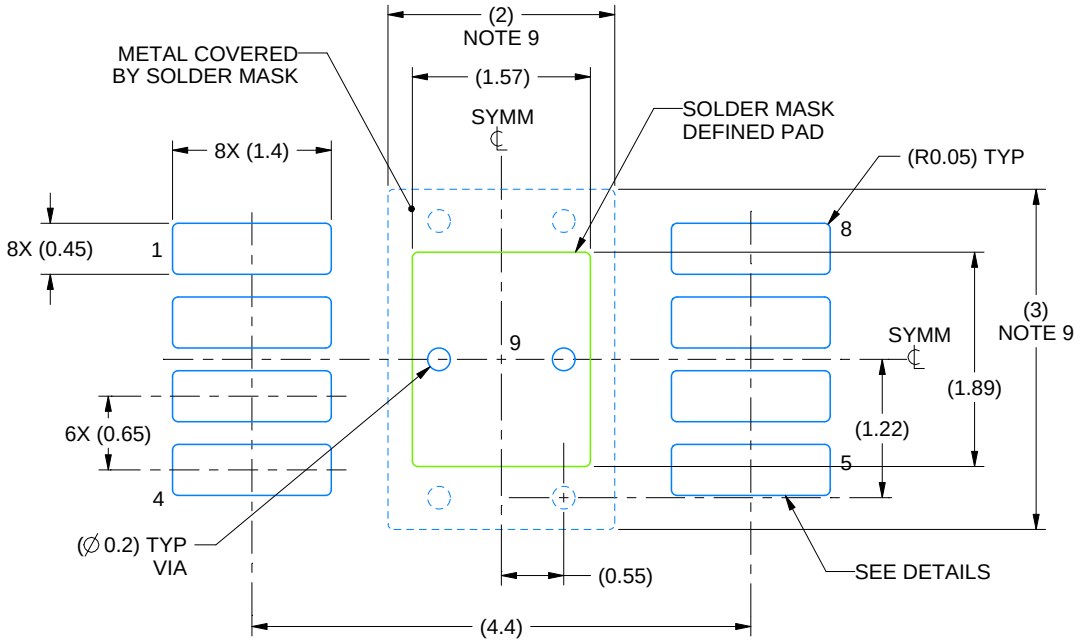
SMALL OUTLINE PACKAGE



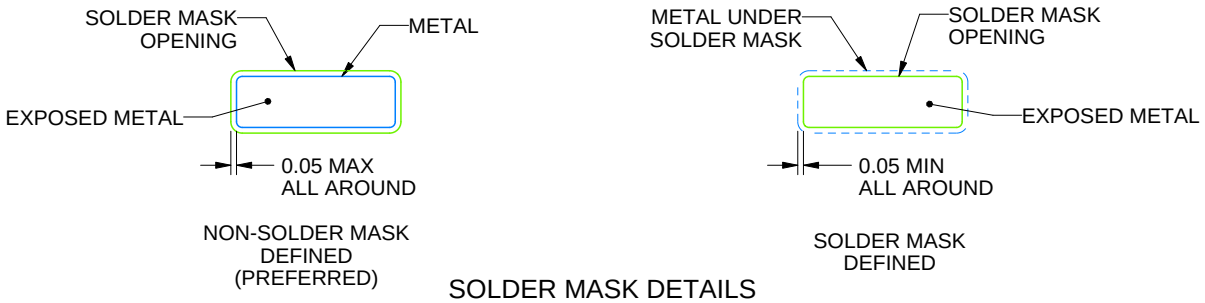
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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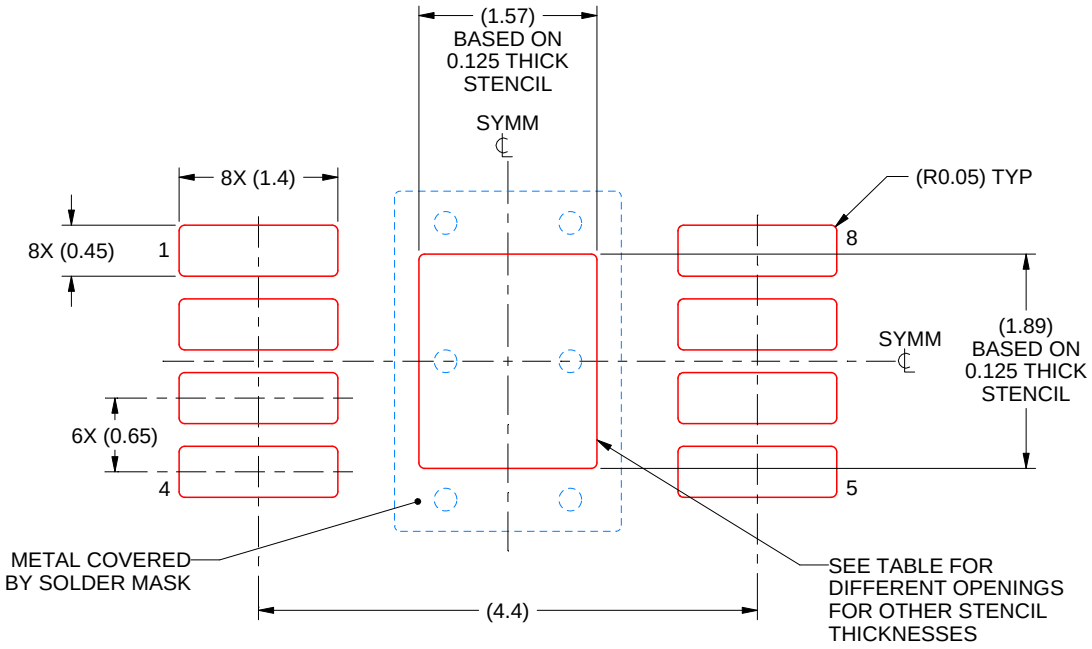
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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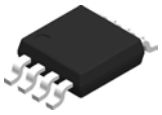
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

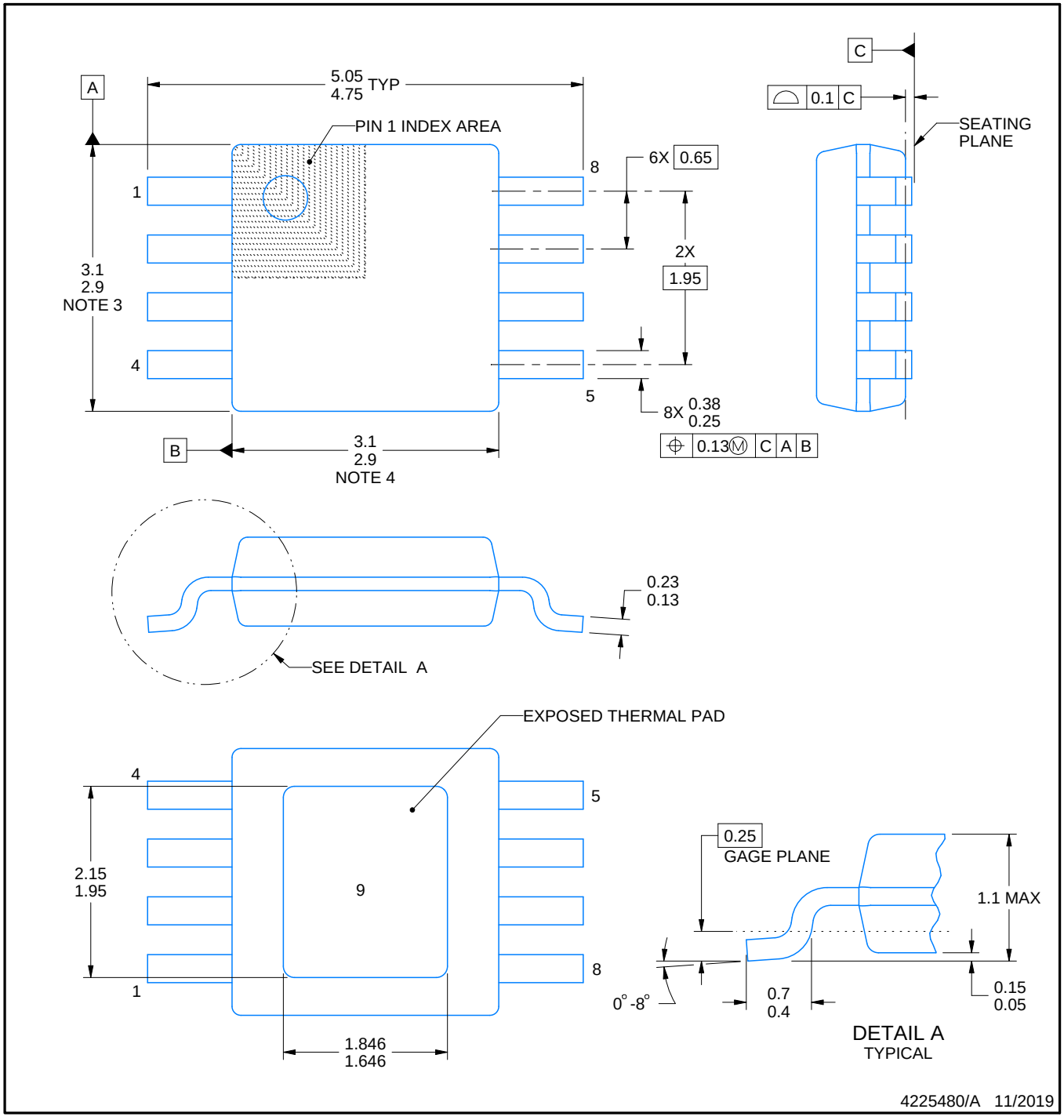
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

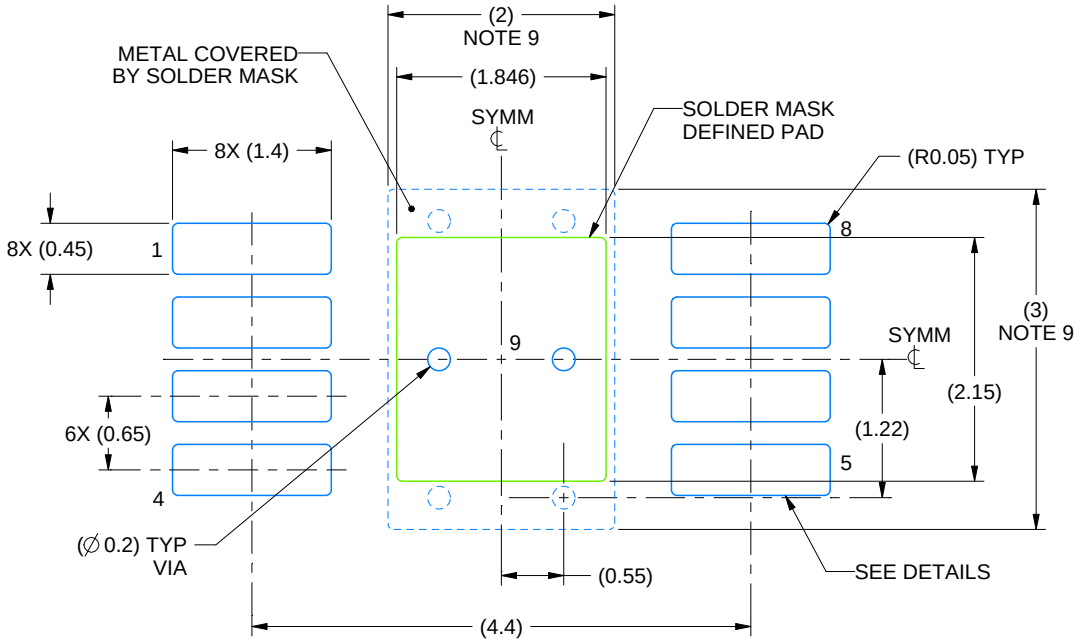
SMALL OUTLINE PACKAGE



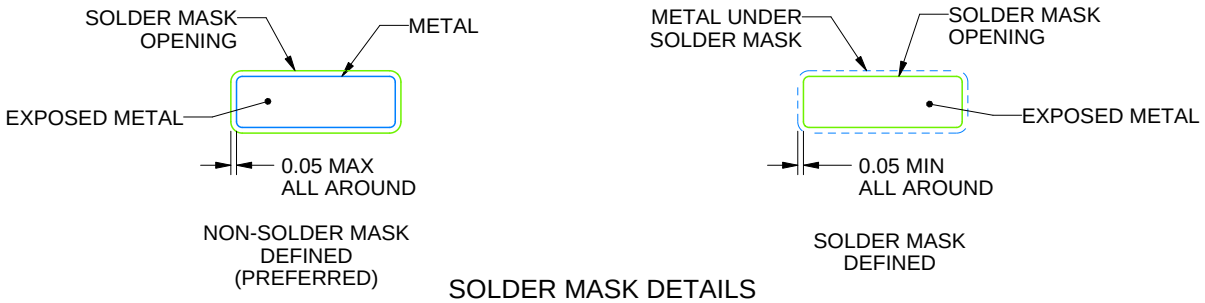
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

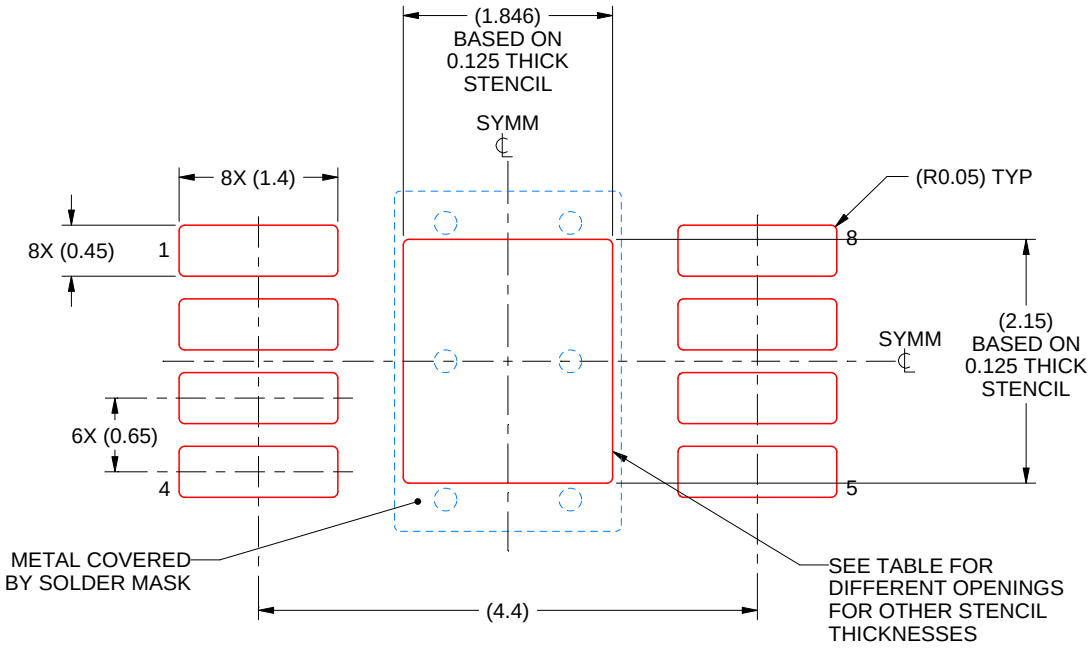


SOLDER MASK DETAILS

4225480/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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