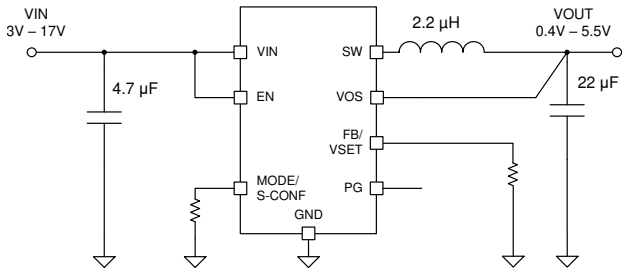
TPS629210E 1-A, 3-V to 17-V, –55°C to +150°C Low I_Q Buck Converter

1 Features

- Extended operating temperature performance
  - –55°C to 150°C operating junction temperature range
- High-efficiency DCS-Control topology
  - Internal compensation
  - Seamless PWM/PFM transition
- 4-µA typical low quiescent current
- Output current up to 1 A
- R_{DSON}: 250-mΩ high side, 85-mΩ low side
- Output voltage accuracy of ±1%
- Configurable output voltage options:
  - V_{FB} external divider: 0.6 V to 5.5 V
  - VSET internal divider:
    - 18 options between 0.4 V and 5.5 V
- Flexibility through the MODE/S-CONF pin
  - 2.5-MHz or 1.0-MHz switching frequency
  - Forced PWM or auto (PFM) power save mode with dynamic mode change option
  - Output discharge on/off
- No external bootstrap capacitor required
- Overcurrent and overtemperature protection
- 100% duty cycle mode
- Precise enable input
- Power-good output
- Pin-to-pin compatible with the TPS629210, TPS629206, and TPS629203 devices
- 0.5-mm pitch, 8-pin SOT-5X3 package

2 Applications

- Aerospace and defense
  - Aircraft cockpit display
  - Ruggedized communication
  - Smart munitions
- Industrial transport



Simplified Schematic

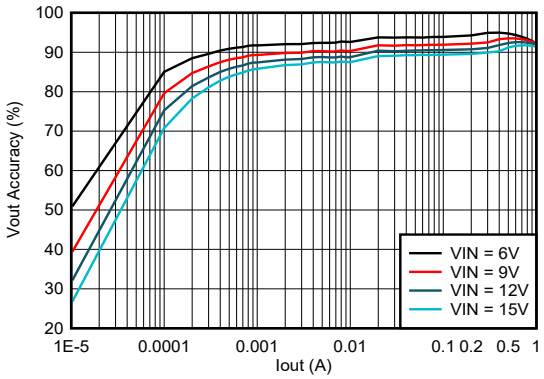
3 Description

The TPS629210E device is a highly efficient, small, and highly flexible synchronous step-down DC-DC converter that easy to use. A wide 3-V to 17-V input voltage range supports a wide variety of systems powered from either 12-V, 5-V, or 3.3-V supply rails, or single-cell or multi-cell Li-Ion batteries. The TPS629210E can be configured to run at either 2.5 MHz or 1 MHz in a forced PWM mode or a variable frequency (auto PFM) mode. In auto PFM mode, the device automatically transitions to power save mode at light loads to maintain high efficiency. The low 4-µA typical quiescent current also provides high efficiency down to the smallest loads. TI's automatic efficiency enhancement (AEE) mode holds a high conversion efficiency through the whole operation range without the need of using different inductors by automatically adjusting the switching frequency based on input and output voltages. In addition to selecting the switching frequency behavior, the MODE/S-CONF input pin can also be used to select between different combinations of external and internal feedback dividers and enabling and disabling the output voltage discharge capability. In the internal feedback configuration, a resistor between the FB/VSET pin and GND can be used to select between 18 different output voltage options (see Table 8-2).

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS629210E	SOT-5X3 (8)	1.60 mm × 2.10 mm (including pins)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency vs Output Current
V_{OUT} = 3.3 V at 1.0-MHz Auto PFM/PWM

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial Release

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5 Device Comparison Table

Device Number	Output Current	Input Voltage	Operating Temperature Range	Switching Frequency	PWM Mode	V_O Adjust
TPS629203	0 A–0.3 A	3 V–17 V	–40°C to 125°C	Selectable 1 MHz or 2.5 MHz options	Selectable auto PWM/PFM or forced PWM	Externally programmable or 18 internal options
TPS629206	0 A–0.6 A					
TPS629210	0 A–1 A					
TPS629210E	0 A–1 A		–55°C to 150°C			

6 Pin Configuration and Functions

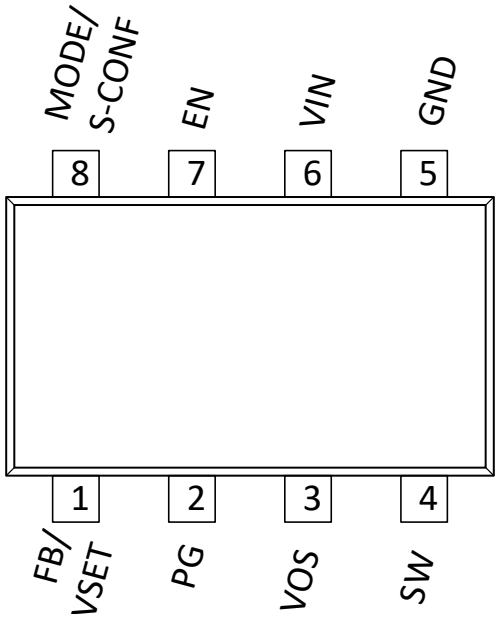

Figure 6-1. TPS629210E 8-Pin DRL SOT-5X3 Pinout

Table 6-1. Pin Functions

Pin		I/O	Description
Name	NO.		
FB/VSET	1	I	Dependent upon device configuration (see Section 8.3.1) • FB: Voltage feedback input. Connect a resistive output voltage divider to this pin. • VSET: Output voltage setting pin. Connect a resistor to GND to choose the output voltage according to Table 8-2.
PG	2	O	Open-drain power-good output
VOS	3	I	Output voltage sense pin. Connect directly to the positive pin of the output capacitor.
SW	4		Switch pin of the converter. Connected to the internal power switches
GND	5		Ground pin
VIN	6	I	Power supply input. Make sure the input capacitor is connected as close as possible between the VIN pin and GND.
EN	7	I	Enable/disable pin including a threshold comparator. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
MODE/S-CONF	8	I	Device mode selection (auto PFM/PWM or forced PWM operation) and Smart-CONFIG pin. Connect a resistor to configure the device according to Table 8-1.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PG, MODE/S-CONF	–0.3	18	V
Voltage(2)	SW(3)	–0.3	V_{IN} + 0.3	V
Voltage(2)	SW (AC, less than 10 ns)(3)	–3.0	23	V
Voltage(2)	FB/VSET, VOS	–0.3	6	V
Current	PG		10	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	3.0		17	V
V_O	Output voltage range	0.4		5.5	V
C_I	Effective input capacitance	3	4.7		µF
C_O	Effective output capacitance(1)	10	22	100	µF
L	Output inductance(2)	1.0(3)	2.2	4.7(4)	µH
I_{OUT}	Output current	0		1	A
I_{SINK_PG}	Sink current at the PG pin			1	mA
T_J	Junction temperature (5)	–55		150	°C

(1) This is for capacitors directly at the output of the device. More capacitance is allowed if there is a series resistance associated to the capacitor.
(2) Nominal inductance value
(3) Not recommended for 1-MHz operation
(4) Larger values of inductance can be used to reduce the ripple current, but they can have a negative impact on efficiency and the overall transient response.
(5) Operating lifetime is derated at junction temperatures greater than 150°C.

7.4 Thermal Information

THERMAL METRIC(1)		SOT-5X3 (8)		UNIT
		JEDEC PCB	TPS6292xx EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	n/a	°C/W

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THERMAL METRIC(1)		SOT-5X3 (8)		UNIT
		JEDEC PCB	TPS6292xx EVM	
Ψ_{JB}	Junction-to-board characterization parameter	20	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{IN} = 3 V to 17 V, T_J = –55°C to +150°C, typical values at V_I = 12 V and T_A = 25°C,unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current (power save mode)	I_{OUT} = 0 mA, device not switching		4		µA
$I_{Q;PWM}$	Operating quiescent current (PWM mode)	V_{IN} = 12 V, V_{OUT} = 1.2 V; I_{OUT} = 0 mA, device switching		5		mA
I_{SD}	Shutdown current into the VIN pin	EN = 0 V		0.25	3	µA
V_{UVLO}	Undervoltage lockout	V_{IN} rising	2.85	2.95	3.0	V
	Undervoltage lockout	V_{IN} falling	2.65	2.75	2.85	V
V_{UVLO}	Undervoltage lockout hysteresis			200		mV
CONTROL AND INTERFACE						
I_{LKG}	EN input leakage current	EN = V_{IN}		3	300	nA
$V_{IH;MODE}$	High-level input voltage at the MODE/S-CONF pin		1.0			V
$V_{IL;MODE}$	Low-level input voltage at the MODE/S-CONF pin				0.15	V
V_{IH}	High-level input voltage at the EN pin		0.97	1.0	1.03	V
V_{IL}	Low-level input voltage at the EN pin		0.87	0.9	0.93	V
V_{PG}	Power-good threshold	V_{FB} rising, referenced to V_{FB} nominal	93%	96%	99%	
		V_{FB} falling, referenced to V_{FB} nominal	89%	93%	96%	
V_{PG_HYS}	Power-good threshold hysteresis	Hysteresis		3%		
$t_{PG,DLY}$	Power-good delay time			32		µs
$t_{PG,DLY}$	Power-good pulldown resistance			10		Ω
$V_{PG,OL}$	Low-level output voltage at the PG pin	I_{SINK} = 1 mA			0.1	V
$I_{PG,LKG}$	Input leakage current into the PG pin	V_{PG} = 5 V		0.01	1	µA
POWER SWITCHES						
$R_{DS;ON}$	High-side FET on resistance			250		mΩ
	Low-side FET on resistance			85		
I_{LIM}	High-side FET current limit		1.5	1.8	2.1	A
	Low-side FET current limit		1.3	1.6	1.9	A
$I_{LIM;SINK}$	Low-side FET sink current limit		0.8	1	1.2	A
T_{SD}	Thermal shutdown threshold	T_J rising		170		°C
	Thermal shutdown hysteresis	T_J falling		20		
f_{SW}	Switching frequency	2.5-MHz selection (FPWM mode)		2.5		MHz
f_{SW}	Switching frequency	1.0-MHz selection (FPWM mode)		1.0		MHz
$T_{ON(MIN)}$	Minimum on time			40		ns
$I_{LKG;SW}$	Leakage current into the SW pin	EN = 0 V, V_{SW} = V_{OS} = 5.5 V		0.1	5	µA
OUTPUT						
V_O	Output voltage regulation	VSET configuration selected, T_J = 25°C	–0.75%		+0.75%	

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7.5 Electrical Characteristics (continued)

V_{IN} = 3 V to 17 V, T_J = –55°C to +150°C, typical values at V_I = 12 V and T_A = 25°C,unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage regulation	VSET option selected, –55°C ≤ T_J ≤ 150°C	–1.5%		+1%	
V_{FB}	Feedback regulation voltage	Adjustable configuration selected		0.6		V
V_{FB}	Feedback voltage regulation	FB option selected, T_J = 25°C	–0.5 %		+ 0.5%	
V_{FB}	Feedback voltage regulation	FB option selected, –55°C ≤ T_J ≤ 150°C	–1.5%		+0.5%	
I_{FB}	Input leakage current into the FB pin	Adjustable configuration, V_{FB} = 0.6 V		1	100	nA
T_{delay}	Start-up delay time	I_O = 0 mA, time from EN rising edge until start switching, external FB configuration selected		700	1750	µs
T_{delay}	Start-up delay time	I_O = 0 mA, time from EN rising edge until start switching, VSET configuration selected		1000	2000	µs
T_{SS}	Soft-start time	I_O = 0 mA after T_{delay}, from first switching pulse until target V_O		600	700	µs
R_{DISCH}	Active discharge resistance	Discharge = ON - option selected, EN = LOW		7.5	20	Ω

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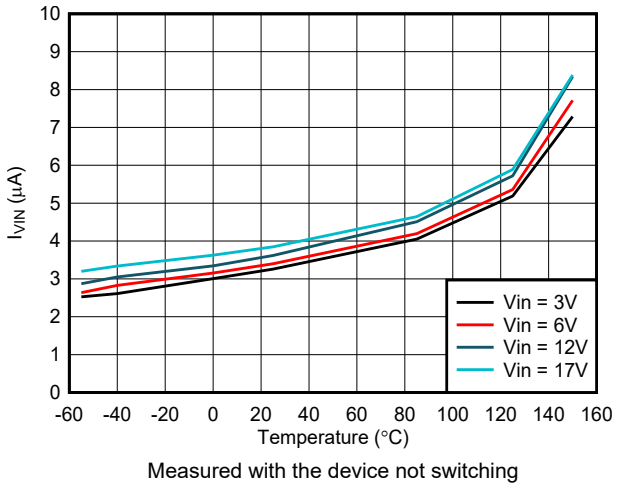
7.6 Typical Characteristics



Measured with the device not switching

Figure 7-1. Typical Quiescent Current vs Temperature

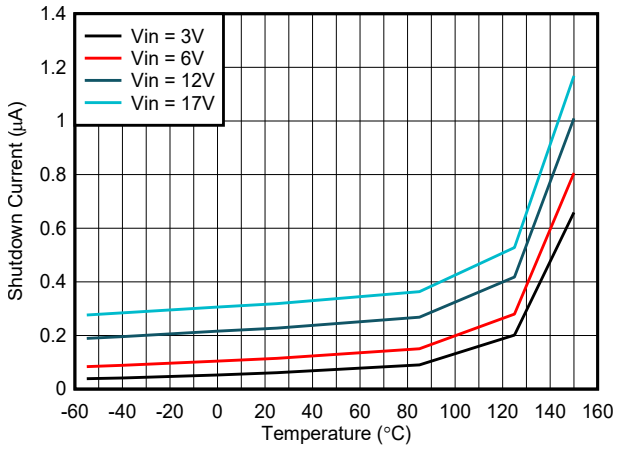


Figure 7-2. Typical Shutdown Current vs Temperature

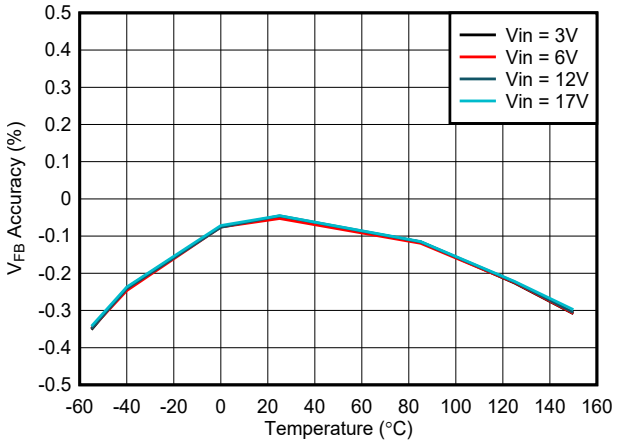
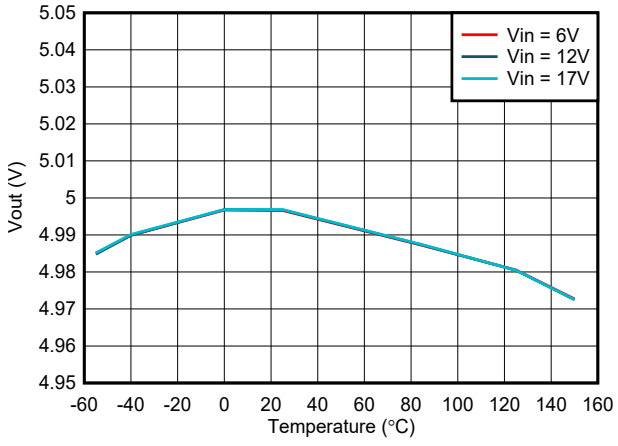
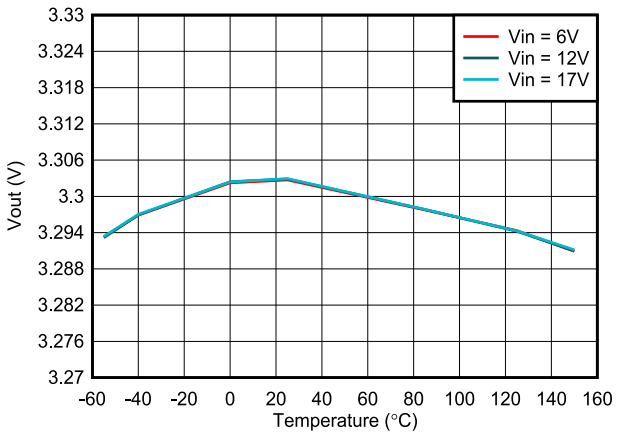


Figure 7-3. Output Voltage Accuracy – External Feedback



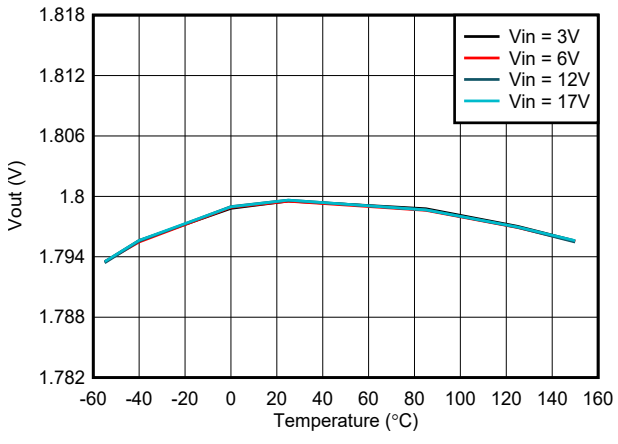
V_{OUT} = 5.0 V

Figure 7-4. Output Voltage Accuracy – VSET Selected



V_{OUT} = 3.3 V

Figure 7-5. Output Voltage Accuracy – VSET Selected



V_{OUT} = 1.8 V

Figure 7-6. Output Voltage Accuracy – VSET Selected

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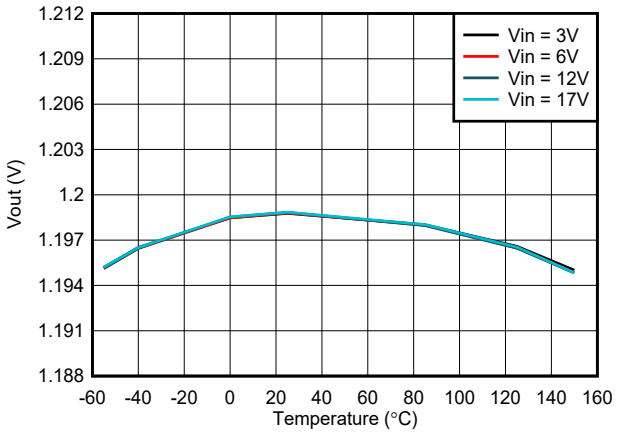
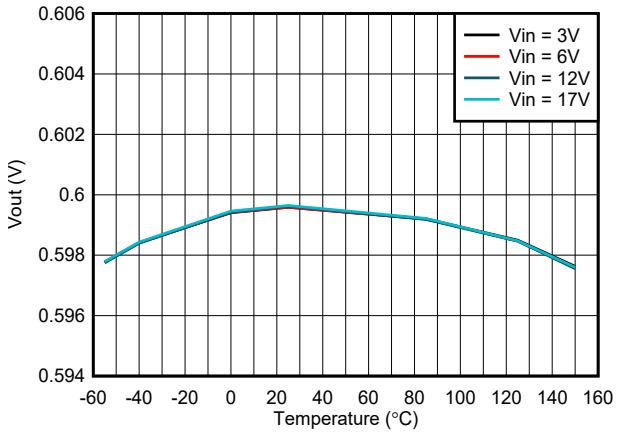
7.6 Typical Characteristics (continued)



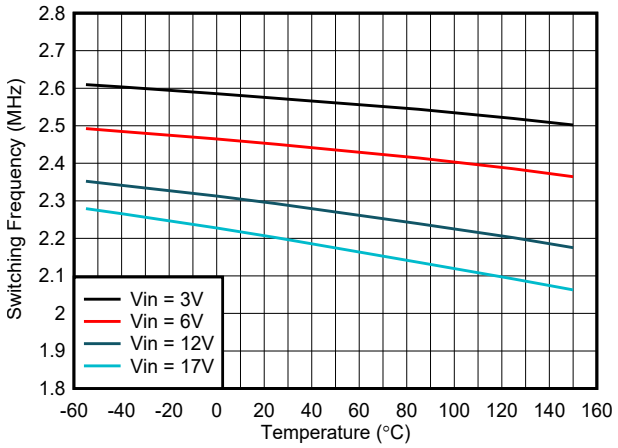
V_{OUT} = 1.2 V

Figure 7-7. Output Voltage Accuracy – VSET Selected



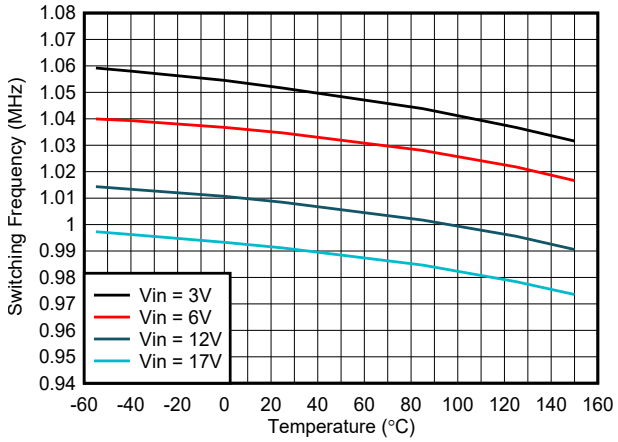
V_{OUT} = 0.6 V

Figure 7-8. Output Voltage Accuracy – VSET Selected



V_{OUT} = 1.2 V F_{SW} = 2.5 MHz I_{OUT} = 0 A
FPWM

Figure 7-9. Switching Frequency vs Temperature



V_{OUT} = 1.2 V F_{sw} = 1.0 MHz I_{OUT} = 0 A
FPWM

Figure 7-10. Switching Frequency vs Temperature

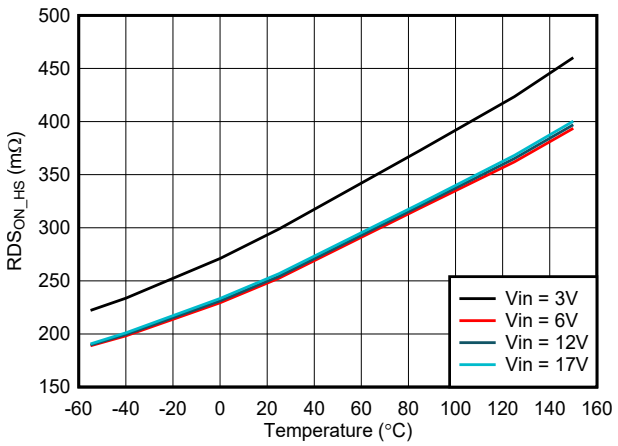


Figure 7-11. High-Side RDS_{ON} vs Temperature

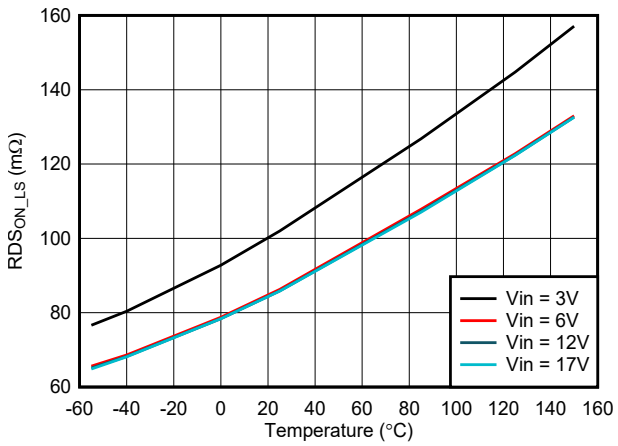


Figure 7-12. Low-Side RDS_{ON} vs Temperature

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7.6 Typical Characteristics (continued)

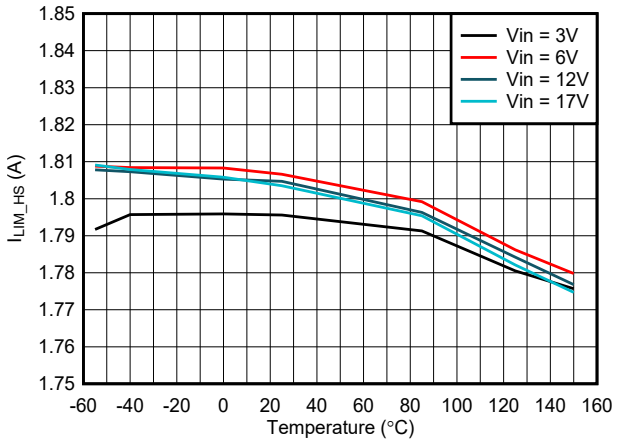

Figure 7-13. High-Side I_{LIM} vs Temperature

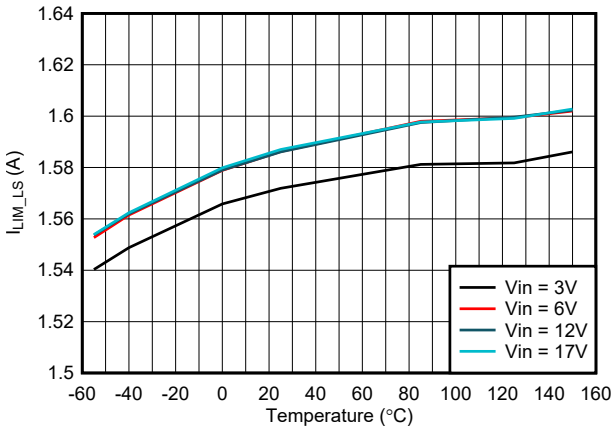

Figure 7-14. Low-Side I_{LIM} vs Temperature

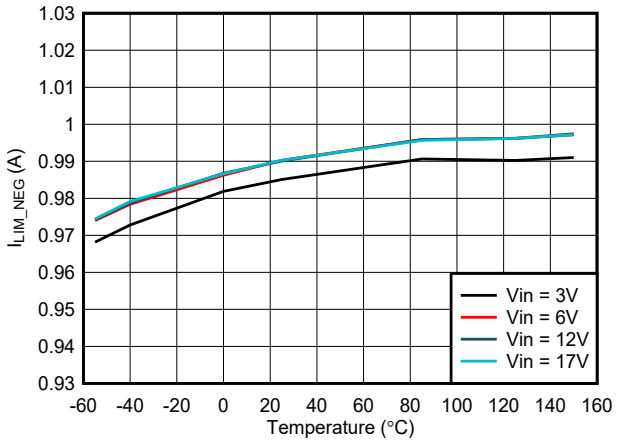

Figure 7-15. Low-Side I_{NEG} vs Temperature

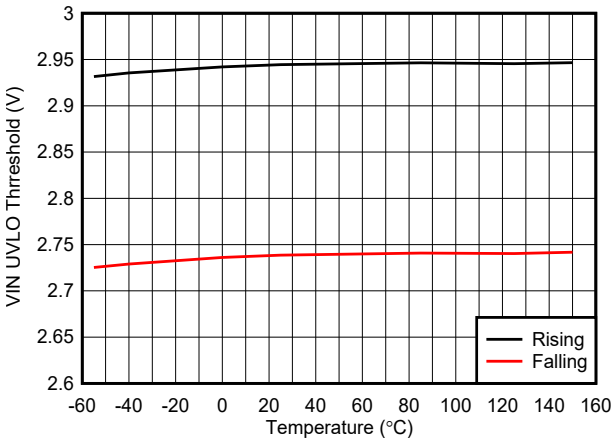

Figure 7-16. V_{IN} UVLO Thresholds vs Temperature

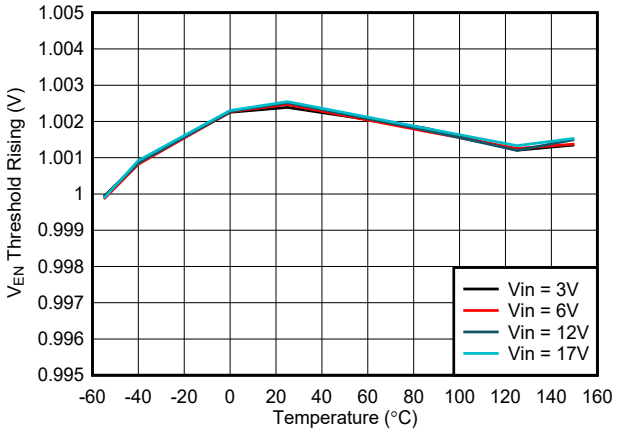

Figure 7-17. Precision Enable Threshold vs Temperature

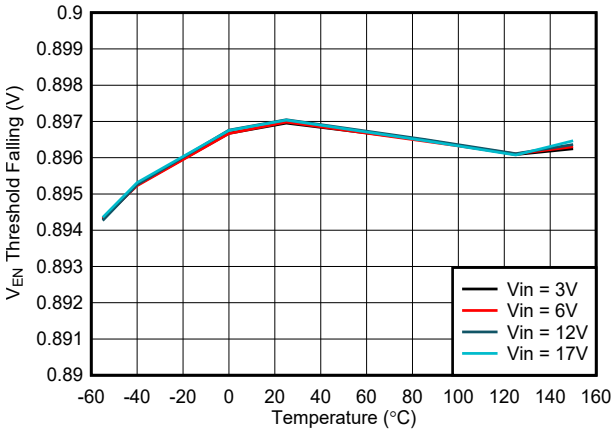

Figure 7-18. Precision Enable Threshold vs Temperature

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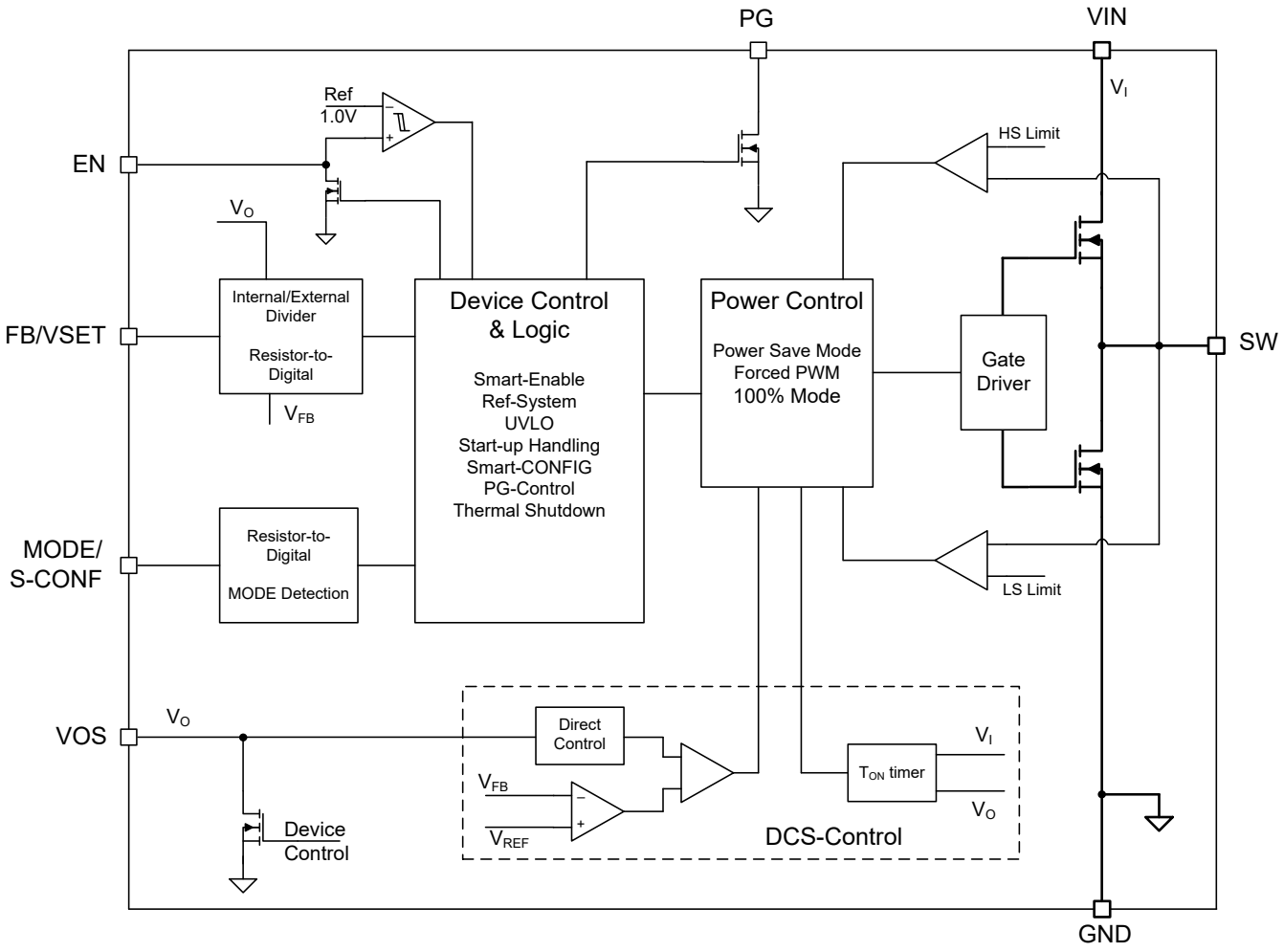
8 Detailed Description

8.1 Overview

The TPS629210E synchronous switched mode power converter is based on DCS-Control (Direct Control with Seamless Transition into power save mode), an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Mode Selection and Device Configuration (MODE/S-CONF Pin)

The MODE/S-CONF pin is an input with two functions. It can be used to customize the device behavior in two ways:

- Select the device mode (forced PWM or auto PFM/PWM operation) traditionally with a HIGH or LOW level.
- Select the device configuration (switching frequency, internal and external feedback, output discharge, and PFM/PWM mode) by connecting a single resistor to this pin.

The device interprets this pin during its start-up sequence after the internal OTP readout and before it starts switching in soft start. If the device reads a HIGH or LOW level, dynamic mode change is active and PFM/PWM mode can be changed during operation. If the device reads a resistor value, there is no further interpretation during operation and the device mode or other configurations cannot be changed afterward.

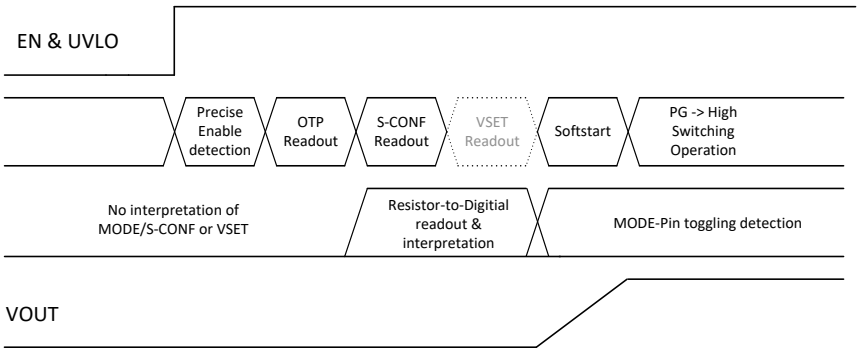

Figure 8-1. Interpretation of S-CONF and VSET Flow

Table 8-1. Smart-CONFIG Setting Table

#	M ODE/S-CONF Level Or Resistor Value [Ω] (1)	FB/VSET Pin	F_{SW} (MHz)	Output Discharge	Mode (Auto Or Forced PWM)	Dynamic Mode Change
	Setting Options by Level					
1	GND	external FB	up to 2.5(2)	yes	Auto PFM/PWM with AEE	Active
2	HIGH (> 1.8 V)	external FB	2.5	yes	Forced PWM	
	Setting Options by Resistor					
3	7.50 k	external FB	up to 2.5(2)	no	Auto PFM/PWM with AEE	not active
4	9.31 k	external FB	2.5	no	Forced PWM	
5	11.50 k	external FB	1	yes	Auto PFM/PWM	
6	14.30 k	external FB	1	yes	Forced PWM	
7	17.80 k	external FB	1	no	Auto PFM/PWM	
8	22.10 k	external FB	1	no	Forced PWM	
9	27.40 k	VSET	up to 2.5(2)	yes	Auto PFM/PWM with AEE	
10	34.00 k	VSET	2.5	yes	Forced PWM	
11	42.20 k	VSET	up to 2.5(2)	no	Auto PFM/PWM with AEE	
12	52.30 k	VSET	2.5	no	Forced PWM	
13	64.90 k	VSET	1	yes	Auto PFM/PWM	
14	80.60 k	VSET	1	yes	Forced PWM	
15	100.00 k	VSET	1	no	Auto PFM/PWM	
16	124.00 k	VSET	1	no	Forced PWM	

(1) E96 Resistor Series, 1% accuracy, temperature coefficient better or equal than ±200 ppm/°C
(2) F_{SW} varies based on V_{IN} and V_{OUT}. See Section 8.4.3 for more details.

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8.3.2 Adjustable V_O Operation (External Voltage Divider)

If the device is configured to operate in classical adjustable V_O operation, the FB/VSET pin is used as the feedback pin and needs to sense V_O through an external divider network. shows the typical schematic for this configuration.

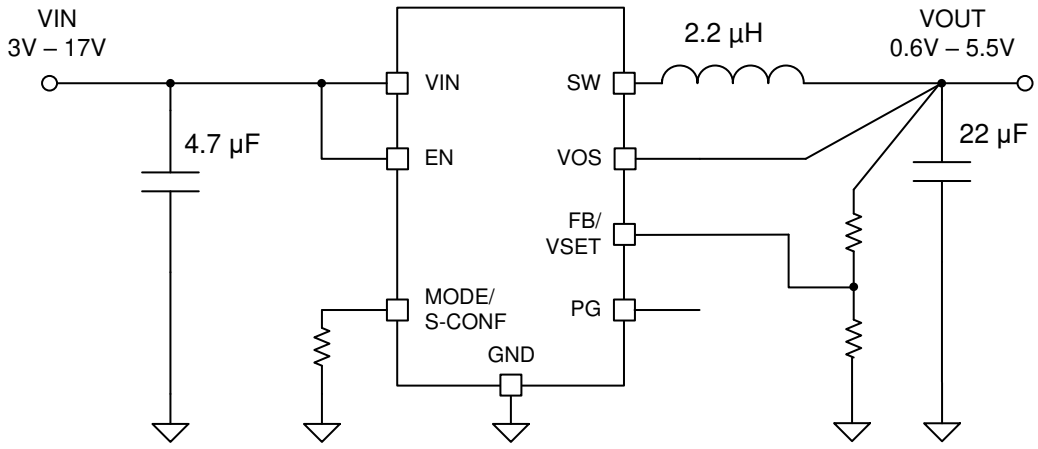

Figure 8-2. Adjustable V_O Operation Schematic

8.3.3 Selectable V_O Operation (VSET and Internal Voltage Divider)

If the device is configured to VSET operation, the device interprets the VSET pin value following the MODE/S-CONF readout (see). There is no further interpretation of the VSET pin during operation and the output voltage cannot be changed afterward without toggling the EN pin.

shows the typical schematic for this configuration, where V_O is directly sensed at the VOS pin of the device. V_O is sensed only through the VOS pin by an internal resistor divider. The target V_O is programmed by an external resistor connected between VSET and GND (see Table 8-2).

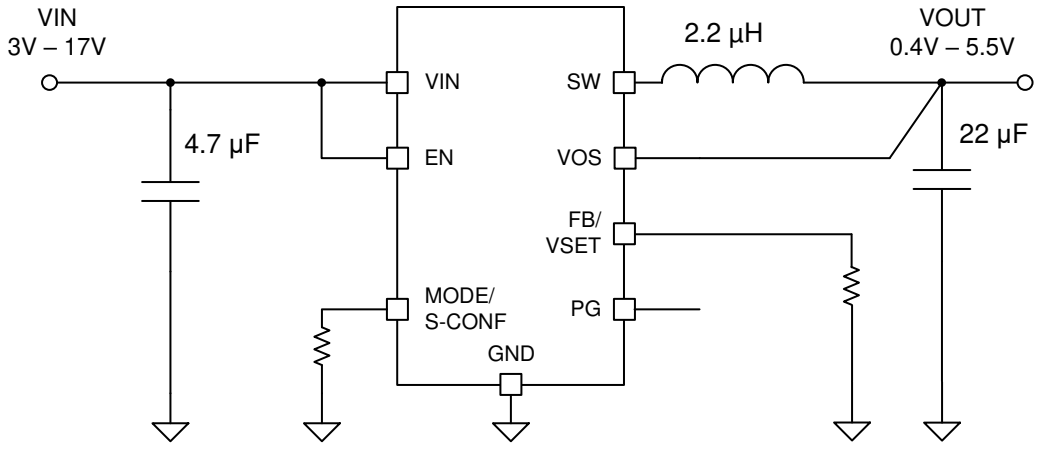

Figure 8-3. Selectable V_O Operation Schematic

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Table 8-2. VSET Selection Table

VSET #	Resistor Value [Ω](1)	Target V_O [V]
1	GND	1.2
2	4.87 k	0.4
3	6.04 k	0.6
4	7.50 k	0.8
5	9.31 k	0.85
6	11.50 k	1.0
7	14.30 k	1.1
8	17.80 k	1.25
9	22.10 k	1.3
10	27.40 k	1.35
11	34.00 k	1.8
12	42.20 k	1.9
13	52.30 k	2.5
14	64.90 k	3.8
15	80.60 k	5.0
16	100.00 k	5.1
17	124.00 k	5.5
18	249.00 k or larger/open	3.3

(1) E96 Resistor Series, 1% accuracy, temperature coefficient better or equal to ±200 ppm/°C

8.3.4 Smart Enable with Precise Threshold

The voltage applied at the EN pin of the TPS629210E is compared to a fixed threshold rising voltage. This allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The precise enable input allows the use of a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin.

The enable input threshold for a falling edge is lower than the rising edge threshold. The TPS629210E starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

An internal resistor pulls the EN pin to GND and avoids the pin to be floating. This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to a low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

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8.3.5 Power Good (PG)

The TPS629210E has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. V_{IN} must remain present for the PG pin to stay low.

If the power-good output is not used, it is recommended to tie to GND or leave open.

Table 8-3. Power-Good Indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
V_{VIN} > UVLO	HIGH	No	V_O on target	**High Impedance**
			V_O < target	**LOW**
		Yes	x	**LOW**
	LOW	x	x	**LOW**
1.8 V < V_{VIN} < UVLO	x	x	x	**LOW**
V_I < 1.8 V	x	x	x	**Undefined**

8.3.6 Output Discharge Function

The purpose of the discharge function is to make sure there is a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once the TPS629210E has been enabled at least once since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled (EN pin = low), in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V.

8.3.7 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

8.3.8 Current Limit and Short Circuit Protection

The TPS629210E is protected against overload and short circuit events. If the inductor current exceeds the current limit, I_{LIM_HS}, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current limit threshold, I_{LIM_LS}.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given in Equation 1.

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (1)$$

where:

- I_{LIMH} is the static current limit as specified in the electrical characteristics.
- L is the effective inductance at the peak current.
- V_L is the voltage across the inductor (V_{IN} – V_{OUT}).
- t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

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$$I_{peak(typ)} = I_{LIMH} + \frac{VIN - VOUT}{L} \times 50ns \quad (2)$$

The TPS629210E also includes a low-side negative current limit ($I_{LIM:SINK}$) to protect against excessive negative currents that can occur in forced PMW mode under heavy to light load transient conditions. If the negative current in the low-side switch exceeds the $I_{LIM:SINK}$ threshold, the low-side switch is disabled. Both the low-side and high-side switches remain off until an internal timer re-enables the high-side switch based on the selected PWM switching frequency.

CAUTION

It is recommended that the inductor be sized such that the inductor ripple current, ΔI_L (see Equation 9), does not exceed 1.6 A to avoid the potential for continuous operation of the negative current limit with no output load (I_O = 0 A).

8.3.9 Thermal Shutdown

The junction temperature of the device, T_J, is monitored by an internal temperature sensor. If T_J rises and exceeds the thermal shutdown threshold, T_{SD}, the device shuts down. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis, the converter resumes normal operation, beginning with soft start. During a PFM skip pause, the thermal shutdown feature is not active. A shutdown or restart is only triggered during a switching cycle. See Section 8.4.2.

8.4 Device Functional Modes

8.4.1 Forced Pulse Width Modulation (PWM) Operation

The TPS629210E has two operating modes: forced PWM mode discussed in this section and auto PFM/PWM mode as discussed in Section 8.4.2.

With the MODE/S-CONF pin set to forced PWM mode, the device operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of either 1.0 MHz or 2.5 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT}, and the inductance. The on time in forced PWM mode is given by Equation 3.

$$TON = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{sw}} \quad (3)$$

For very small output voltages, an absolute minimum on time of about 40 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high.

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8.4.2 Power Save Mode Operation (Auto PFM/PWM)

When the MODE/S-CONF pin is configured for auto PFM/PWM mode, power save mode is allowed. The device operates in PWM mode as long the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the ripple current of the inductor. Power save mode is entered seamlessly to make sure there is high efficiency in light-load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of power save mode is seamless in both directions.

The TPS629210E adjusts the on time (TON) in power save mode, depending on the input voltage and the output voltage to maintain highest efficiency. The on time in steady-state operation can be estimated as:

With the MODE/S-CONF pin set to 1.0-MHz operation:

$$TON\ (\mu s) = \frac{\mathrm{VOUT}}{VIN} \tag{4}$$

With the MODE/S-CONF pin set to 2.5-MHz operation:

$$TON = 100 \times \frac{VIN}{VIN - VOUT}\,[ns] \tag{5}$$

Using TON, the typical peak inductor current in power save mode is approximated by:

$$ILPSM_{(peak)} = \frac{(VIN - VOUT)}{L} \times TON \tag{6}$$

The output voltage ripple in power save mode is given by Equation 7:

$$\Delta V = \frac{L \times VIN^2}{200 \times C}\left(\frac{1}{VIN - VOUT} + \frac{1}{VOUT}\right) \tag{7}$$

Note

When V_{IN} decreases to typically 15% above V_{OUT}, the device will not enter power save mode regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 AEE (Automatic Efficiency Enhancement)

When the MODE/S-CONF pin is configured for auto PFM/PWM with AEE mode, the TPS629210E provides the highest efficiency over the entire input voltage and output voltage range by automatically adjusting the switching frequency of the converter (see Equation 8). To keep the efficiency high over the entire duty cycle range, the switching frequency is adjusted while maintaining the ripple current amplitudes. This feature compensates for the very small duty cycles of high V_{IN} to low V_{OUT} conversions, which can limit the control range in other topologies.

$$F_{sw}(MHz) = 10 \times V_{OUT} \times \frac{V_{IN} - V_{OUT}}{V_{IN}^{\ 2}} \tag{8}$$

Traditionally, the efficiency of a switched mode converter decreases if V_{OUT} decreases, V_{IN} increases, or both. By decreasing the switching losses at lower V_{OUT} values or higher V_{IN} values, the AEE feature provides an efficiency enhancement across various duty cycles, especially for the lower V_{OUT} values, where fixed frequency converters suffer from a significant efficiency drop. Furthermore, when used with the recommended 2.2-µH

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inductor, the ripple current amplitudes remains low enough to deliver the full output current without reaching current limit across the entire range of input and output voltages (see Figure 8-4).

By using the same TON configuration (see Equation 9) across the entire load range in AEE mode, the inductor ripple current in AEE mode becomes effectively independent of the output voltage and can be approximated by Equation 9:

$$\Delta I_L\ (mA) = TON \times \frac{(VIN - VOUT)}{L} = 0.1 \times \frac{VIN\ (V)}{L\ (\mu H)} \tag{9}$$

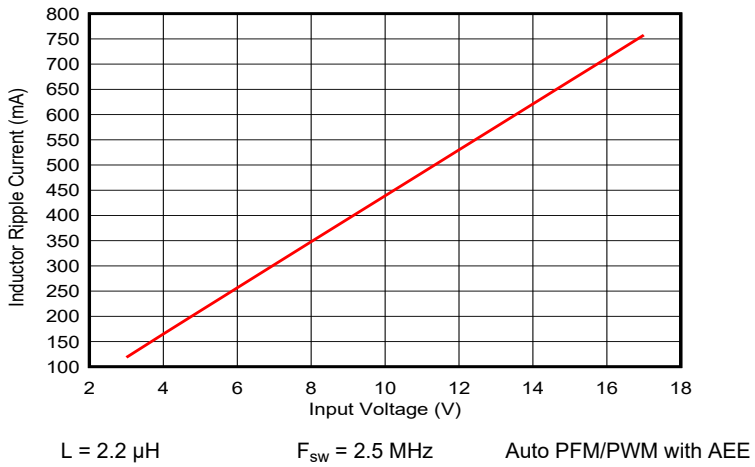

Figure 8-4. Typical Inductor Ripple Current Versus Input Voltage in AEE Mode

The TPS629210E operates in AEE mode as long as the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous mode (DCM), which happens when the output current becomes smaller than half the inductor ripple current.

8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter operated in PWM mode is given in Equation 10.

$$D = \frac{\mathrm{VOUT}}{VIN} \tag{10}$$

The duty cycle increases as the input voltage comes close to the output voltage and the off time of the high-side switch gets smaller. When the minimum off time of typically 80 ns is reached, the TPS629210E scales down its switching frequency while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences. For example, getting the longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$VIN_{(\min)} = VOUT + IOUT\left(R_{DS(on)} + R_L\right) \tag{11}$$

where:

- I_{OUT} is the output current.
- $R_{DS(on)}$ is the on-state resistance of the high-side FET.

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- R_L is the DC resistance of the inductor used.

8.4.5 Starting into a Prebiased Load

The TPS629210E is capable of starting into a prebiased output. The device only starts switching when the internal soft-start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPS629210E does not start switching unless the voltage at the feedback pin drops to the target. Performance is the same for devices configured for VSET operation (internal feedback), however, the switching will be delayed until the soft-start ramp reaches the internal feedback voltage.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS629210E device is a highly efficient, small, and highly-flexible synchronous step-down DC-DC converter that is easy to use. A wide input voltage range of 3 V to 17 V supports a wide variety of inputs like 12-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

9.2 Typical Application

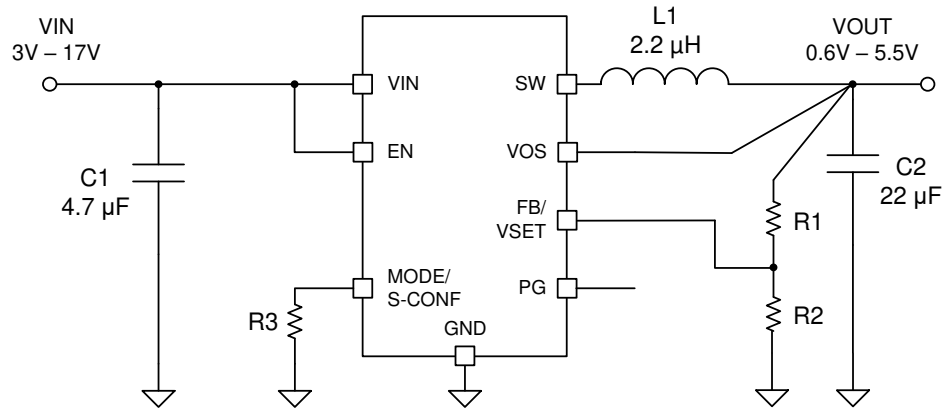

Figure 9-1. Typical Application Setup

Table 9-1. List of Components

Reference	Description	Manufacturer
L1	2.2-µH inductor	XGL3530-222; Coilcraft
C1	4.7 µF, 25 V, Ceramic, 1206	C3216X7R1E475K160AC, TDK
C2	22 µF, 6.3 V, Ceramic, 0805	GCM21BD70J226ME36L, MuRata
R1	Depending on V_{OUT}; see Section 9.2.2.2.	Standard 1% metal film
R2	Depending on V_{OUT}; see Section 9.2.2.2.	Standard 1% metal film
R3	Depending on device setting, see Section 8.3.1.	Standard 1% metal film

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9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS629210E device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Programming the Output Voltage

The output voltage of the TPS629210E is adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Table 9-2. It is recommended to choose resistor values that allow a current of at least 2 µA, meaning the value of R2 should not exceed 300 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R1 = R2 \times \left(\frac{VOUT}{VFB} - 1 \right) \tag{12}$$

where

- VFB is 0.6 V.

Table 9-2. Setting the Output Voltage

Nominal Output Voltage	R1	R2	Exact Output Voltage
0.8 V	51 kΩ	150 kΩ	0.804 V
1.2 V	130 kΩ	130 kΩ	1.200 V
1.5 V	150 kΩ	100 kΩ	1.500 V
1.8 V	475 kΩ	237 kΩ	1.803 V
2.5 V	523 kΩ	165 kΩ	2.502 V
3.3 V	619 kΩ	137 kΩ	3.311 V
5 V	619 kΩ	84.5 kΩ	4.995 V

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device. The TPS629210E is optimized to work within a range of external components.

9.2.2.3.1 Output Filter and Loop Stability

The TPS629210E is internally compensated to be stable with a range of LC filter combinations. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter using Equation 13.

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$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (13)$$

Table 9-3 can be used to simplify the output filter component selection. The values in Table 9-3 are nominal values, and the effective capacitance was considered to be +20% and –50%. Different values can work, but care has to be taken on the loop stability which is affected. More information on the sizing of the LC filter of a DCS-Control regulator can be found in the *Optimizing the TPS62130/40/50/60 Output Filter Application Note*.

Table 9-3. Recommended LC Output Filter Combinations

	4.7 µF	10 µF	22 µF	47 µF	100 µF	200 µF
1 µH (3) (4)			√	√	√	√ (2)
1.5 µH		√	√	√	√ (2)	
2.2 µH		√	√(1)	√	√ (2)	
3.3 µH	√	√	√	√		
4.7 µH	√	√	√	√(2)		

(1) This LC combination is the standard value and recommended for most applications.
(2) Output capacitance needs to have an ESR of ≥ 10 mΩ for stable operation. See Section 9.3.1.
(3) Not recommended for 1-MHz operation
(4) At full load, I_{Lpeak} can exceed I_{LIM_HS} at higher input or output voltages.

Although the TPS629210E is stable without the pole and zero being in a particular location, an external feedforward capacitor can also be added to adjust their location based on the specific needs of the application. This can provide better performance in power save mode, improved transient response, or both.

A more detailed discussion on the optimization for stability versus transient response can be found in the *Optimizing Transient Response of Internally Compensated DC-DC Converters Application Note* and *Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family Application Note*.

9.2.2.3.2 Inductor Selection

The TPS629210E is designed for a nominal 2.2-µH inductor. Larger values can be used to achieve a lower inductor current ripple but they can have a negative impact on efficiency and transient response. Smaller values than 2.2 µH cause larger inductor current ripple, which cause larger negative inductor currents in forced PWM mode and higher peak currents at full load. Therefore, they are not recommended at larger voltages across the inductor as it is the case for high input voltages and low output voltages. With low output current in forced PWM mode, this causes a larger negative inductor current peak that can exceed the negative current limit. At low or no output current and small inductor values, the output voltage can therefore not be regulated any more. More detailed information on further LC combinations can be found in the *Optimizing the TPS62130/40/50/60 Output Filter Application Note*.

The inductor selection is affected by several effects like the following:

- Inductor ripple current
- Output ripple voltage
- PWM-to-PFM transition point
- Efficiency

In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 14 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \quad (14)$$

$$\Delta I_{L(\max)} = \frac{VIN_{(\max)}}{L_{(\min)}} \times 100ns \quad (15)$$

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where:

- I_L(max) is the maximum inductor current.
- ΔI_L is the peak-to-peak inductor ripple current.
- L(min) is the minimum effective inductor value.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS629210E and are recommended for use:

Table 9-4. List of Inductors

Type	Inductance [µH]	DCR [mΩ]	Current [A](1)	Dimensions [L×W×H] mm	Manufacturer
DFE201210U-1R5M(2)	1.5 µH, ±20%	115	2.5	2.0 × 1.2 × 1.0	muRata
DFE252012PD-2R2M	2.2 µH, ±20%	84	2.8	2.5 × 2.0 × 1.2	muRata
XGL3530-222ME	2.2 µH, ±20%	20	4.0	3.5 × 3.2 × 3	Coilcraft
XGL4020-222ME	2.2 µH, ±20%	19.5	6.2	4 × 4 × 2.1	Coilcraft
XGL3530-332ME	3.3 µH, ±20%	33	3.3	3.5 × 3.2 × 3	Coilcraft
XGL4020-472ME	4.7 µH, ±20%	43	4.1	4 × 4 × 2.1	Coilcraft

(1) I_{SAT} at 30% drop
(2) For smaller size solutions that do not require maximum efficiency at the full output current

The inductor value also determines the load current at which power save mode is entered:

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \quad (16)$$

9.2.2.3.3 Capacitor Selection

9.2.2.3.3.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS629210E allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see *Optimizing the TPS62130/40/50/60 Output Filter Application Note* for more information).

In power save mode, the output voltage ripple depends on the following:

- Output capacitance
- ESR
- ESL
- Peak inductor current

Using ceramic capacitors provides small ESR, ESL, and low ripple.

The output capacitor needs to be as close as possible to the device, and it is recommended to have the VOS signal and feedback resistors (if used) should be connected to the positive terminal of the output capacitor.

For large output voltages, the DC bias effect of ceramic capacitors is large and the effective capacitance has to be observed.

9.2.2.3.3.2 Input Capacitor

For most applications, 4.7-µF nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.

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Table 9-5. List of Capacitors

Type	Nominal Capacitance [µF]	Voltage Rating [V]	Size	Manufacturer
C3216X7R1E475K160AC	4.7	25	1206(1)	TDK
C3216X7R1E106K160AC	10	25	1206(1)	TDK

(1) Smaller (0805 or 0603) options may be used and are available from various manufacturers.

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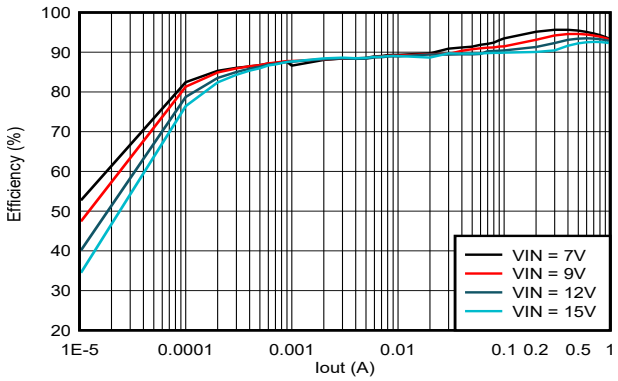
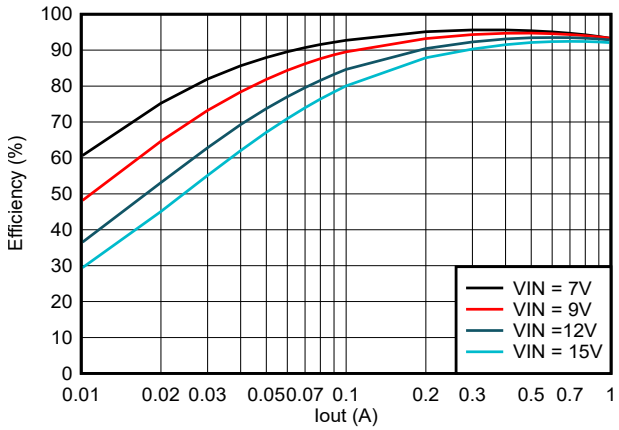
9.2.3 Application Curves



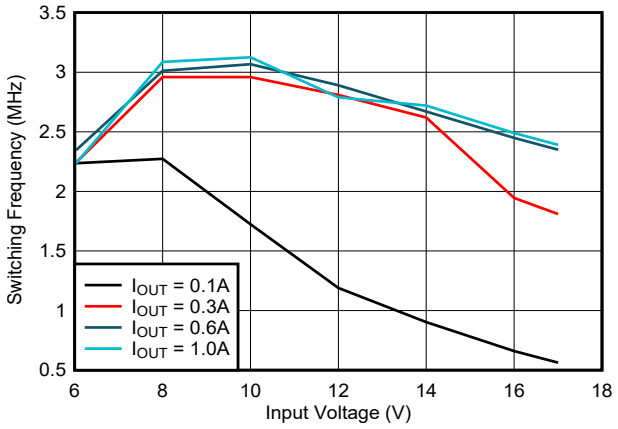
V_{OUT} = 5.0 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-2. Efficiency vs Output Current



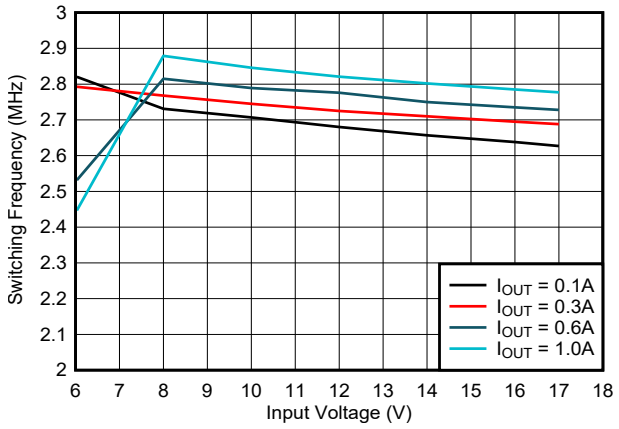
V_{OUT} = 5.0 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-3. Efficiency vs Output Current



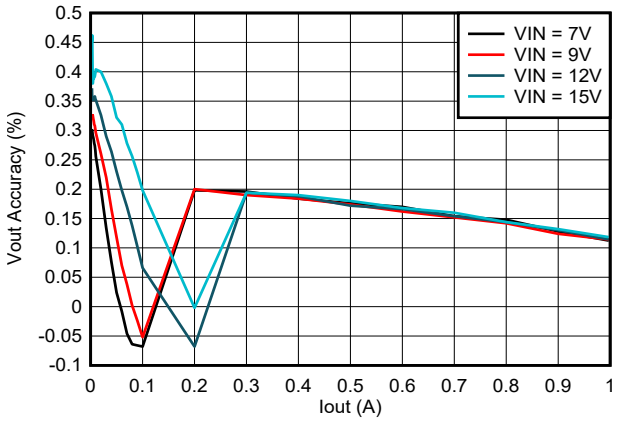
V_{OUT} = 5.0 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-4. Switching Frequency vs Input Voltage



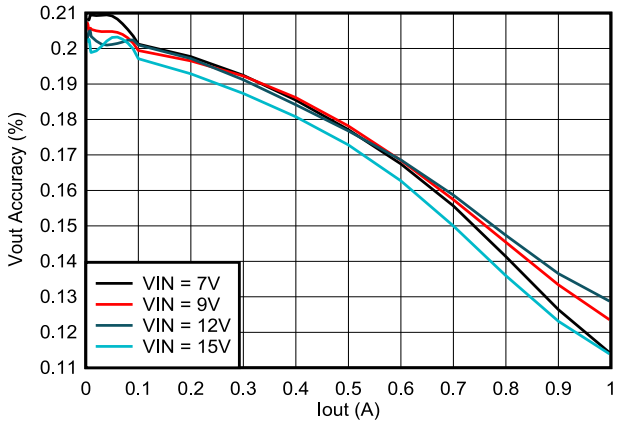
V_{OUT} = 5.0 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-5. Switching Frequency vs Input Voltage



V_{OUT} = 5.0 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-6. Output Voltage vs Output Current



V_{OUT} = 5.0 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-7. Output Voltage vs Output Current

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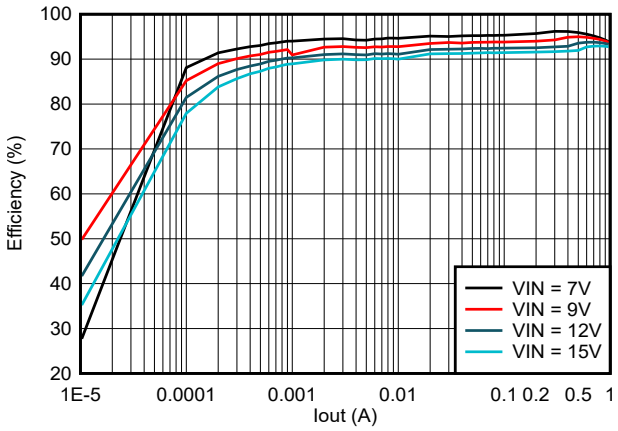
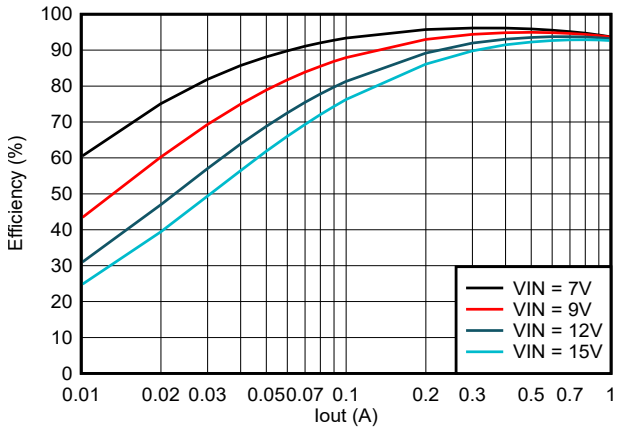
9.2.3 Application Curves (continued)



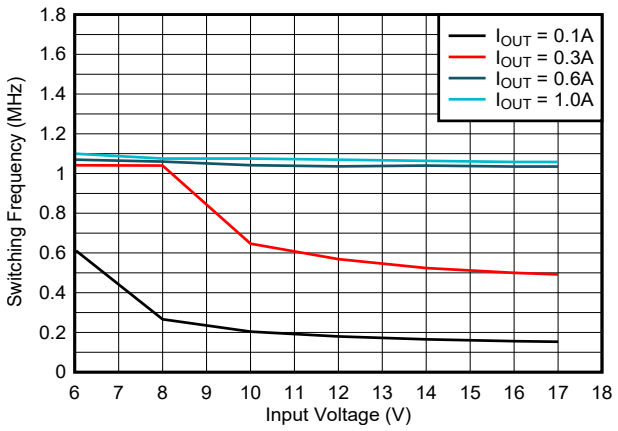
V_{OUT} = 5.0 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-8. Efficiency vs Output Current



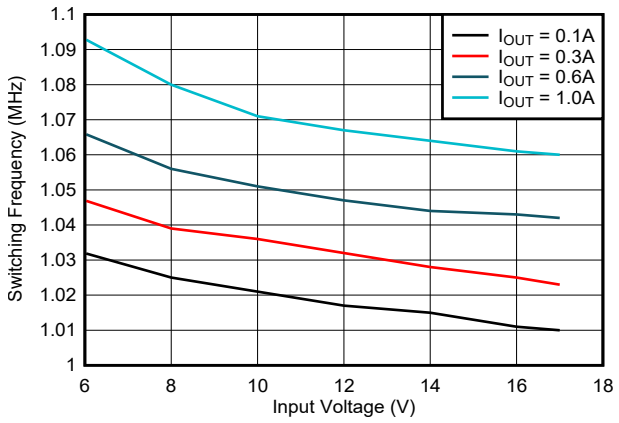
V_{OUT} = 5.0 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-9. Efficiency vs Output Current



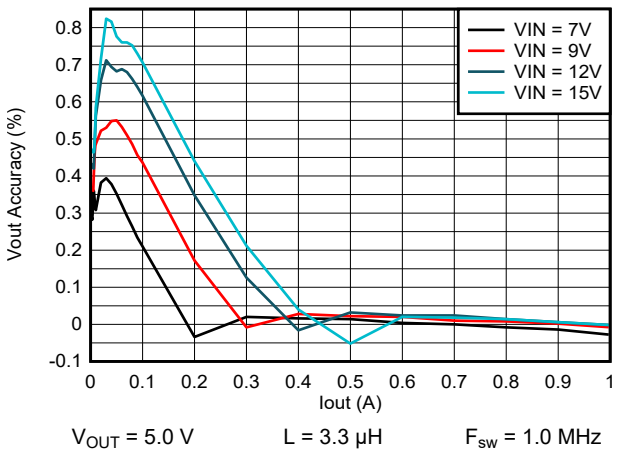
V_{OUT} = 5.0 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-10. Switching Frequency vs Input Voltage



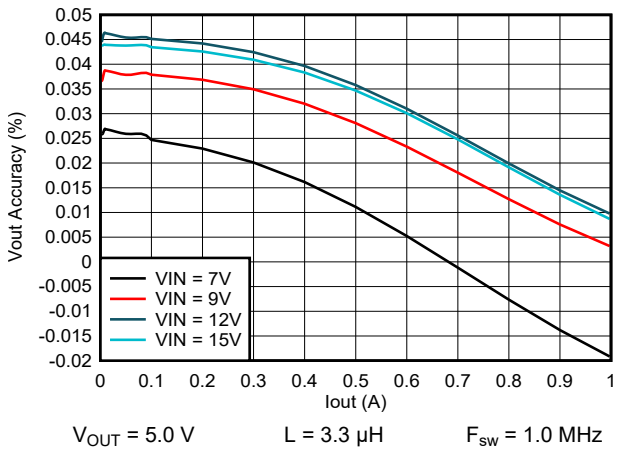
V_{OUT} = 5.0 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-11. Switching Frequency vs Input Voltage



V_{OUT} = 5.0 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-12. Output Voltage vs Output Current



V_{OUT} = 5.0 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-13. Output Voltage vs Output Current

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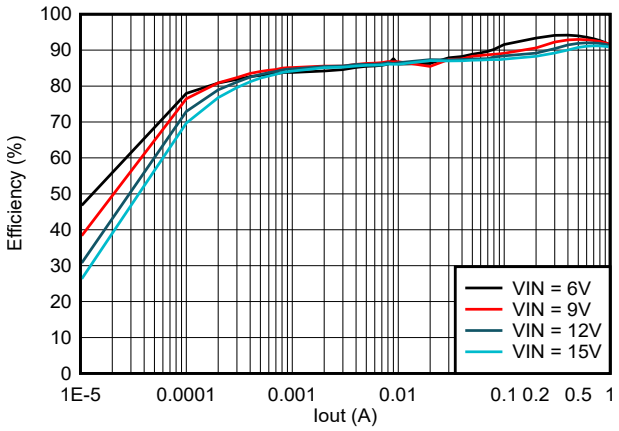
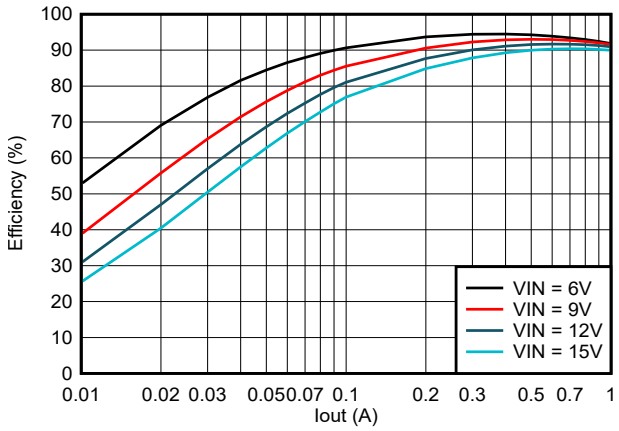
9.2.3 Application Curves (continued)



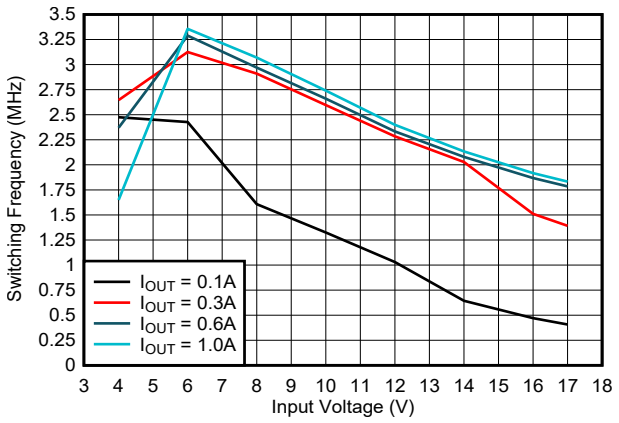
V_{OUT} = 3.3 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-14. Efficiency vs Output Current



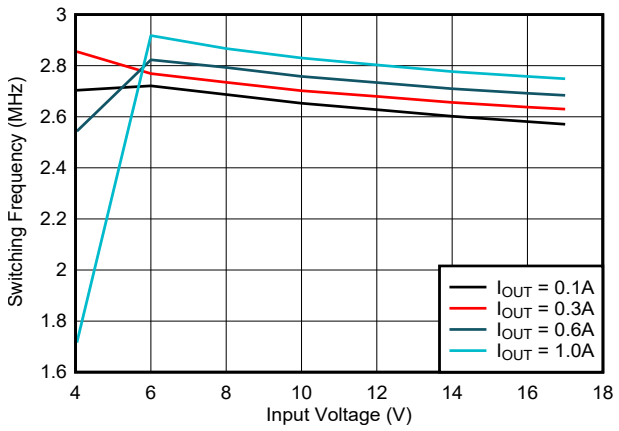
V_{OUT} = 3.3 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-15. Efficiency vs Output Current



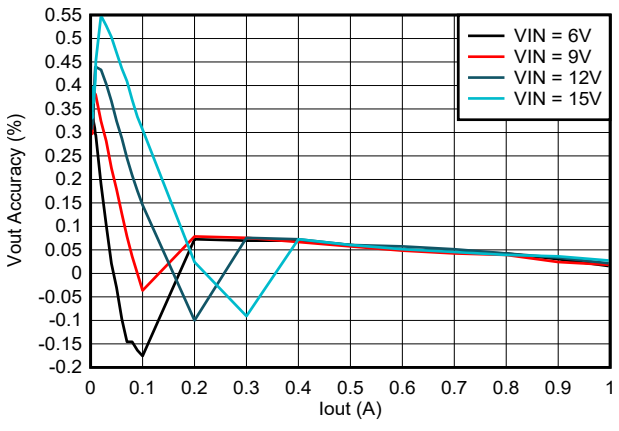
V_{OUT} = 3.3 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-16. Switching Frequency vs Input Voltage



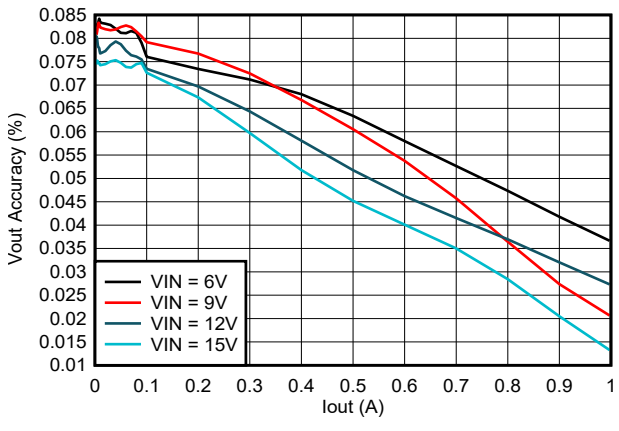
V_{OUT} = 3.3 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-17. Switching Frequency vs Input Voltage



V_{OUT} = 3.3 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-18. Output Voltage vs Output Current



V_{OUT} = 3.3 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-19. Output Voltage vs Output Current

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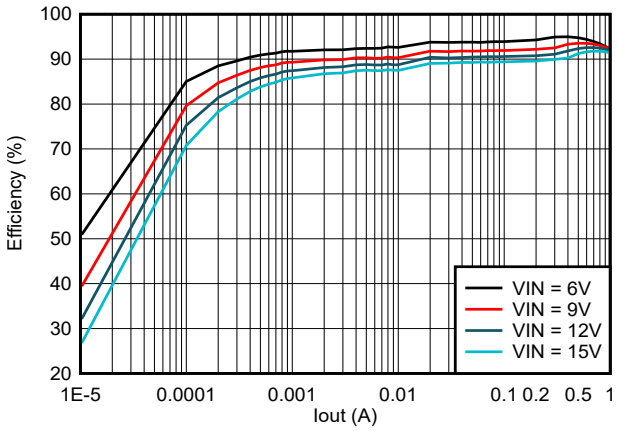
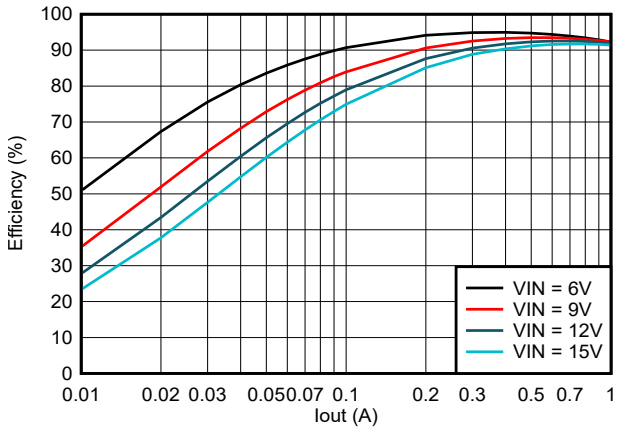
9.2.3 Application Curves (continued)



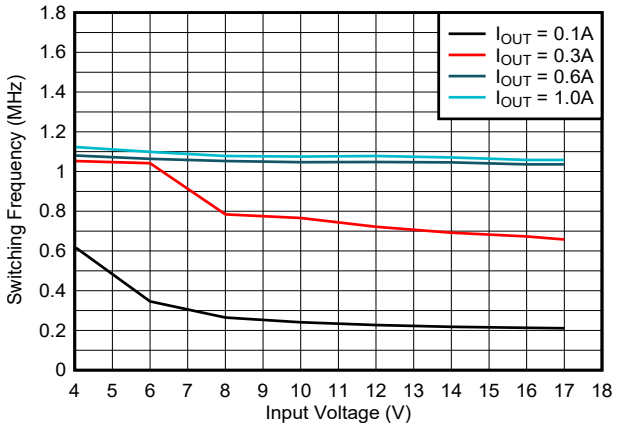
V_{OUT} = 3.3 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-20. Efficiency vs Output Current



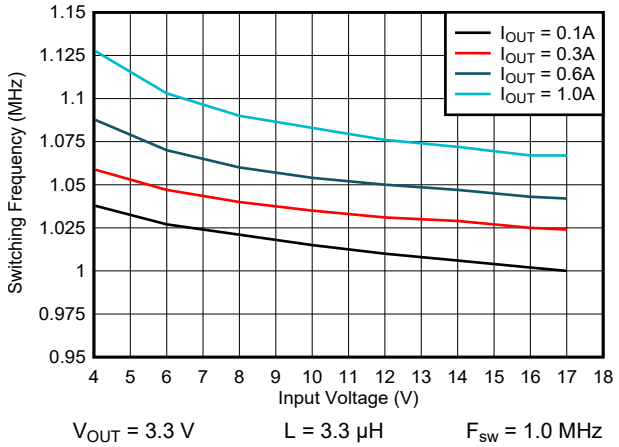
V_{OUT} = 3.3 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-21. Efficiency vs Output Current



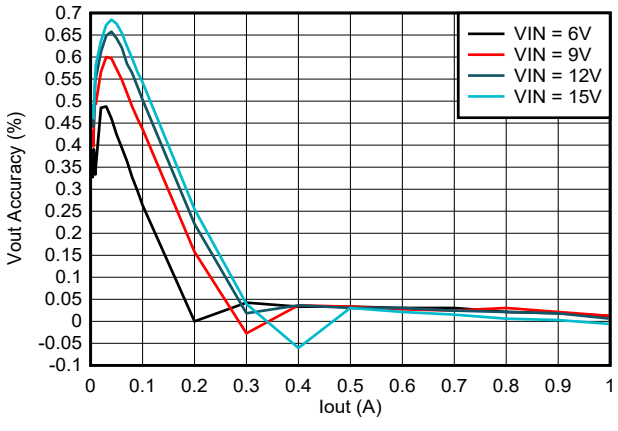
V_{OUT} = 3.3 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-22. Switching Frequency vs Input Voltage



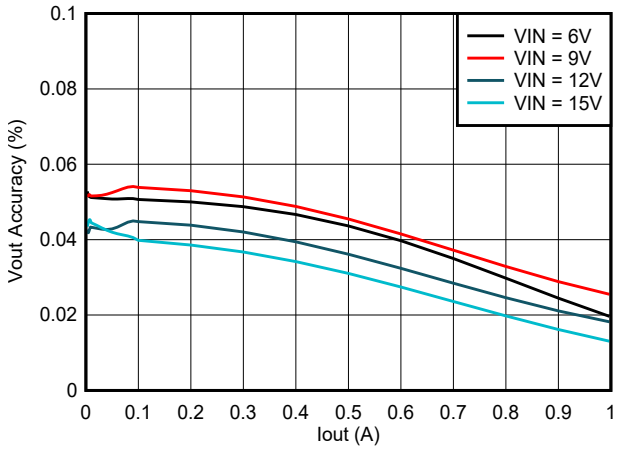
V_{OUT} = 3.3 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-23. Switching Frequency vs Input Voltage



V_{OUT} = 3.3 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-24. Output Voltage vs Output Current



V_{OUT} = 3.3 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-25. Output Voltage vs Output Current

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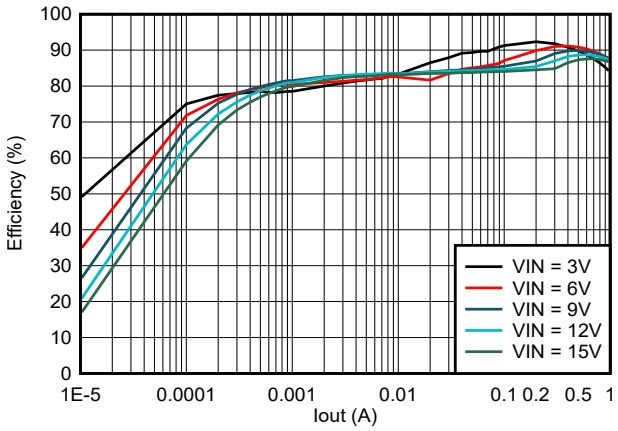
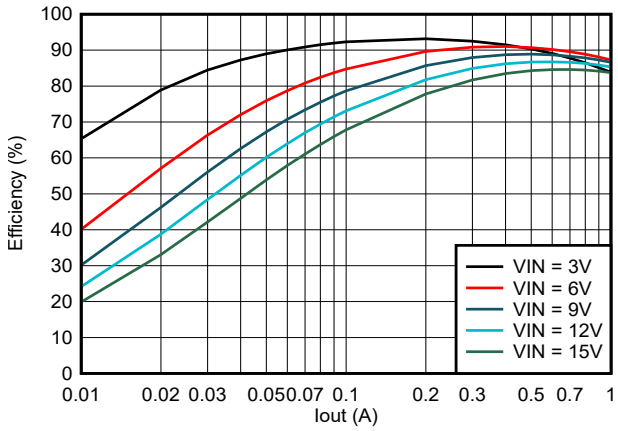
9.2.3 Application Curves (continued)



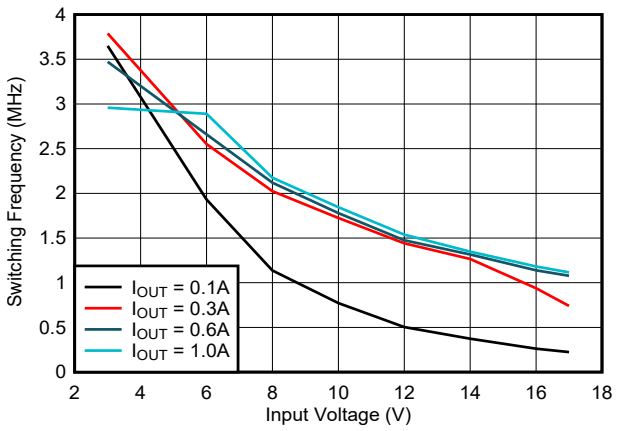
V_{OUT} = 1.8 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-26. Efficiency vs Output Current



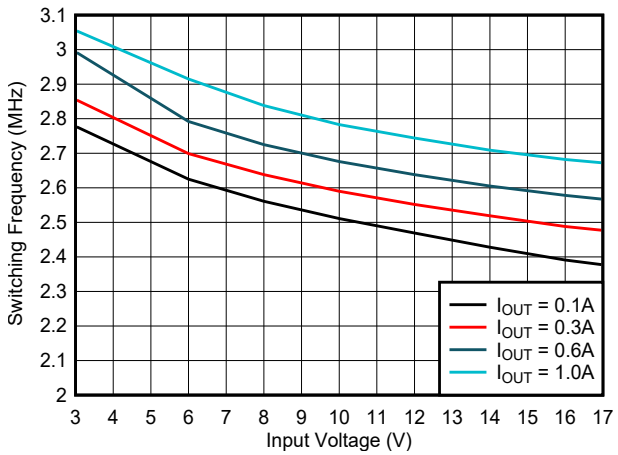
V_{OUT} = 1.8 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-27. Efficiency vs Output Current



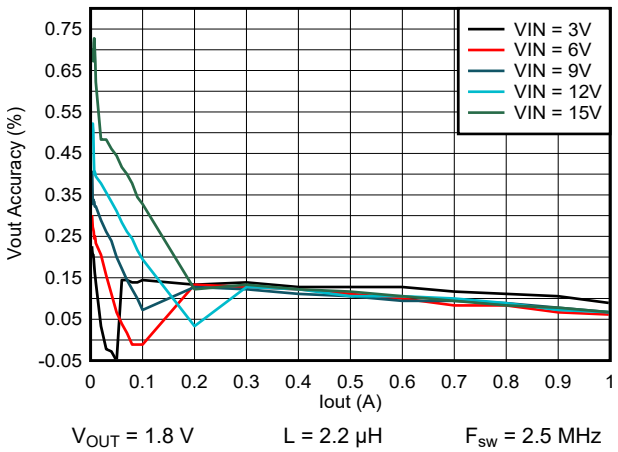
V_{OUT} = 1.8 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-28. Switching Frequency vs Input Voltage



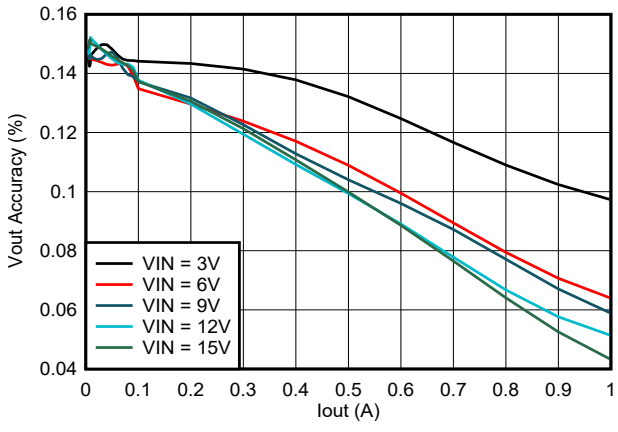
V_{OUT} = 1.8 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-29. Switching Frequency vs Input Voltage



V_{OUT} = 1.8 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-30. Output Voltage vs Output Current



V_{OUT} = 1.8 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-31. Output Voltage vs Output Current

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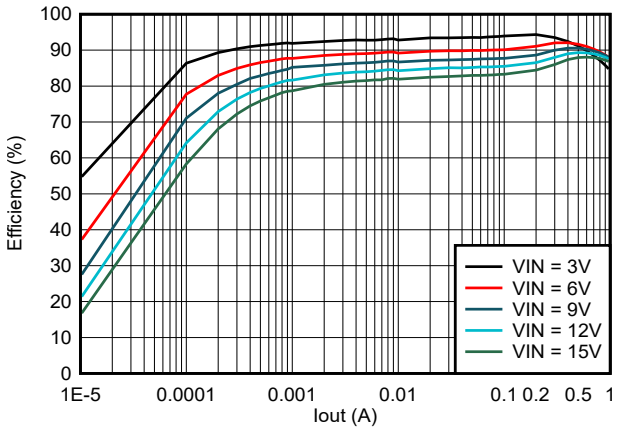
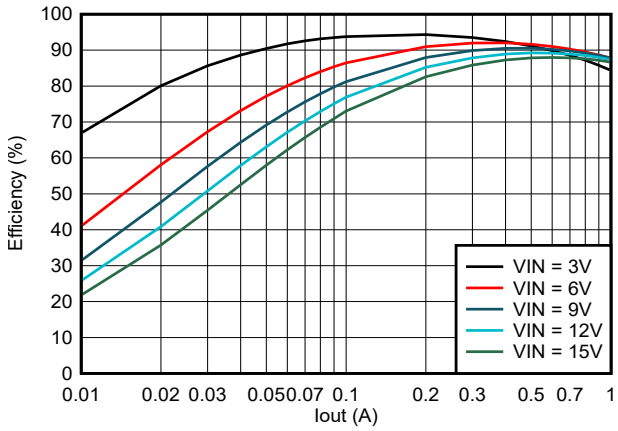
9.2.3 Application Curves (continued)



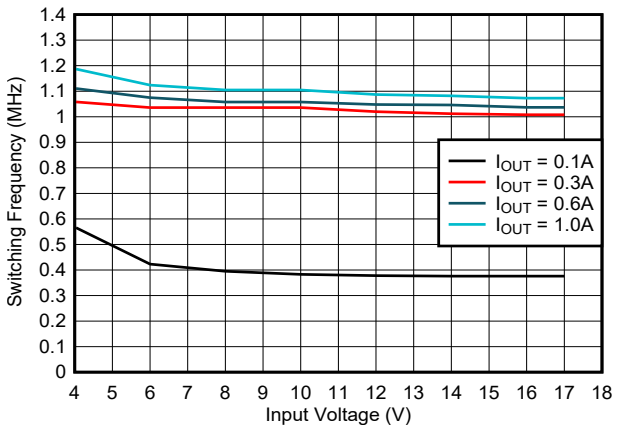
V_{OUT} = 1.8 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-32. Efficiency vs Output Current



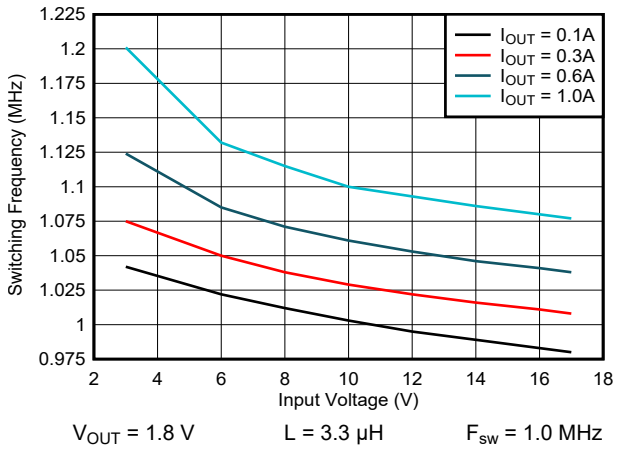
V_{OUT} = 1.8 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-33. Efficiency vs Output Current



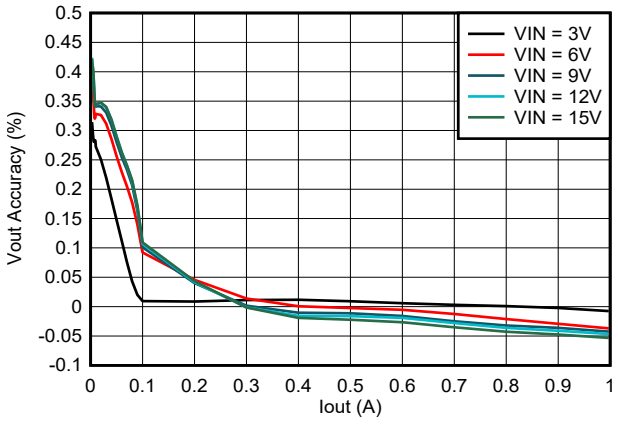
V_{OUT} = 1.8 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-34. Switching Frequency vs Input Voltage



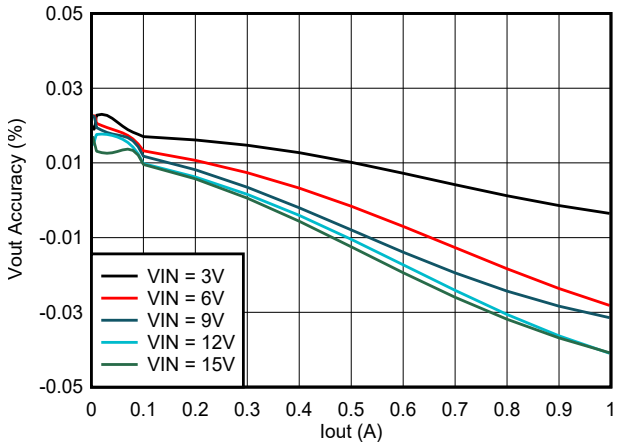
V_{OUT} = 1.8 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-35. Switching Frequency vs Input Voltage



V_{OUT} = 1.8 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-36. Output Voltage vs Output Current



V_{OUT} = 1.8 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-37. Output Voltage vs Output Current

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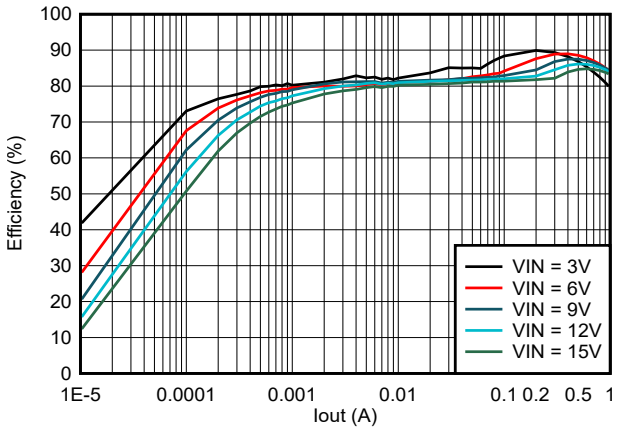
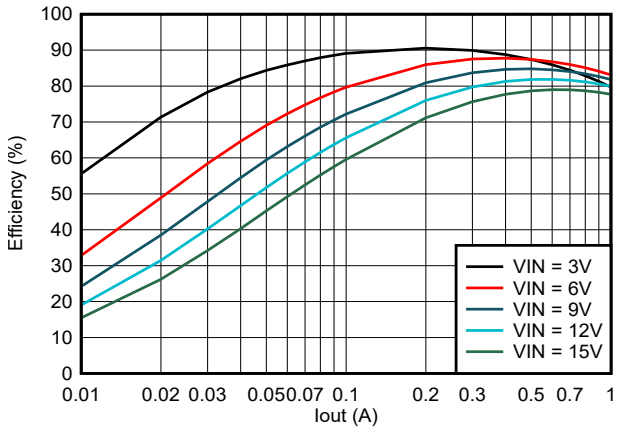
9.2.3 Application Curves (continued)



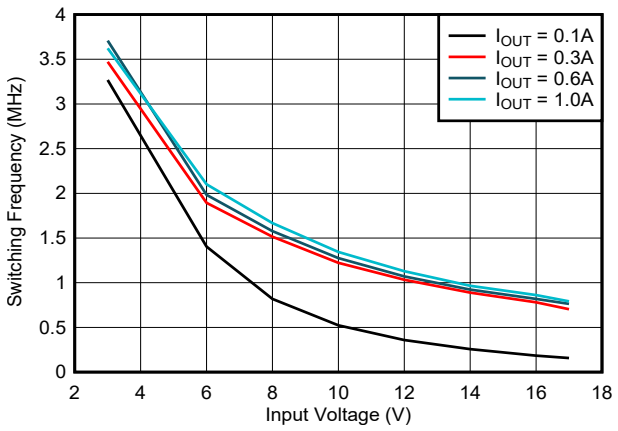
V_{OUT} = 1.2 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-38. Efficiency vs Output Current



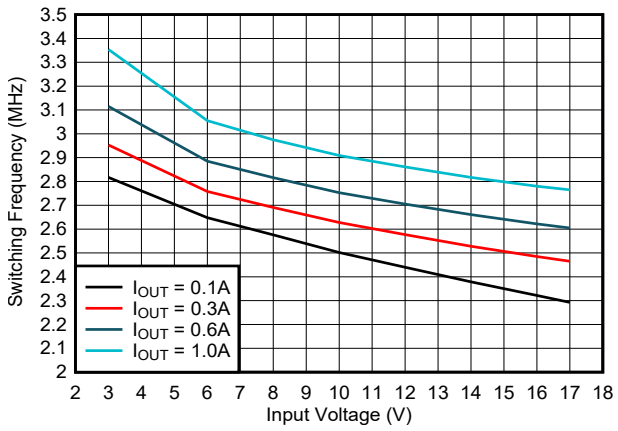
V_{OUT} = 1.2 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-39. Efficiency vs Output Current



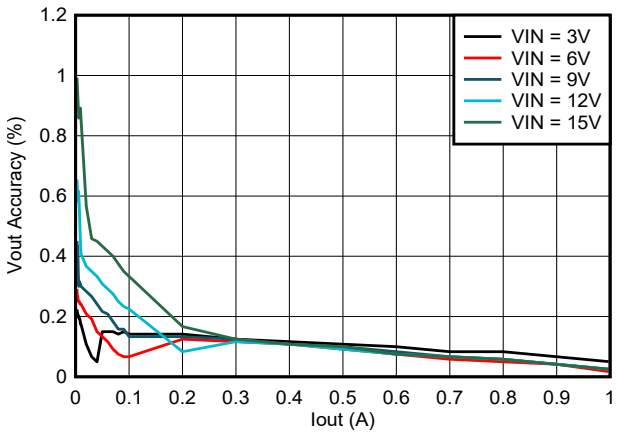
V_{OUT} = 1.2 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-40. Switching Frequency vs Input Voltage



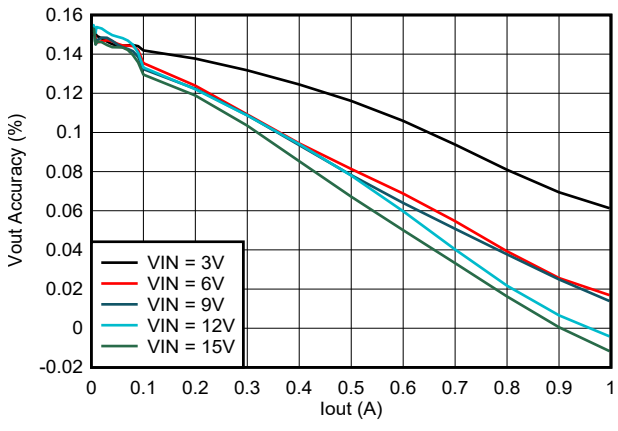
V_{OUT} = 1.2 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-41. Switching Frequency vs Input Voltage



V_{OUT} = 1.2 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-42. Output Voltage vs Output Current



V_{OUT} = 1.2 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-43. Output Voltage vs Output Current

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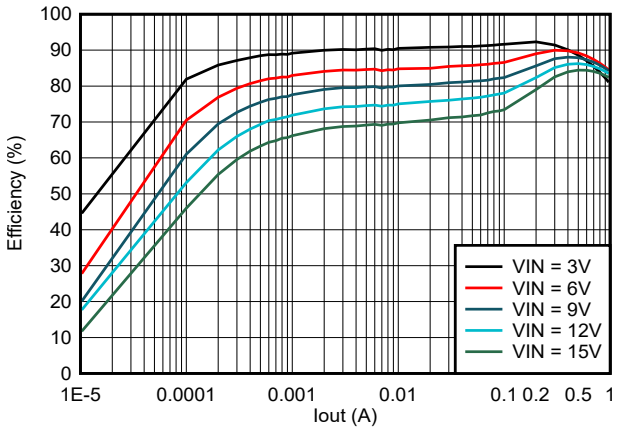
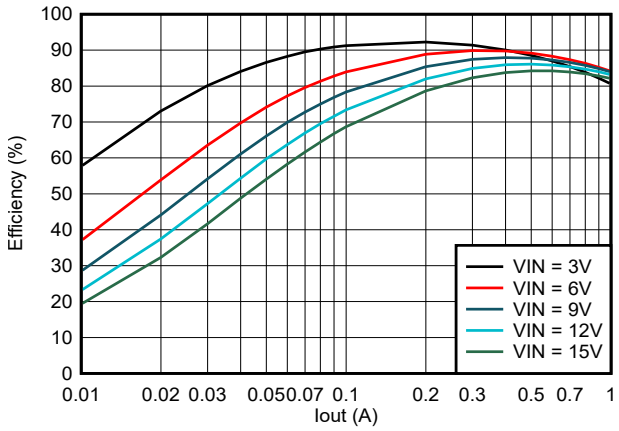
9.2.3 Application Curves (continued)



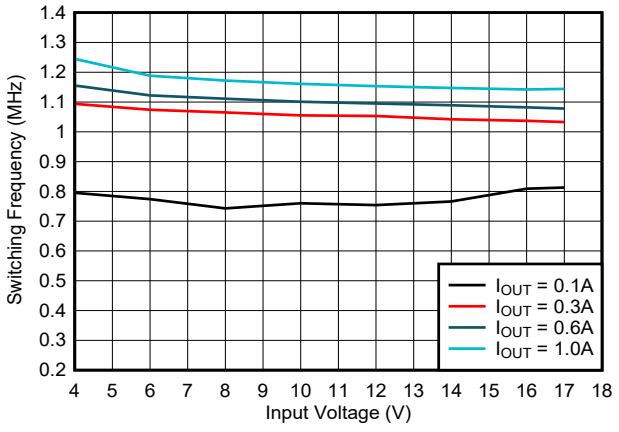
V_{OUT} = 1.2 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-44. Efficiency vs Output Current



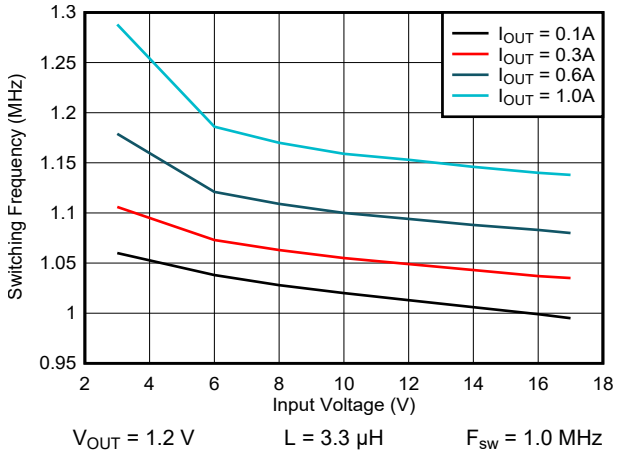
V_{OUT} = 1.2 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-45. Efficiency vs Output Current



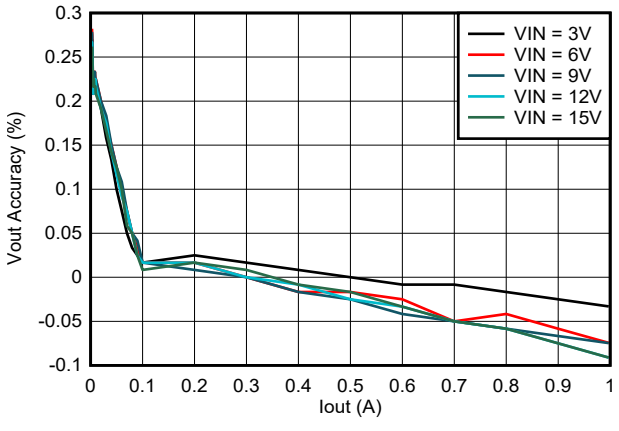
V_{OUT} = 1.2 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-46. Switching Frequency vs Input Voltage



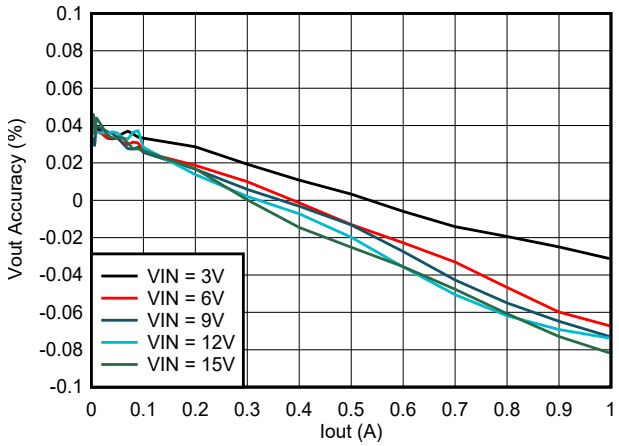
V_{OUT} = 1.2 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-47. Switching Frequency vs Input Voltage



V_{OUT} = 1.2 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-48. Output Voltage vs Output Current



V_{OUT} = 1.2 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-49. Output Voltage vs Output Current

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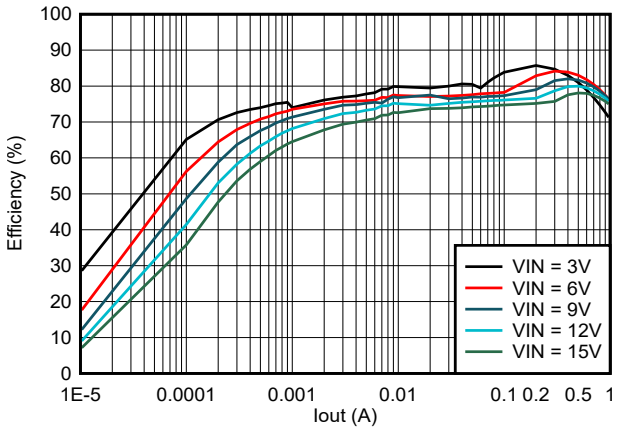
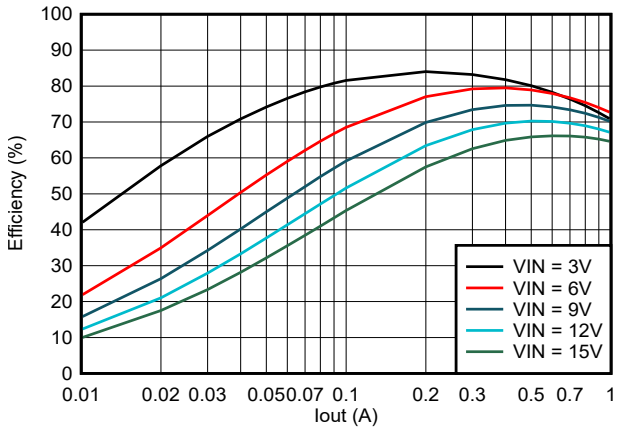
9.2.3 Application Curves (continued)



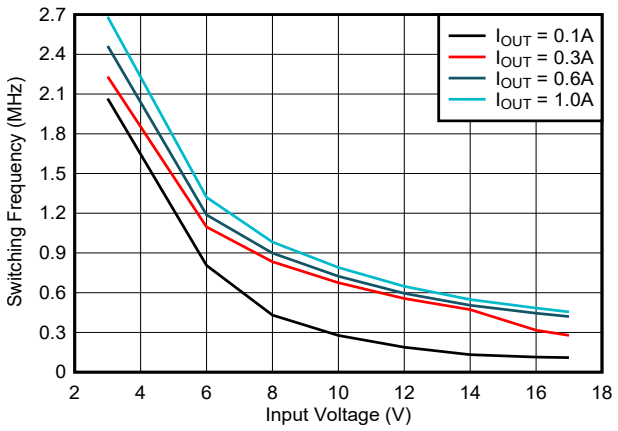
V_{OUT} = 0.6 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-50. Efficiency vs Output Current



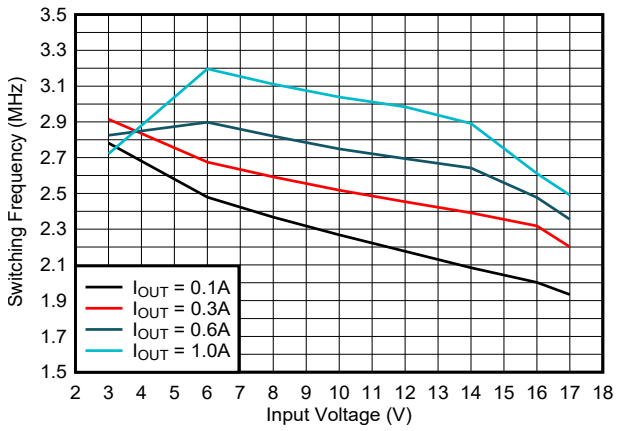
V_{OUT} = 0.6 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-51. Efficiency vs Output Current



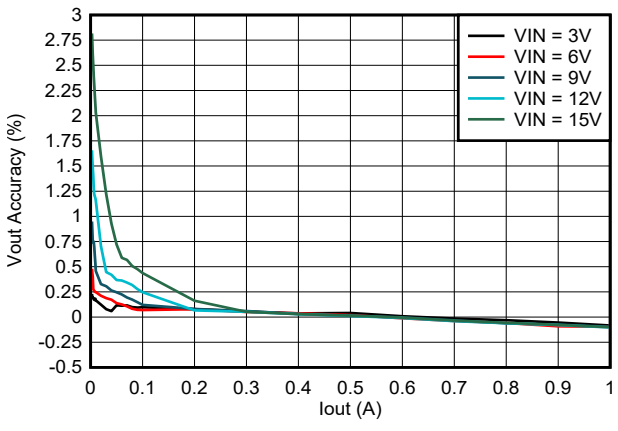
V_{OUT} = 0.6 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-52. Switching Frequency vs Input Voltage



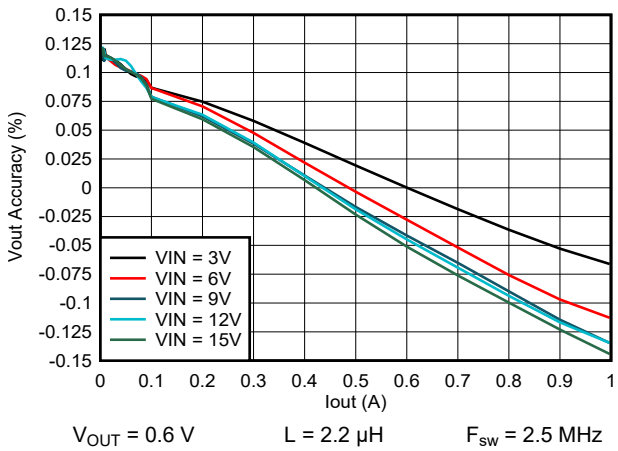
V_{OUT} = 0.6 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-53. Switching Frequency vs Input Voltage



V_{OUT} = 0.6 V L = 2.2 µH F_{sw} = 2.5 MHz Auto PFM/PWM

Figure 9-54. Output Voltage vs Output Current



V_{OUT} = 0.6 V L = 2.2 µH F_{sw} = 2.5 MHz Forced PWM

Figure 9-55. Output Voltage vs Output Current

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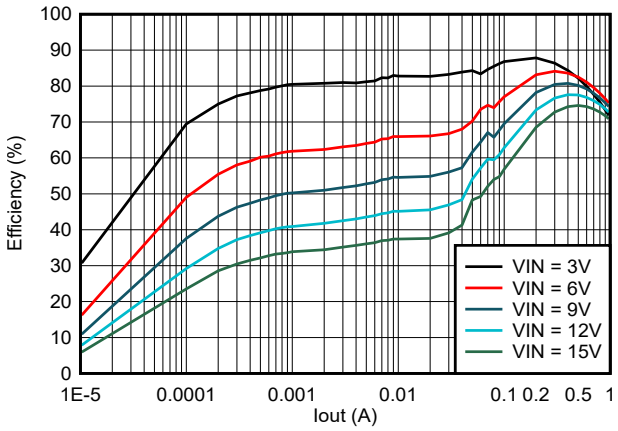
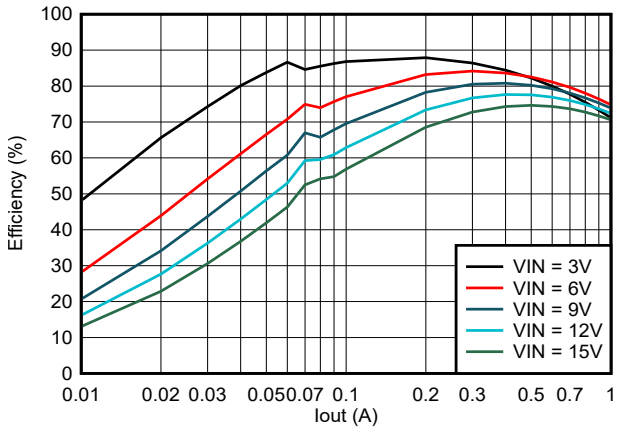
9.2.3 Application Curves (continued)



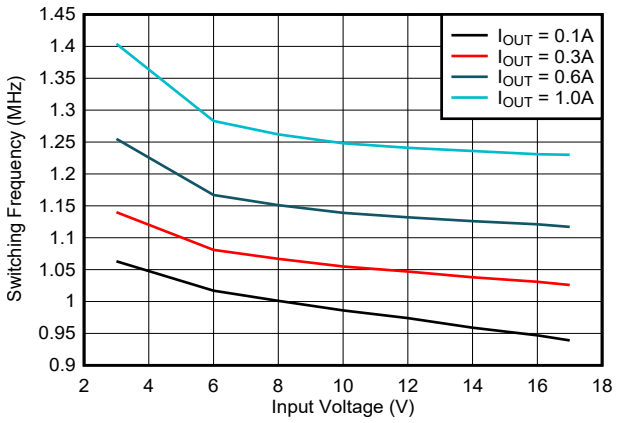
V_{OUT} = 0.6 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-56. Efficiency vs Output Current



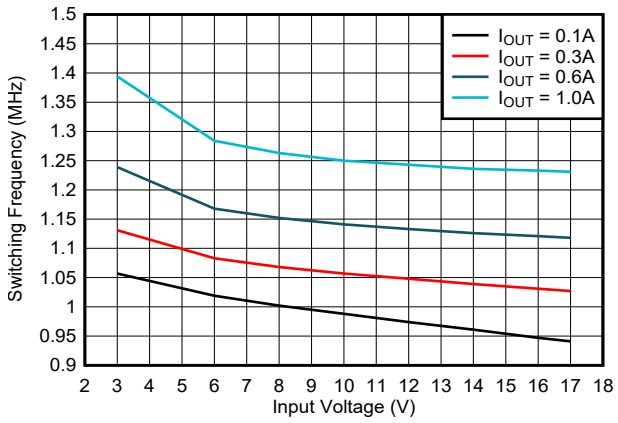
V_{OUT} = 0.6 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-57. Efficiency vs Output Current



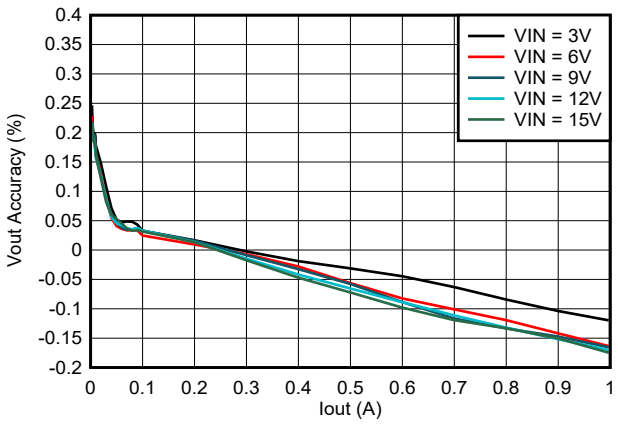
V_{OUT} = 0.6 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-58. Switching Frequency vs Input Voltage



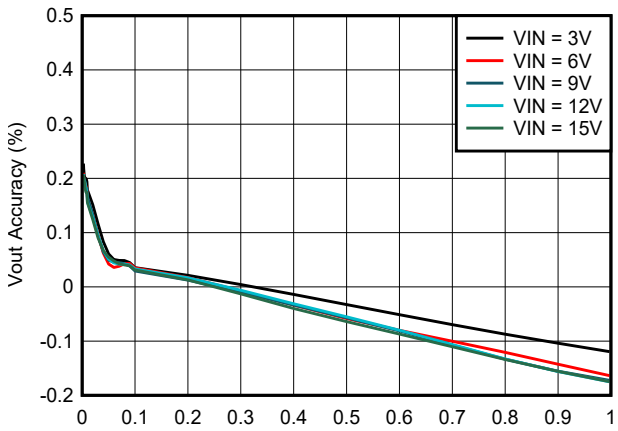
V_{OUT} = 0.6 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-59. Switching Frequency vs Input Voltage



V_{OUT} = 0.6 V L = 3.3 µH F_{sw} = 1.0 MHz Auto PFM/PWM

Figure 9-60. Output Voltage vs Output Current



V_{OUT} = 0.6 V L = 3.3 µH F_{sw} = 1.0 MHz Forced PWM

Figure 9-61. Output Voltage vs Output Current

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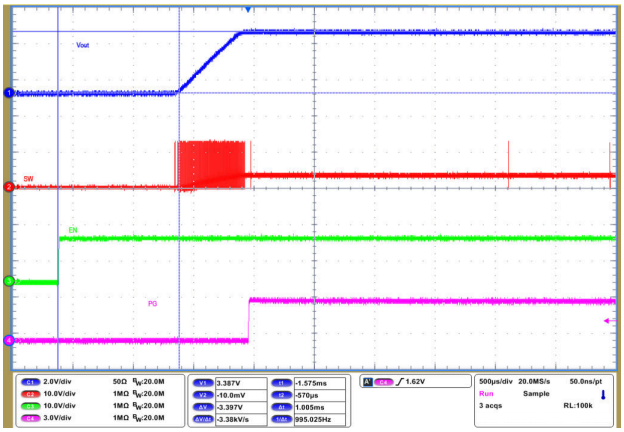
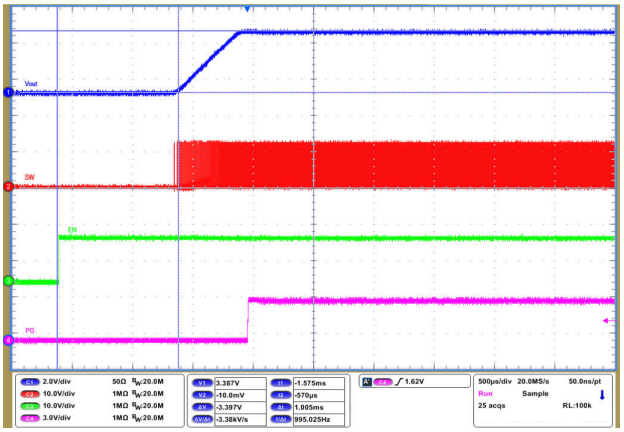
9.2.3 Application Curves (continued)



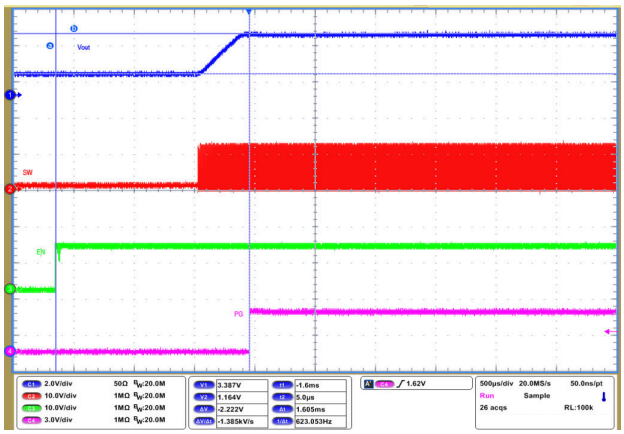
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0 A | Auto PFM/PWM

Figure 9-62. Start-Up Timing



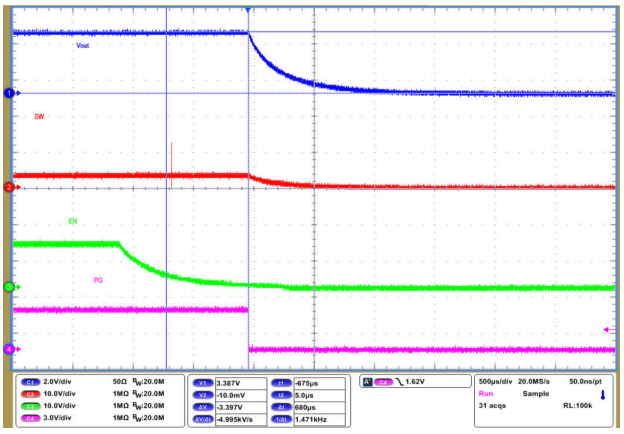
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Forced PWM

Figure 9-63. Start-Up Timing



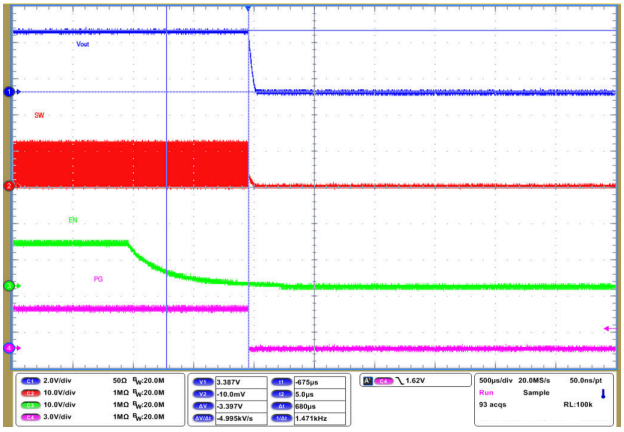
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0 A | Forced PWM

Figure 9-64. Start-Up into Prebiased Output



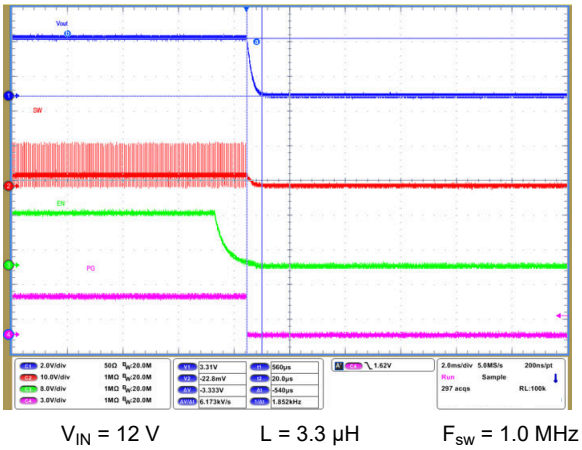
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0 A | Auto PFM/PWM

Figure 9-65. Shutdown Timing with Output Discharge Enabled



V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Forced PWM

Figure 9-66. Shutdown Timing with Output Discharge Disabled



V_{IN} = 12 V | L = 3.3 µH | F_{sw} = 1.0 MHz
V_{OUT} = 3.3 V | I_O = 10 mA | Auto PFM/PWM

Figure 9-67. Shutdown Timing with Output Discharge Enabled

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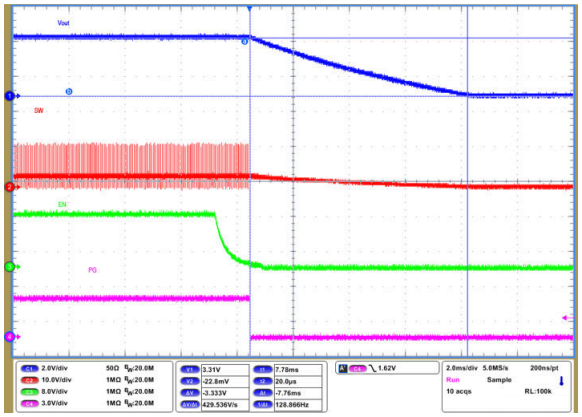
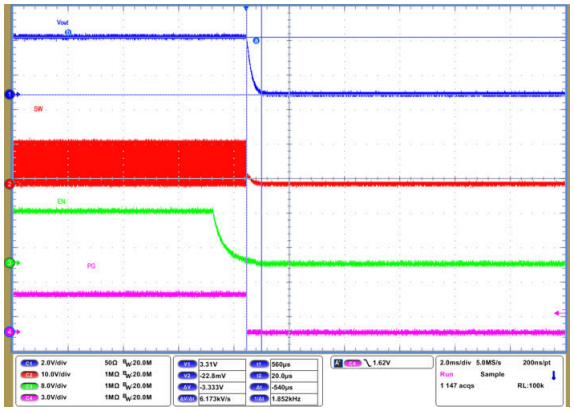
9.2.3 Application Curves (continued)



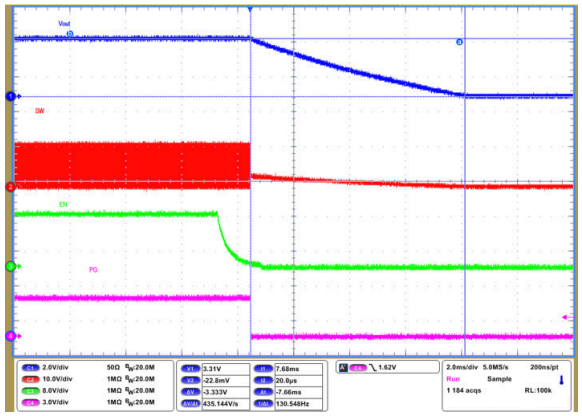
V_{IN} = 12 V | L = 3.3 µH | F_{sw} = 1.0 MHz
V_{OUT} = 3.3 V | I_O = 10 mA | Auto PFM/PWM

Figure 9-68. Shutdown Timing with Output Discharge Disabled



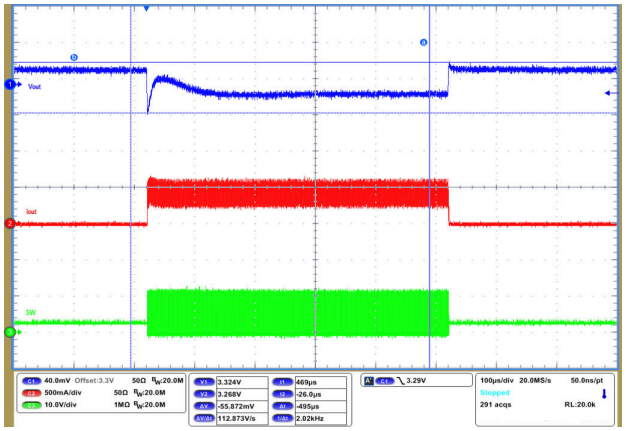
V_{IN} = 12 V | L = 3.3 µH | F_{sw} = 1.0 MHz
V_{OUT} = 3.3 V | I_O = 10 mA | Forced PWM

Figure 9-69. Shutdown Timing with Output Discharge Enabled



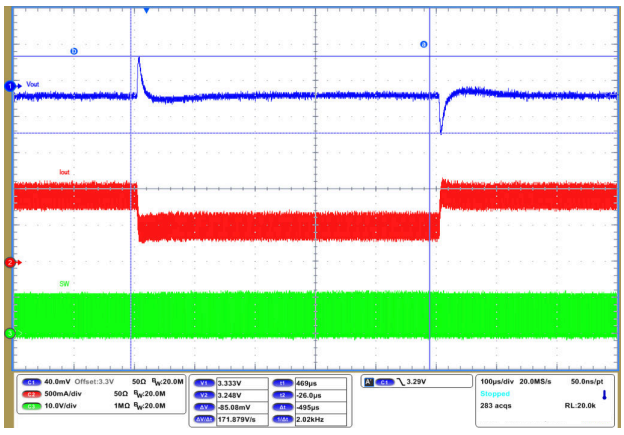
V_{IN} = 12 V | L = 3.3 µH | F_{sw} = 1.0 MHz
V_{OUT} = 3.3 V | I_O = 10 mA | Forced PWM

Figure 9-70. Shutdown Timing with Output Discharge Disabled



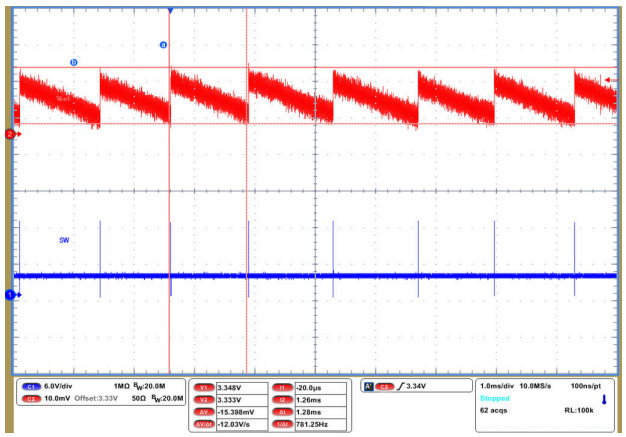
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0 A to 0.5 A | Auto PFM/PWM

Figure 9-71. Load Transient Response



V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0.5 A to 1 A | Auto PFM/PWM

Figure 9-72. Load Transient Response



V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0 A | Auto PFM/PWM

Figure 9-73. Output Voltage Ripple

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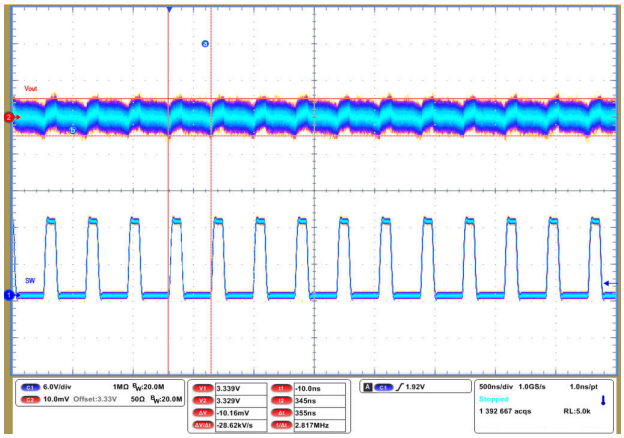
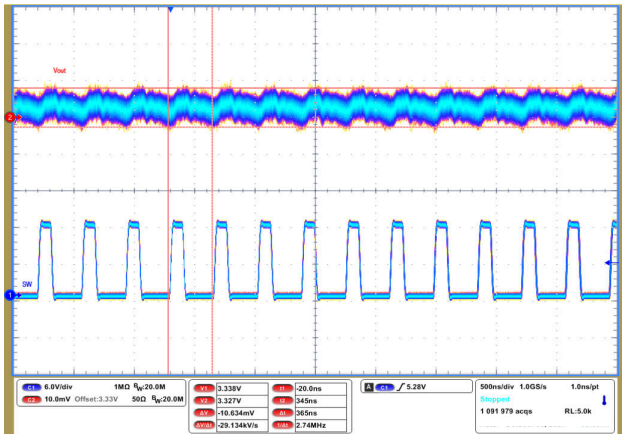
9.2.3 Application Curves (continued)



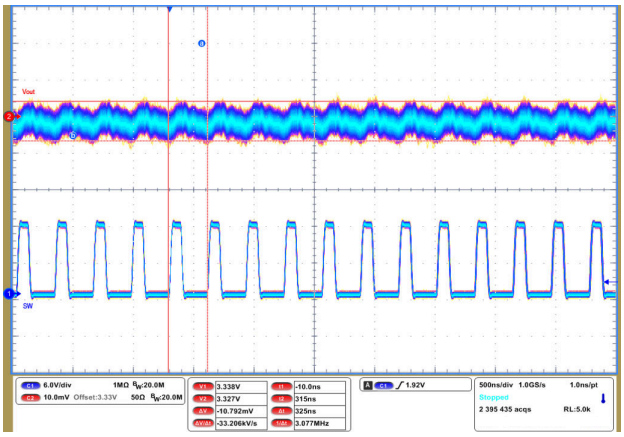
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 0 A | Forced PWM

Figure 9-74. Output Voltage Ripple



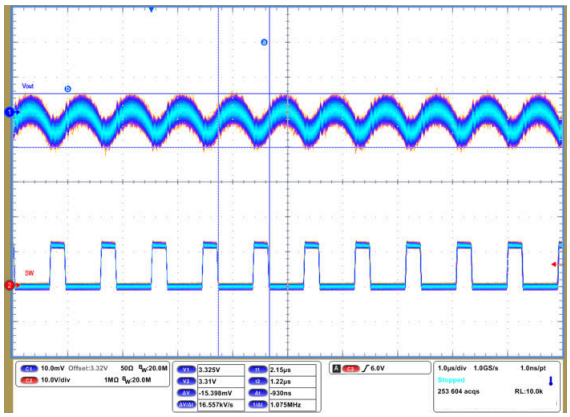
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Auto PFM/PWM

Figure 9-75. Output Voltage Ripple



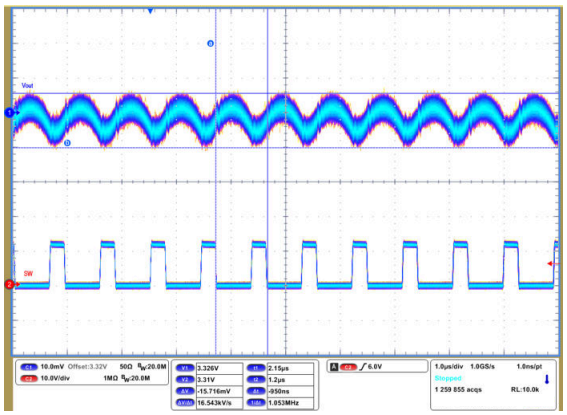
V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Forced PWM

Figure 9-76. Output Voltage Ripple



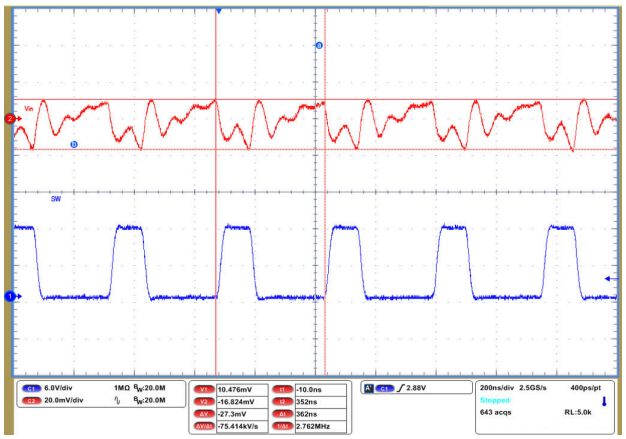
V_{IN} = 12 V | L = 3.3 µH | F_{sw} = 1.0 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Auto PFM/PWM

Figure 9-77. Output Voltage Ripple



V_{IN} = 12 V | L = 3.3 µH | F_{sw} = 1.0 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Forced PWM

Figure 9-78. Output Voltage Ripple



V_{IN} = 12 V | L = 2.2 µH | F_{sw} = 2.5 MHz
V_{OUT} = 3.3 V | I_O = 1 A | Auto PFM/PWM

Figure 9-79. Input Voltage Ripple

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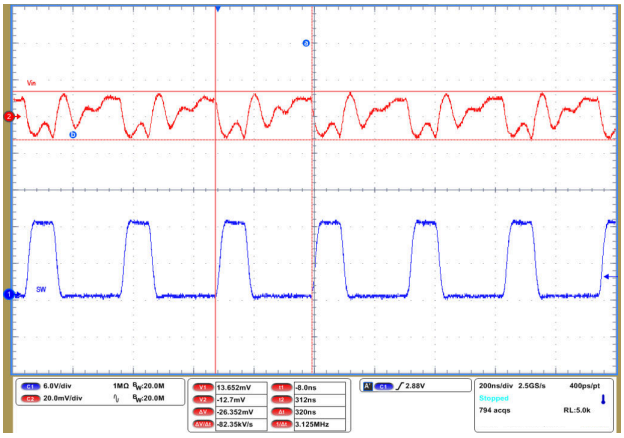
9.2.3 Application Curves (continued)

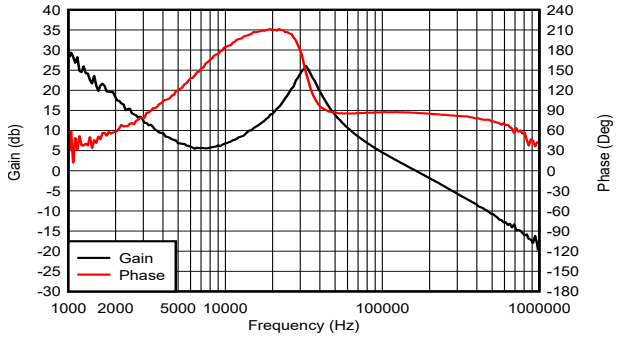


V_{IN} = 12 V
V_{OUT} = 3.3 V

L = 2.2 µH
I_O = 1 A

F_{sw} = 2.5 MHz
Forced PWM

Figure 9-80. Input Voltage Ripple

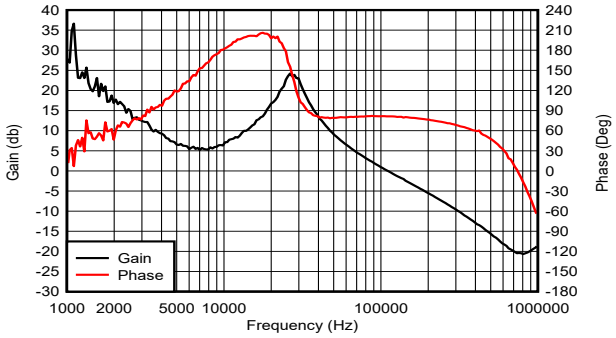


V_{IN} = 12 V
V_{OUT} = 0.6 V

L = 2.2 µH
I_O = 1 A

F_{sw} = 2.5 MHz
Forced PWM

Figure 9-81. Bode Plot



V_{IN} = 12 V
V_{OUT} = 0.6 V

L = 3.3 µH
I_O = 1 A

F_{sw} = 1.0 MHz
Forced PWM

Figure 9-82. Bode Plot

9.3 System Examples

9.3.1 Powering Multiple Loads

In applications where the TPS629210E is used to power multiple load circuits, it is possible that the total capacitance on the output is very large. In order to properly regulate the output voltage, there needs to be an appropriate AC signal level on the VOS pin. Tantalum capacitors have a large enough ESR to keep output voltage ripple sufficiently high on the VOS pin. With low-ESR ceramic capacitors, the output voltage ripple can get very low, so it is not recommended to use a large capacitance directly on the output of the device. If there are several load circuits with their associated input capacitor on a PCB, these loads are typically distributed across the board. This adds enough trace resistance (R_{trace}) to keep a large enough AC signal on the VOS pin for proper regulation.

The minimum total trace resistance on the distributed load is 10 mΩ. The total capacitance n × C_{IN} in Figure 9-83 was 32 × 47 µF of ceramic X7R capacitors.

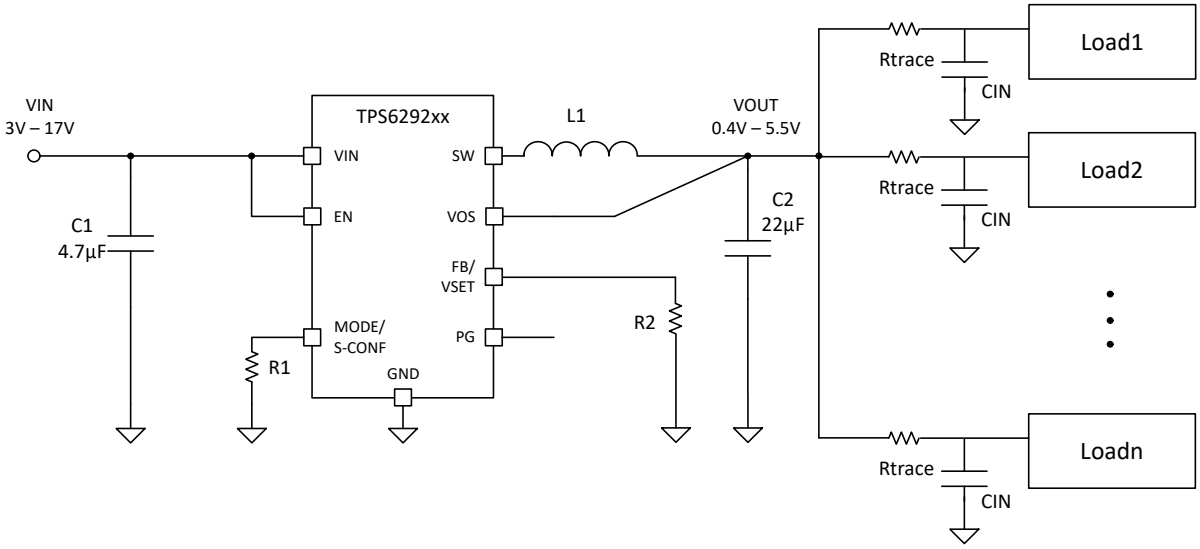


Figure 9-83. Multiple Loads Example

9.3.2 Inverting Buck-Boost (IBB)

The need to generate negative voltage rails for electronic designs is a common challenge. The wide 3-V to 17-V input voltage range of the TPS629210E makes it ideal for an inverting buck-boost (IBB) circuit, where the output voltage is inverted or negative with respect to ground.

The circuit operation in the IBB topology differs from that in the traditional buck topology. Though the components are connected the same as with a traditional buck converter, the output voltage terminals are reversed. See Figure 9-84 and Figure 9-85.

The maximum input voltage that can be applied to an IBB converter is less than the maximum voltage that can be applied to the TPS629210E in a typical buck configuration. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, and not V_{IN} to ground. Thus, the input voltage range of the TPS629210E in an IBB configuration becomes 3 V to 17 V + V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but only negative. Thus, the output voltage for a TPS629210E in an IBB configuration may be set between –0.4 V and –5.5 V.

The maximum output current for the TPS629210E in an IBB topology is normally lower than a traditional buck configuration due to the average inductor current being higher in an IBB configuration. Traditionally, lower input or (more negative) output voltages results in a lower maximum output current. However, using a larger inductor value or the higher 2.5-MHz frequency setting can be used to recover some or all of this lost maximum current capability.

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When implementing an IBB design, it is important to understand that the IC ground is tied to the negative voltage rail, and in turn, the electrical characteristics of the TPS629210E device are referenced to this rail. During power up, as there is no charge in the output capacitor, the IC GND pin (and V_{OUT}) are effectively 0 V, thus parameters such as the V_{IN} UVLO and EN thresholds are the same as in a typical buck configuration. However, after the output voltage is in regulation, due to the negative voltage on the IC GND pin, the device traditionally continues to operate below what could appear to be the normal UVLO/EN falling thresholds relative to the system ground. Thus, special care needs to be taken if the user is utilizing the dynamic mode change feature on the MODE pin of the TPS629210E or driving the EN pin from an upstream microcontroller as the high and low thresholds are relative to the negative rail and not the system ground.

More information on using a DCS regulator in an IBB configuration can be found in the *Description Compensating the Current Mode Boost Control Loop Application Note* and *Using the TPS6215x in an Inverting Buck-Boost Topology Application Note*.

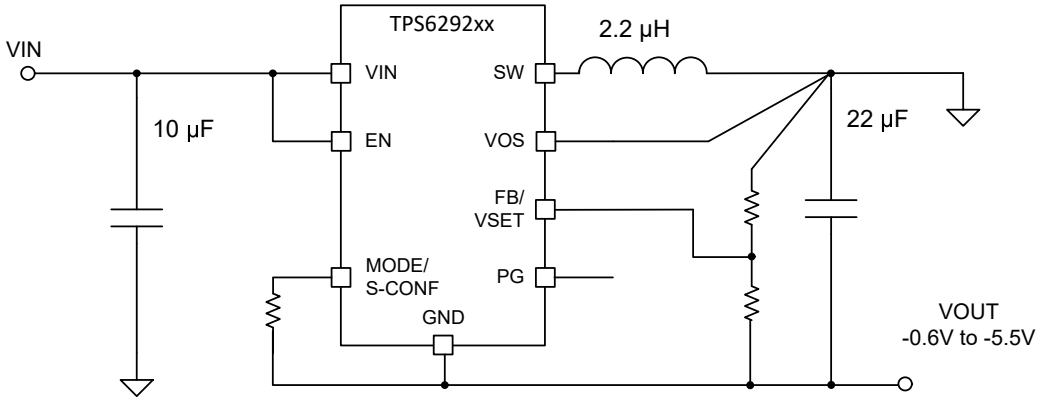

Figure 9-84. IBB Example with Adjustable Feedback

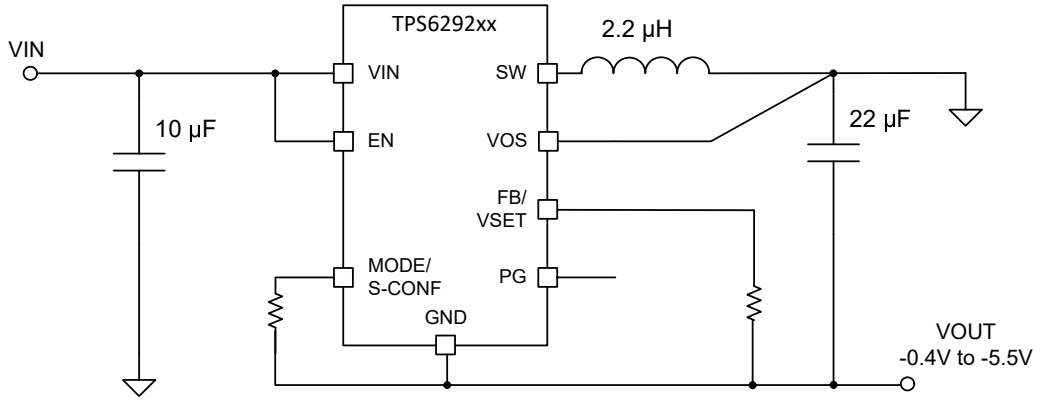

Figure 9-85. IBB Example with Internal Feedback

10 Power Supply Recommendations

The power supply to the TPS629210E needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS629210E.

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11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more so at high switching frequencies. Therefore, the PCB layout of the TPS629210E demands careful attention to make sure proper operation and to get the performance specified. A poor layout can lead to issues like the following:

- Poor regulation (both line and load)
- Stability and accuracy weaknesses
- Increased EMI radiation
- Noise sensitivity

See Figure 11-1 for the recommended layout of the TPS629210E, which is designed for common external ground connections. The input capacitor should be placed as close as possible between the VIN and GND pin of the TPS629210E.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops that conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane. The same applies for the S-CONFIG/MODE and VSET programming resistors.

The package uses the pins for power dissipation. Thermal vias on the VIN, GND, and SW pins help to spread the heat through the PCB.

In case any of the digital inputs (EN or S-CONF/MODE pins) need to be tied to the input supply voltage at VIN, the connection must be made directly at the input capacitor as indicated in the schematics.

The recommended layout is implemented on the EVM and shown in the *TPS629210EEVM User's Guide*.

11.2 Layout Example

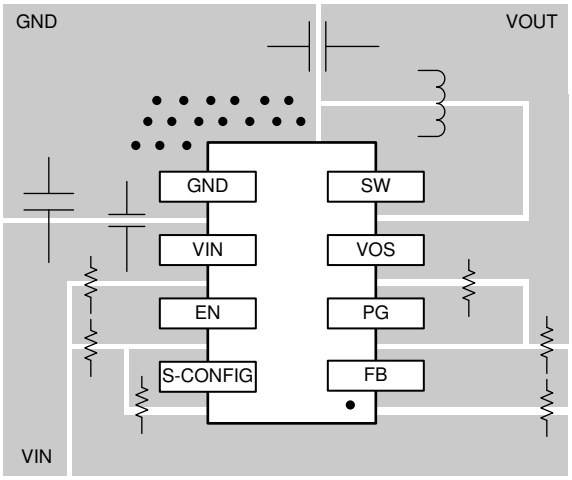

Figure 11-1. TPS629210E Layout

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11.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The following are basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design (for example, increasing copper thickness, thermal vias, number of layers)
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Note* and *Semiconductor and IC Package Thermal Metrics Application Note*.

The TPS629210E is designed for a maximum operating junction temperature (T_J) of 150°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it is recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS629210E device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Note*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Note*
- Texas Instruments, *TPS629210EEVM User's Guide*
- Texas Instruments, *Description Compensating the Current Mode Boost Control Loop Application Note*
- Texas Instruments, *Using the TPS6215x in an Inverting Buck-Boost Topology Application Note*
- Texas Instruments, *Optimizing the TPS62130/40/50/60 Output Filter Application Note*
- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters Application Note*
- Texas Instruments, *Description Compensating the Current Mode Boost Control Loop Application Note*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS629210DRLR-ET	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-55 to 150	T10T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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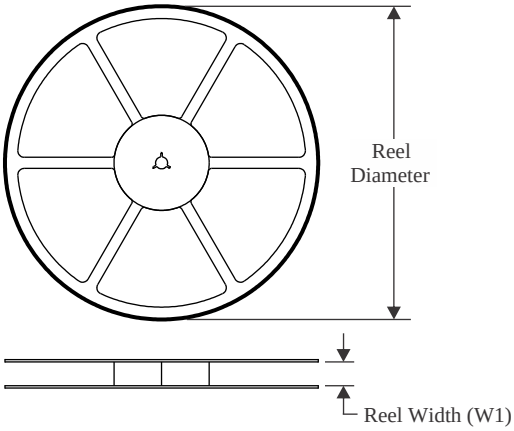
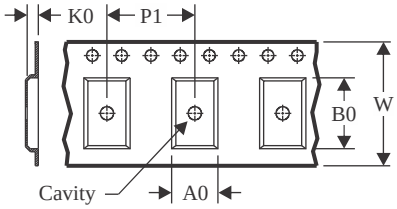
TAPE AND REEL INFORMATION

REEL DIMENSIONS

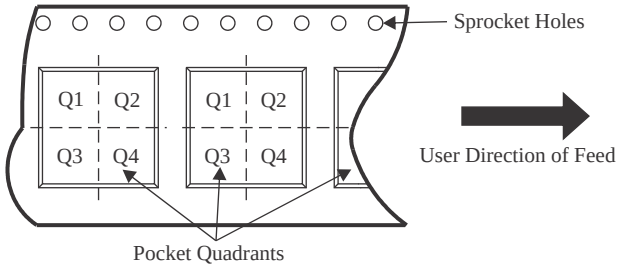


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

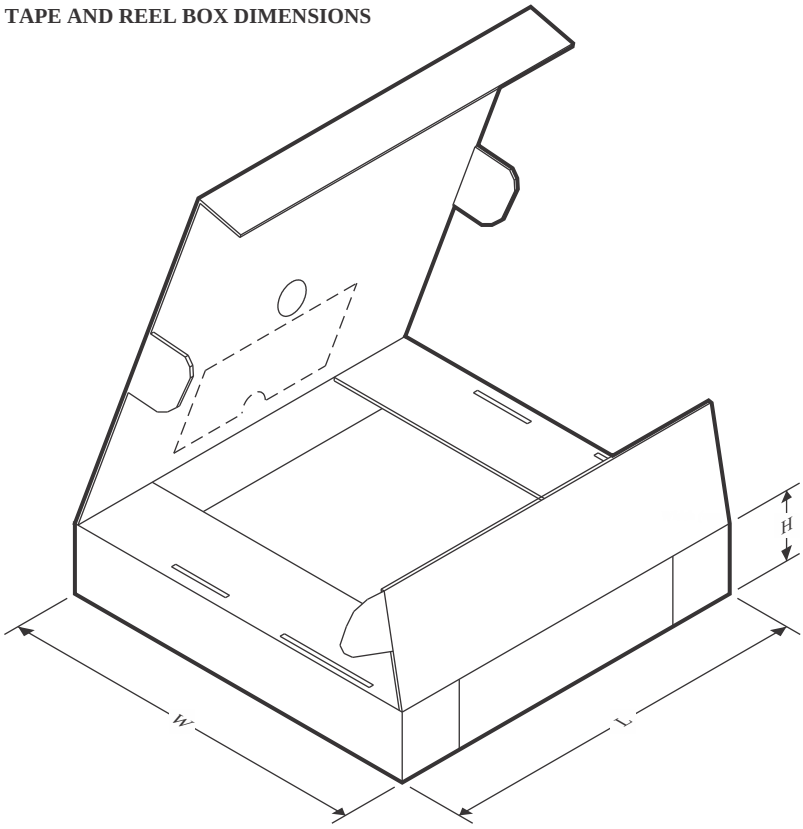
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS629210DRLR-ET	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS629210DRLR-ET	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

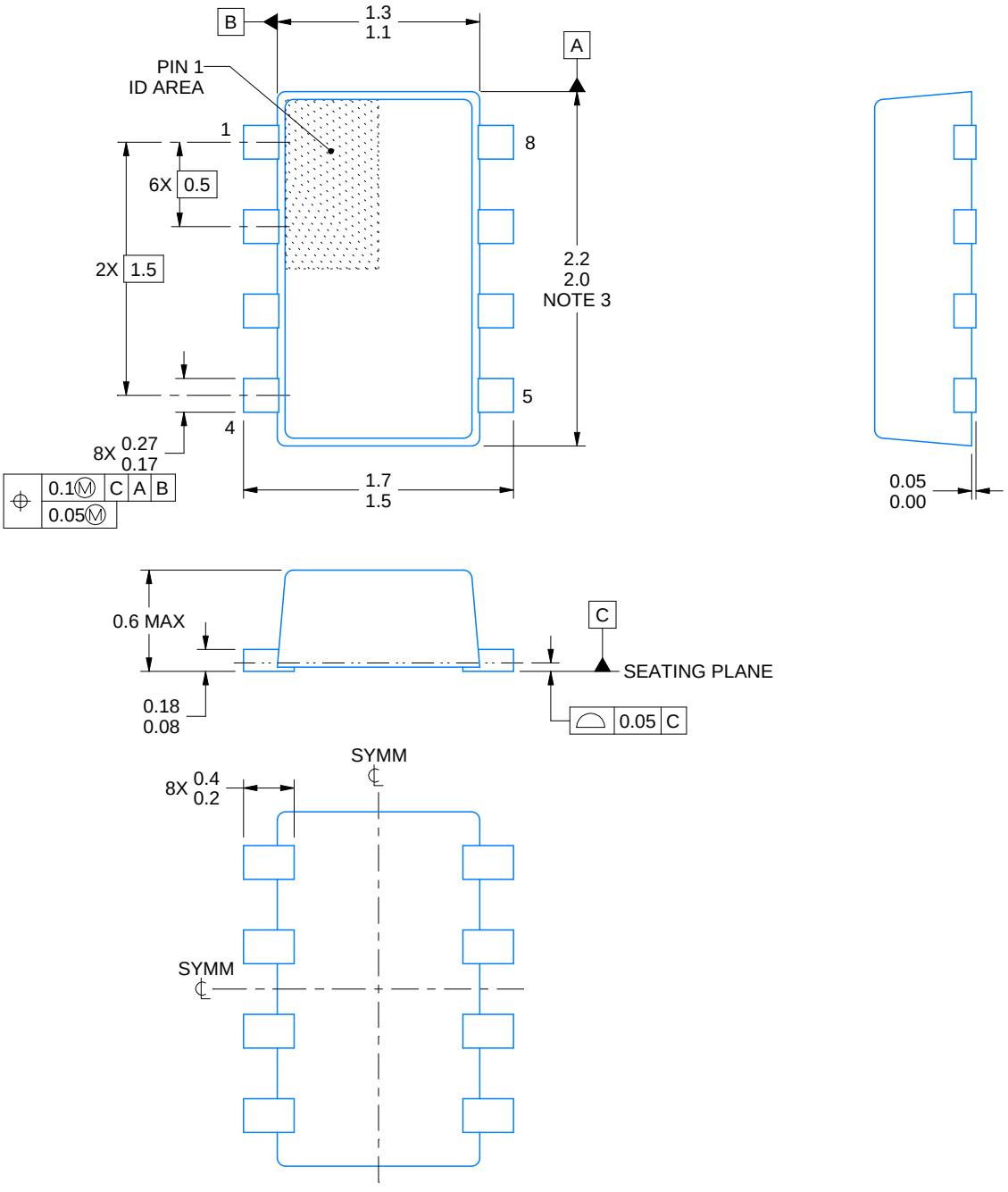


PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

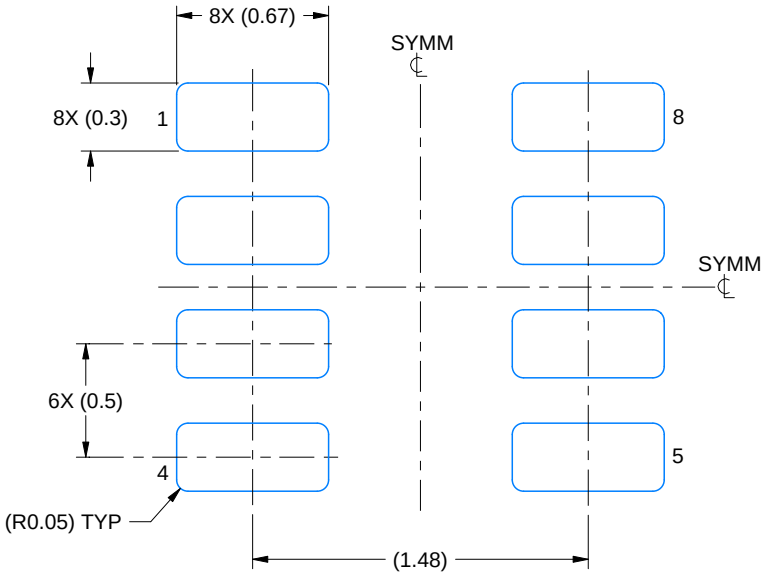
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

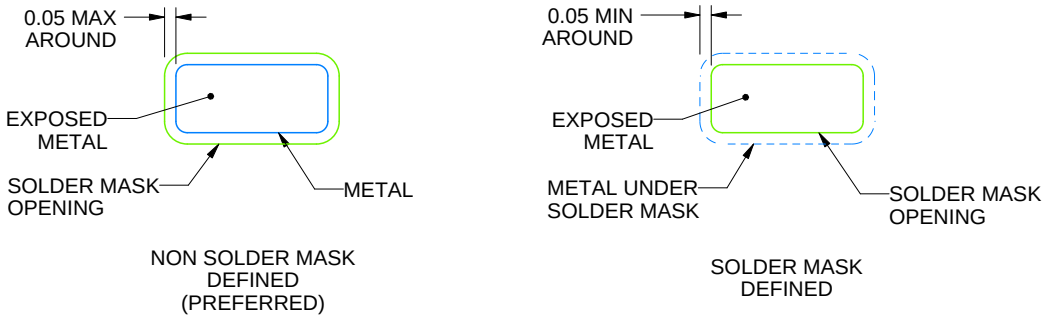
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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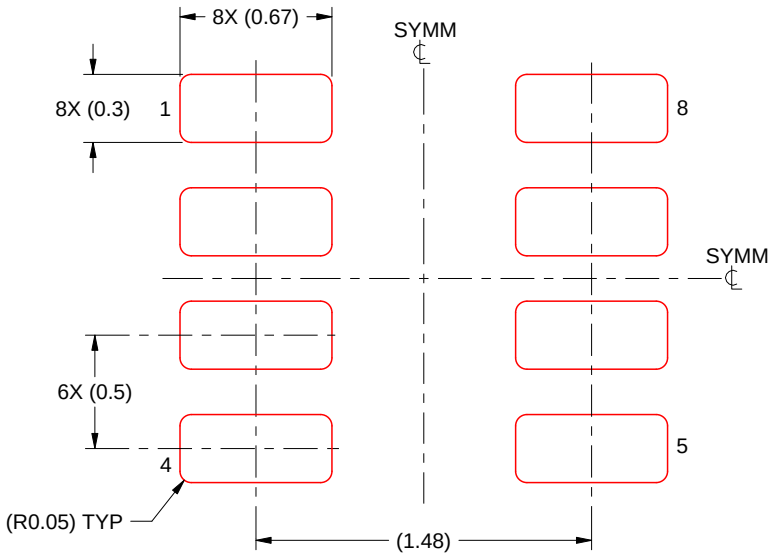
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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